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A Low Phase Noise Crystal Oscillator with a Fast Start-Up Bandgap Reference for WLAN Applications

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Abstract: This article presents the design and implementation of a 40 MHz crystal oscillator (XO) with low phase noise, based on the 55 nm CMOS process, for wireless transceiver systems, particularly those used in Wireless Local Area Network (WLAN). The proposed design employs a bandgap reference circuit that includes a start-up circuit and a low-voltage common-source common-gate current mirror, which ensures that the bandgap reference circuit is powered up effectively across all temperatures and process corners. A low-pass filter is also incorporated at the low dropout regulator (LDO) input to reduce the phase noise of the XO circuit. The experimental results demonstrate that the proposed design achieves a final phase noise of −164.36 dBc/Hz at 100 kHz offset frequency, with a power consumption of 0.444 mW. The test of start-up time is 0.718 ms and the compact chip area is 0.088 mm^2. According to the simulation and test results, the final FOM value calculated in this paper is 209.93 dBc/Hz at 100 kHz offset.

Keywords: low phase noise crystal oscillator; start-up circuit; self-biased bandgap reference; noise-reduction LDO

Citation: Wu, P.; Li, P.; Chen, X.; Cheng, P.; Zhu, J. A Low Phase Noise Crystal Oscillator with a Fast Start-Up Bandgap Reference for WLAN Applications. *Appl. Sci.* **2023**, *13*, 5652. https://doi.org/10.3390/app13095652

Academic Editor: Christos Bouras

Received: 19 March 2023
Revised: 20 April 2023
Accepted: 3 May 2023
Published: 4 May 2023

1. Introduction

Since its invention by Cady [1] in 1923, the crystal oscillator has undergone significant developments, including the resolution of aging issues in the 1940s and 1950s [2], the achievement of low-power operation in the 1970s and 1980s [3,4], and widespread use in wireless communications [5], navigation [6], satellites [7], and radar [8], among other fields. In wireless communication applications, such as radio frequency transceivers [9,10] and digital circuits [11,12], crystal oscillators are utilized to generate stable and accurate reference clocks.

The mechanical resonator of the crystal oscillator primarily uses crystalline quartz, which is anisotropic and can produce various shapes and vibrations through different cutting methods [13]. The AT-cut and SC-cut chips are more commonly used in research. The AT-cut chip is simple to process, smaller in size, and the resonator of this cut type has a better oscillation frequency versus temperature than the SC-cut type, which was used in this paper. The SC-cut crystal requires the incorporation of a B-mode suppression network, which exists near the fundamental frequency of the B-mode-generated vibration [14]. The equivalent model of the crystal oscillator is generally represented as a parallel RLC network [15], with a fixed parallel capacitor C_0, as shown in Figure 1. As the frequency of the crystal oscillator usually coincides with the series resonant frequency of one of the branches, the equivalent model can be simplified to a single branch in parallel with C_0, as illustrated on the right side of Figure 1. Multiple branches exist because the mechanical oscillation occurs at approximate odd harmonics, referred to as overtones [16]. Although

overtone crystal oscillators are not widely used, they can offer higher frequencies by operating the crystal oscillator at the overtone rate. The quality factor of crystal oscillators is much higher than that of ordinary LC circuits, generally exceeding 10,000 [17], making them a favorable replacement for LC oscillators. Additionally, the coupling in the crystal to the external circuit must be weak, $C_0 \gg C_q$ resulting in a small access factor of $p \approx C_q/C_0$ in Figure 1, which further enhances the exceptional frequency stability of quartz crystals. Therefore, crystal oscillators are commonly utilized to provide a highly stable and fixed reference frequency or clock.

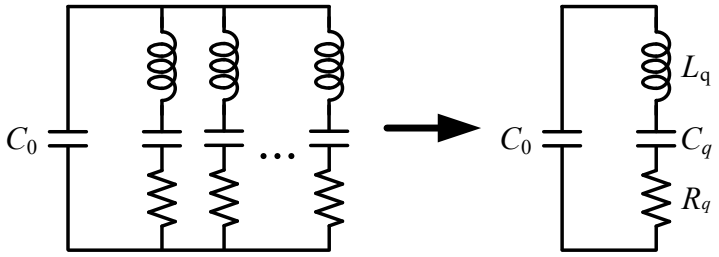


Figure 1. Electrical model of quartz crystal.

In modern electronic information systems technology, phase-locked loops are widely used to generate the required high-frequency clock, and crystal oscillators are used to generate low-noise and low-frequency reference clocks. The XO phase noise can have a considerable impact on the in-band noise of PLL. Therefore, it is essential to have XO circuits that can achieve low phase noise for designing high-performance PLLs and transceivers.

The keys to achieving low phase noise in crystal oscillators are a reduction in noise due to power supply fluctuations and 1/f flicker noise in amplifiers and resonators [18], and the amplifier amplitude modulation to phase modulation (AM to PM) transition due to the nonlinear effects within the crystal [19,20]. Paper [21] has discussed various types of oscillators, where the requirement for high Q and adequate suppression of 1/f flicker phase-type noise is emphasized. A number of oscillator topologies are also discussed, including Pierce, Miller, Butler, and bridged T-configurations. In [22], a LPF (low pass filter) was added to the LDO input to reduce the contribution of supply noise to XO noise, but this circuit does not specify a way to prevent the bandgap reference circuit from entering the simplex state and its phase noise is only −153.1 dBc/Hz at 100 kHz offset. In fact, few papers (if any) have shown a 40 MHz crystal oscillator complete design with phase noise near or below −160 dBc/Hz at 100 kHz offset.

This article will present a low phase noise crystal oscillator circuit that incorporates a fast start-up bandgap reference to meet the requirements of such applications. This paper first describes the background of crystal oscillator circuit research, and then analyzes the bandgap reference with start-up circuit in Section 2.1. In addition, we analyze the noise contribution of the crystal oscillator circuit and explain the design of the crystal oscillator and LDO circuit in Section 2.2. The third chapter is devoted to the analysis and comparison of the simulation and test results of the crystal oscillator. Finally, the last two chapters are the discussion and conclusion of this design.

2. Circuit Composition of Low Phase Noise Crystal Oscillator

Figure 2 depicts the comprehensive configuration of the low phase noise crystal oscillator presented in this research, which comprises a bandgap reference, a low dropout regulator, and a crystal oscillator. In the context of the on-chip system, the crystal oscillator needs to remain operational even when other modules are in sleep mode. Hence, we have devised a crystal oscillator with an independent bandgap reference circuit and a noise-reduction LDO. The LDO is specifically designed to provide 1.2 V power supply, which is low noise, to the crystal oscillator.

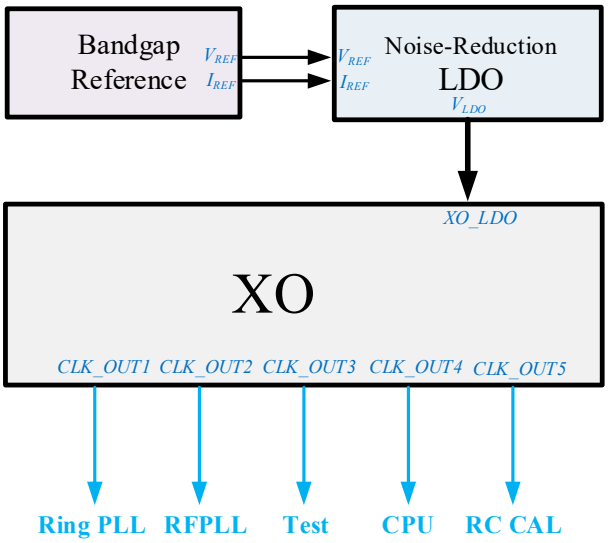


Figure 2. The overall structure of low phase noise crystal oscillator.

2.1. Bandgap Reference with a Start-Up Circuit

The bandgap reference circuit proposed in this paper is shown in Figure 3, which mainly consists of a start-up circuit, a low-voltage common-source common-gate current mirror, diodes and resistors.

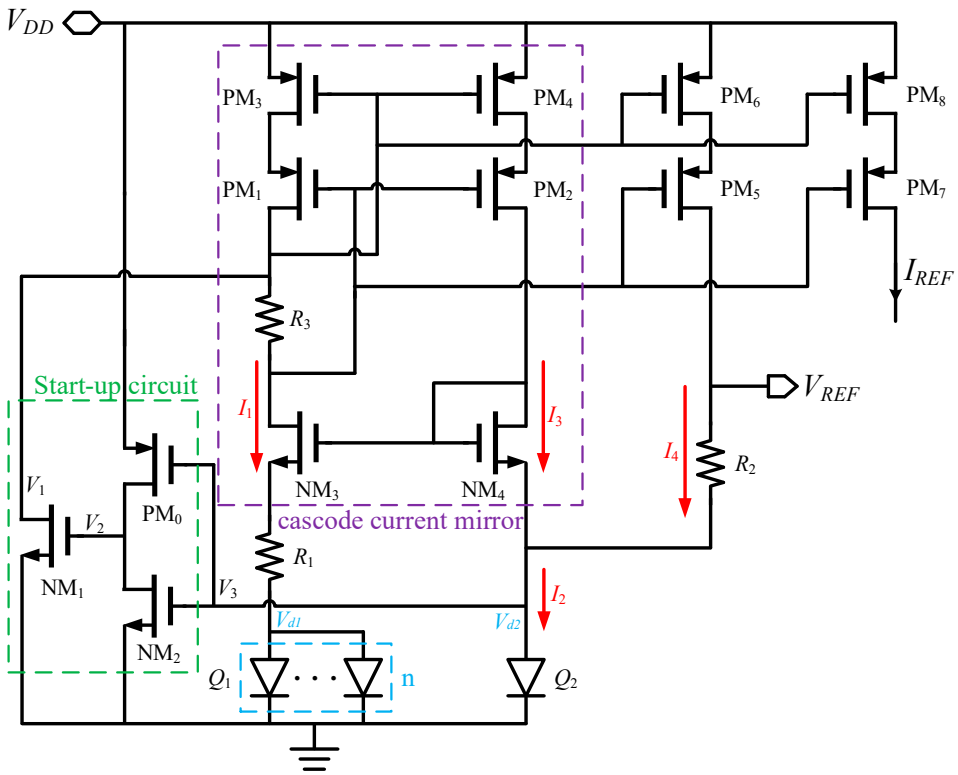


Figure 3. Transistor-level block diagram of a bandgap reference circuit.

For a diode, the relationship between current and voltage is

$$I = I_S\left(e^{\frac{V}{V_T}} - 1\right) \quad (1)$$

in which V is the voltage across the diode, $V_T = kT/q$, and I_S is the reverse saturation current. At room temperature, that is, when T = 300 K, $V_T \approx 26$ mV, so that $e^{\frac{V}{V_T}} \gg 1$. Thus, Equation (1) can be simplified to

$$I = I_S e^{\frac{V}{V_T}} \tag{2}$$

From Equation (2), we can ascertain the relationship between V and I as

$$V = V_T \ln(I/I_S) \tag{3}$$

In Figure 3, the current flowing through Q_1 (Q_1 is regarded as the set of n diodes) is

$$I_1 = nI_S e^{\frac{V_1}{V_T}} \tag{4}$$

If the voltage of the Q_1 anode is V_{d1} and the voltage of the Q_2 anode is V_{d2}, the relationship between V_{d1} and I_1 can be obtained as

$$V_{d1} = V_T \ln\left(\frac{I_1}{nI_S}\right) \tag{5}$$

The current flowing through Q_2 is

$$I_2 = I_s e^{\frac{V_{d2}}{V_T}} \tag{6}$$

The relationship between V_2 and I_2 can be obtained as

$$V_{d2} = V_T \ln\left(\frac{I_2}{I_S}\right) \tag{7}$$

In the circuit we designed, $I_1 = I_3 = I_4$, $I_2 = I_3 + I_4$. So one can ascertain

$$\begin{aligned} I_1 \cdot R_1 &= V_{d2} - V_{d1} \\ &= V_T \ln\left(\tfrac{I_2}{I_S}\right) - V_T \ln\left(\tfrac{I_1}{nI_S}\right) \\ &= V_T \ln\left(n \cdot \tfrac{I_2}{I_1}\right) \\ &= V_T \ln(2n) \end{aligned} \tag{8}$$

Therefore, the current I_1 can be obtained as

$$I_1 = \frac{V_T \ln(2n)}{R_1} \tag{9}$$

We can express the output voltage V_{REF} with the following expression::

$$V_{REF} = \frac{V_T \ln(2n)}{R_1} \cdot R_2 + V_{d2} \tag{10}$$

At room temperature, $\partial_{V2}/\partial_T \approx -1.5$ mV/K. However, $\partial_{VT}/\partial_T \approx 0.087$ mV/K, so we chose $(R_2/R_1)\cdot\ln(2n)\cdot(0.087\text{ mV/K}) = 1.5$ mV/K, that is, $(R_2/R_1)\cdot\ln(2n) \approx 17.2$. In the design of this article, we chose n = 160. Figure 4 shows the change in V_{REF} with temperature obtained by simulation, from which it can be seen that the V_{REF} has changed by a total of 1.9 mV in the range of temperature from −40 °C to 125 °C at the ss process corner, in which the voltage changes are most obvious. In addition, temperature drift coefficient can be calculated to be about 10 ppm in the range of −40 °C to +125 °C. By the way, the ss process corners mentioned above denotes the NFET-Slow and PFET-Slow corner.

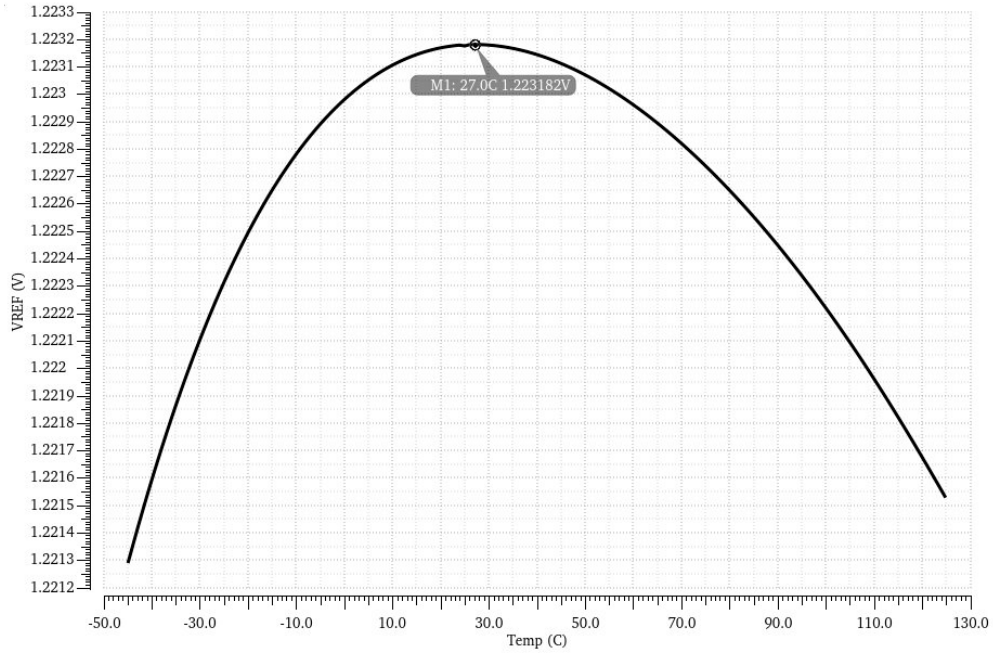


Figure 4. Variation of V_{REF} with the temperature at ss process corners.

An important issue in the power-independent bias circuits described above is the existence of a degenerate bias point, which necessitates a start-up circuit to ensure that the current mirror works properly at power-up. The circuit in the green box in Figure 3 is the start-up circuit designed in this article. Upon powering up, transistor PM_0 turns on due to the gate voltage V_3 of transistor PM_0 being 0 V. The turning on of transistor PM_0 causes the gate voltage V_2 of transistor NM_1 to become high. When V_2 becomes high, transistor NM_1 is turned on, and the conduction of transistor NM_1 causes V_1 voltage to drop. The drop in V_1 voltage causes transistors PM_3 and PM_4 to turn on, which in turn turns on the current mirror. After the current mirror is turned on, the V_3 voltage rises, and the increase in V_3 voltage causes the transistor NM_2 to turn on. The conduction of NM_2 makes the V_2 voltage drop, and the drop of V_2 voltage causes the transistor NM_1 to turn off so that the startup circuit automatically turns off after completing the startup task. In the start-up circuit designed in this article, after the start-up circuit is automatically turned off, transistors PM_0 and NM_2 will still be on, which will consume a certain amount of current. To reduce current consumption, the W/L of transistor PM_0 designed in this design is very small, so the on-resistance of PM_0 will be large. Therefore, the current flowing through transistors PM_0 and NM_2 will be very small, and the simulation shows that the current is 1.7 μA, so the leakage current is negligible. Figure 5 shows the simulation result of the start-up circuit, and the process corner and temperature are set to tt (−40 °C), tt 55 °C, tt 125 °C, ss 125 °C, ff (−40 °C). As can be seen from the figure, the design start-up circuit is fully capable of covering all process corners and temperatures and the bandgap reference can produce stable voltage after 1.62 μs in the worst case.

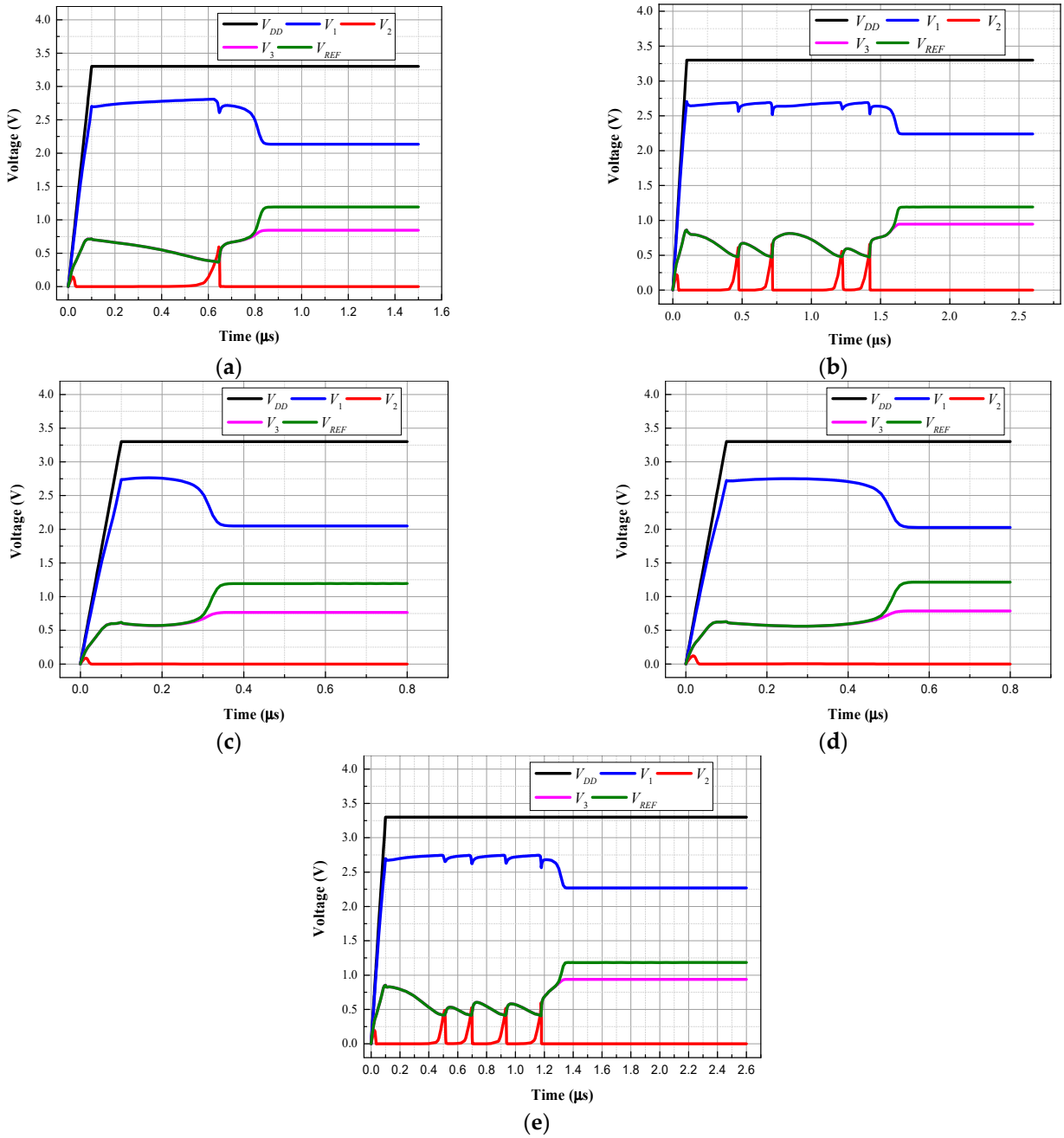


Figure 5. Simulation results of start-up circuits at different process corners and temperatures: (**a**) tt 55 °C, (**b**) tt (−40 °C), (**c**) tt 125 °C, (**d**) ss 125 °C, (**e**) ff (−40 °C).

2.2. Design of Low Phase Noise Crystal Oscillator

2.2.1. Analysis of Noise Contribution of LDO

LDO is an effective means of attenuating the input power supply ripple and mitigating noise. In WLAN chips, the crystal oscillator is typically employed as the reference clock source of PLL, and it is subject to stringent phase noise requirements. The major contributors to the oscillator noise are LDO power supply noise, device noise within the oscillation circuit, and resistive thermal noise. Since these sources of noise are uncorrelated, the phase noise of the crystal oscillator can be formulated using Equation (11).

$$L_{TOTAL} = \sqrt{L_{LDO}{}^2 + L_{TRAN}{}^2 + L_R{}^2} \quad (11)$$

L_{TOTAL}, L_{LDO}, L_{TRAN} and L_R are the total output phase noise of the crystal oscillator, the LDO output phase noise, the noise of transistors and resistors in the oscillator at a frequency offset f_m, respectively. When the crystal oscillator is used as the reference clock source of the PLL in the WLAN chip, its integral noise range is often 10 kHz–10 MHz [23,24], and the phase noise of crystal oscillators mainly affects the in-band noise of the PLL, while the bandwidth of the PLL is generally a few hundred kHz to a few MHz. Thus, in this paper, f_m is selected as 100 kHz.

The traditional LDO using NMOS power tube is shown in Figure 6.

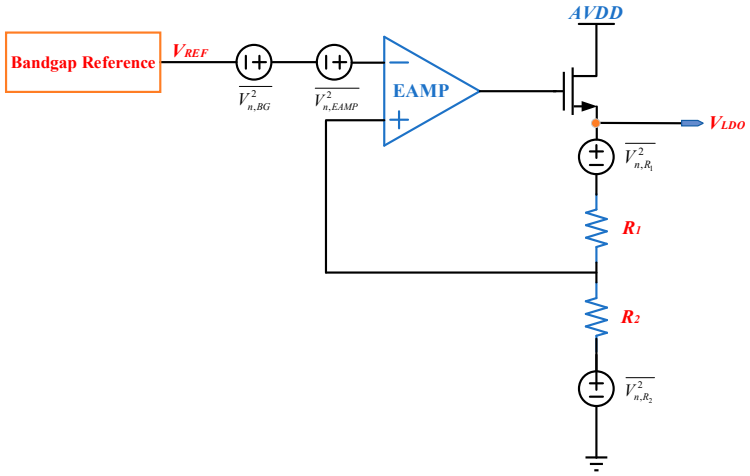


Figure 6. The structure of traditional LDO. BG: bandgap reference.

The output noise of the LDO consists of three main components: $\overline{V_{n,BG}^2}$ is the noise of the bandgap reference output voltage, $\overline{V_{n,EAMP}^2}$ is the equivalent input noise of the error amplifier (EAMP), and $\overline{V_{n,R_1}^2}$ and $\overline{V_{n,R_2}^2}$ are the noise of resistors. Since there is no correlation between these types of noise, the equivalent output noise of the LDO can be expressed as Equation (12) [25].

$$\overline{V_{n,LDO}^2} = \int_{f_1}^{f_2} \left[\left(\overline{V_{n,BG}^2} + \overline{V_{n,EAMP}^2} \right) \left(1 + \frac{R_1}{R_2} \right)^2 + \overline{V_{n,R_1}^2} + \overline{V_{n,R_2}^2} \left(\frac{R_1}{R_2} \right)^2 \right] df \quad (12)$$

The expression (12) reveals that the resistors R_1 and R_2 in the feedback network themselves introduce some thermal noise and also affect the contribution of the LDO equivalent input noise to the output voltage noise. Secondly, the two resistors will have a large area overhead. Due to the $V_{BG} = V_{LDO}$ of this design, the LDO can use a non- resistive non- resistivefeedback structure, then we can obtain the feedback coefficient $\beta = 1$. For the impact of a non-resistive feedback structure, we need to connect a resistor in series with the compensation capacitor to solve the stability problem.

As shown in Figure 7, removing the LDO feedback resistors, the equivalent output noise of the LDO can be changed as in Equation (13).

$$\overline{V_{n,LDO}^2} = \int_{f_1}^{f_2} \left(\overline{V_{n,BG}^2} + \overline{V_{n,EAMP}^2} \right) df \quad (13)$$

As demonstrated by Equation (13), the impact of the bandgap reference and EAMP-generated noise on the LDO output voltage noise cannot be overlooked. In order to mitigate this impact, it is customary to introduce an RC low-pass filter with a sufficiently low cutoff frequency at the LDO input. To select an appropriate RC low-pass filter, this study presents a design in the subsequent section. Additionally, PN is the control signal of the system and is accessed via SPI. When the LDO output is normal, the PN signal is low and the NMOS tube is cut off to prevent the LDO output from shorting out and the noise contribution from

this NMOS is very low and negligible. When the LDO output is turned off, the PN signal is high.

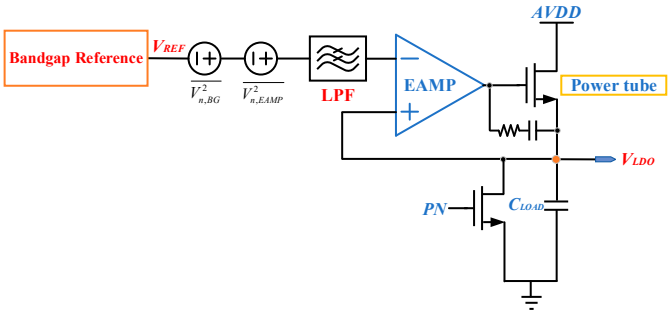


Figure 7. Broadband LDO non-resistive feedback structure. BG: bandgap reference.

2.2.2. Design of Crystal Oscillator

The crystal oscillator structure proposed in this article is shown in Figure 8.

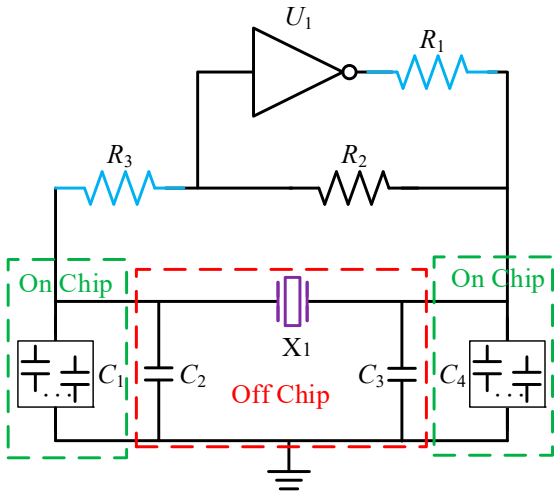


Figure 8. Structure of Crystal Oscillator.

Crystal X_1 operates in the inductive region described above, that is, crystal X_1 is used as an inductor. The inverter U_1 provides a 180° phase shift, and the crystal X_1 and the capacitors C_1~C_4 on both sides form a π network to provide an additional 180° phase shift. R_2 acts as the feedback resistor, biasing inverter U_1 at $VDD/2$, such that it operates in the linear region as an amplifier with maximum gain, as shown in Figure 9. Inverter U_1 amplifies noise, including thermal noise from crystals, in the series-parallel frequency range [4], which leads to oscillator oscillation.

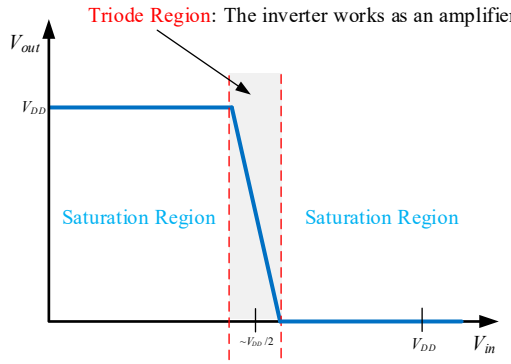


Figure 9. Inverter transfer function.

R_1 serves a dual purpose in this design, as described in the following passage. Firstly, R_1, in conjunction with capacitors C_3 and C_4, forms a low-pass filter which attenuates spurious oscillations and delivers a clean output signal. Secondly, R_1 limits the driving power of the quartz crystal to prevent the exceeding of the allowable driving power, particularly in the case of low-power quartz crystals, which can cause damage or accelerate crystal ageing. R_3, on the other hand, plays a role in limiting the amplitude of the signal that enters inverter U_1, thus preventing the signal from breaking through the gate oxide layer of U_1. However, since R_3 also introduces noise, it is crucial to select an appropriate resistance value to avoid excessive noise, as illustrated in Figure 10.

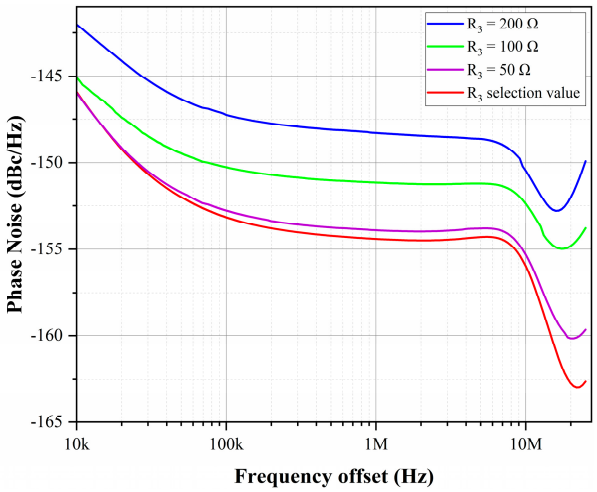


Figure 10. Comparison of phase noise of crystal oscillator with different R_3 resistance values.

Crystal X1 and external capacitors are components soldered to the printed circuit board (PCB), as shown in the red box in Figure 8. Except for the devices in the red box, the devices in Figure 8 are integrated into the chip, with C_1 and C_4 being programmable capacitors to fine-tune the oscillation frequency of the crystal oscillator.

The transistor-level circuit of inverter U_1 designed in this article is shown in Figure 11 as a CMOS amplifier with enable control, with PU and PD as complementary enable control signals. When PU is high and PD is low, the circuit vibrates normally; when PU is low and PD is high, the circuit enables shutdown, PM_1 and NM_1 are turned off, XO is turned off, and the circuit enters a low-power mode. The PU and PD signals mentioned above come from the system and are used to control the switching of the crystal oscillator via SPI.

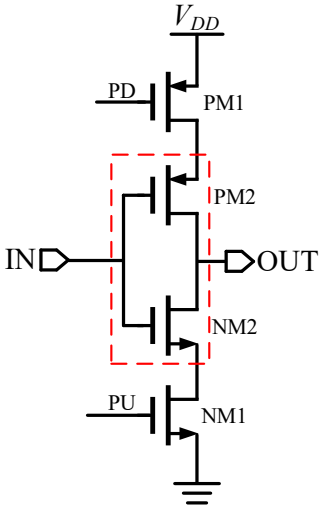


Figure 11. Structure of inverter U_1.

2.2.3. Design of Broadband LDO

Figure 12 depicts the LDO circuit designed with a closed-loop configuration comprising a conventional power tube, error amplifier, and sampling feedback. The LDO employs NMOS transistors as the power tube, leading to improved response time and reduced on-chip capacitance area. This configuration is also referred to as a broadband regulator. The amplifier input adopts a folded common-source and common-gate structure, which enhances common-mode rejection and output impedance. The op-amp gain (A_v) is obtained by multiplying the cross-conductor of the input tube by the output impedance. The power tube is designed with a source-follower configuration and has a gain almost equal to 1, hence, the gain of the complete loop is the product of the op-amp gain and the feedback coefficient $A_v\beta$. By eliminating feedback resistors, the feedback coefficient β is 1 and, therefore, the loop gain is equal to the op-amp gain.

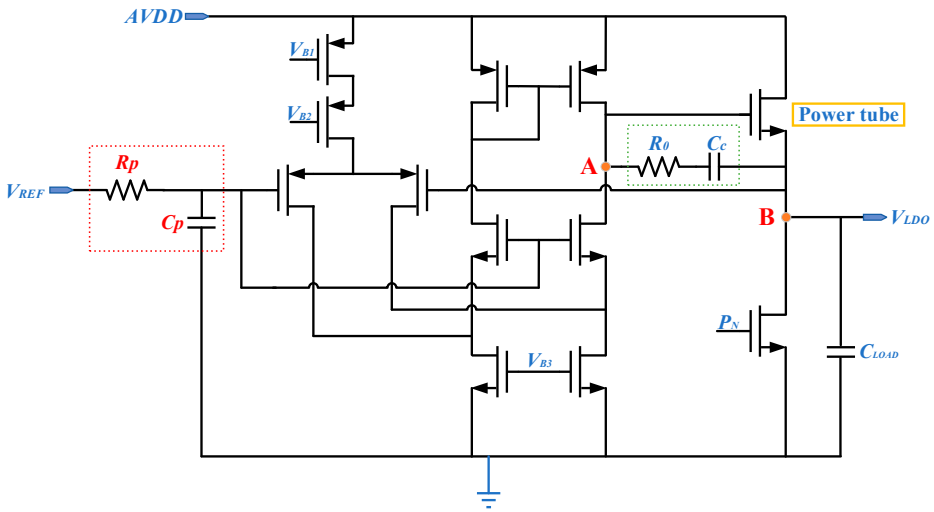


Figure 12. Transistor-level block diagram of the broadband LDO.

Regarding stability, the primary pole of the LDO is located at the op-amp's output, while the secondary pole is at the power tube's output, which restricts the load current at the output and complicates in-band compensation for capacitance. Even if there is only a small amount of load capacitance at the output, it can either provide or absorb the load current during transient response. As a result, a capacitor can be added at the output of the op-amp to create a low-frequency main pole p_0, using high resistance at this location.

$$p_0 = \frac{1}{2\pi R_{oe} C_c} \tag{14}$$

In the aforementioned equation, the equivalent impedance of the LDO output node is represented by R_0, while the compensation capacitor is represented by C_c. It is worth noting that the secondary pole p_1 is located at the LDO output node.

$$p_1 = \frac{g_{m,power}}{2\pi C_{load}} \tag{15}$$

The $g_{m,\,power}$ in the above equation is the trans-conductance value of the power tube, and C_{load} is the load capacitance value. The structure without feedback resistors of the LDO causes the secondary pole to move too close to the main pole at the time of no-load, making stability a problem. Therefore, a zero point needs to be introduced to offset the effect of the secondary pole. In this paper, a resistor is connected in series with the compensation

capacitor to form a current-limiting zero-point z_0, which is placed at a higher frequency than the secondary pole.

$$z_0 = \frac{1}{2\pi R_0 C_c} \tag{16}$$

R_0 in the above equation is the zero-point compensation resistor value.

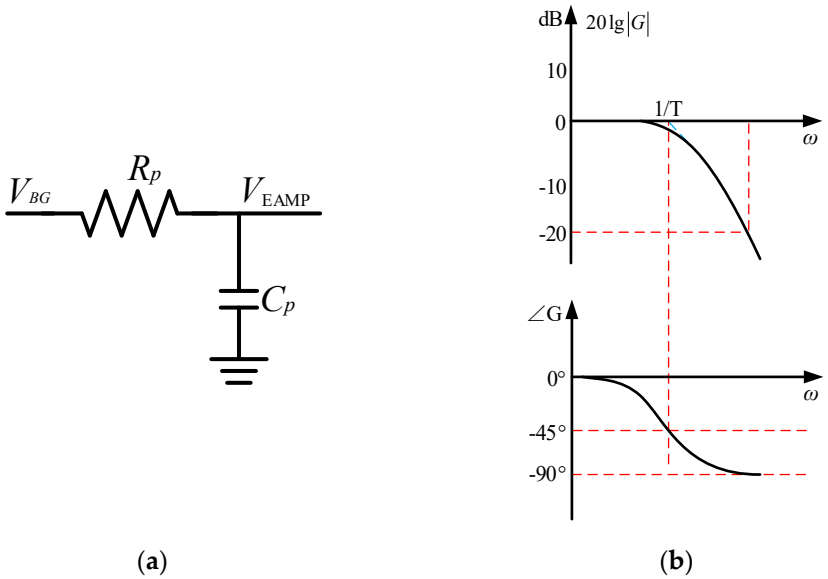
The design of a crystal oscillator with low phase noise is crucial for a phase-locked loop with low phase noise, as the phase noise of the oscillator has a significant impact on the in-band noise [26]. Among various sources influencing the phase noise of the crystal oscillator, power supply noise has a substantial effect due to the high Q value of the crystal. Neglecting power supply noise can result in a low phase noise of the crystal oscillator, even if it is not optimized. Therefore, it is crucial to optimize power supply noise to design a low phase noise crystal oscillator. This paper proposes the use of an RC low-pass filter to suppress bandgap reference noise, and its structure is depicted in Figure 13a. The transfer function of the proposed RC low-pass filter is

$$H(s) = \frac{V_{LDO}}{V_{EAMP}} = \frac{1}{1 + R_p C_p} \tag{17}$$

Let $RC = T$, and the logarithmic amplitude-frequency characteristic of Equation (17) is

$$\begin{aligned} 20\lg|G(j\omega)| &= 20\lg\frac{1}{\sqrt{T^2\omega^2+1}} \\ &= -20\lg\sqrt{T^2\omega^2+1} \end{aligned} \tag{18}$$

The Bode plot of Equation (17) is shown in Figure 13b, from which it can be seen that the cutoff frequency is $1/T$. To minimize the effect of bandgap reference noise on the crystal oscillator phase noise while taking area into account, we chose a cutoff frequency of 10 kHz.



(**a**) (**b**)

Figure 13. (**a**) RC low-pass filter, (**b**) logarithmic plot of RC low-pass filter.

Figure 14 depicts a comparison of the phase noise of a crystal oscillator with and without the proposed RC low-pass filter. The plot reveals that the inclusion of the filter leads to a significant reduction of approximately 11.21 dBc/Hz at 100 kHz offset in the phase noise of the crystal oscillator. The results demonstrate the effectiveness of the proposed approach in minimizing the phase noise of the oscillator.

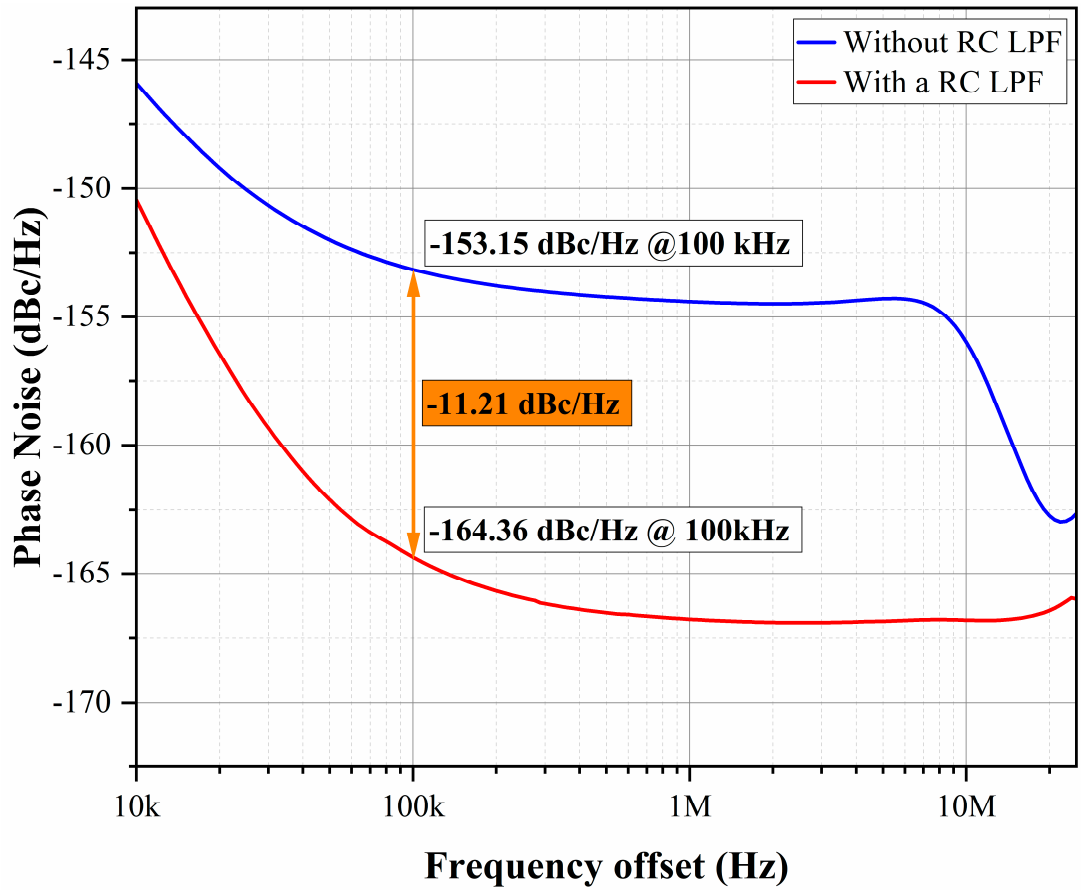


Figure 14. Comparison of phase noise of crystal oscillator with or without RC low-pass filter.

3. Results and Analysis

The final implementation of the low phase noise crystal oscillator is presented in Figure 15, featuring five outputs to cater to multiple modules, with one designated for testing purposes. The open cover diagram of this designed crystal oscillator after the flow of the chip is shown in Figure 16. The fabricated chip, which incorporates a bandgap reference circuit, an LDO circuit, and output buffers, occupies a total area of 0.088 mm^2 in a 55 nm CMOS process. During testing, the oscillator demonstrates stable oscillations at a frequency of 40 MHz once a crystal is attached to the printed circuit board.

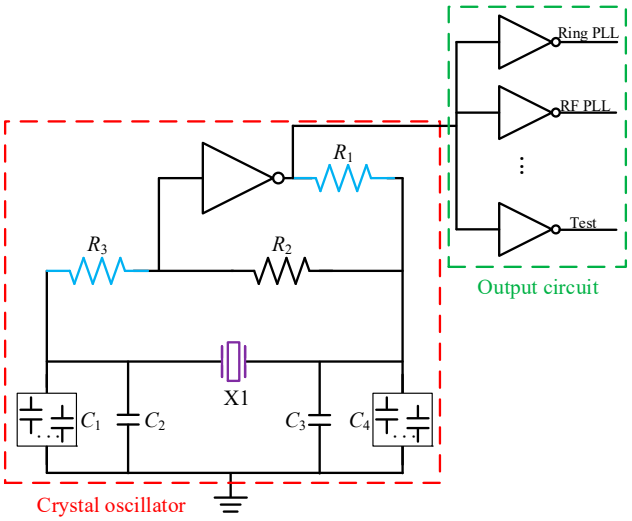


Figure 15. Complete circuit diagram of crystal oscillator.

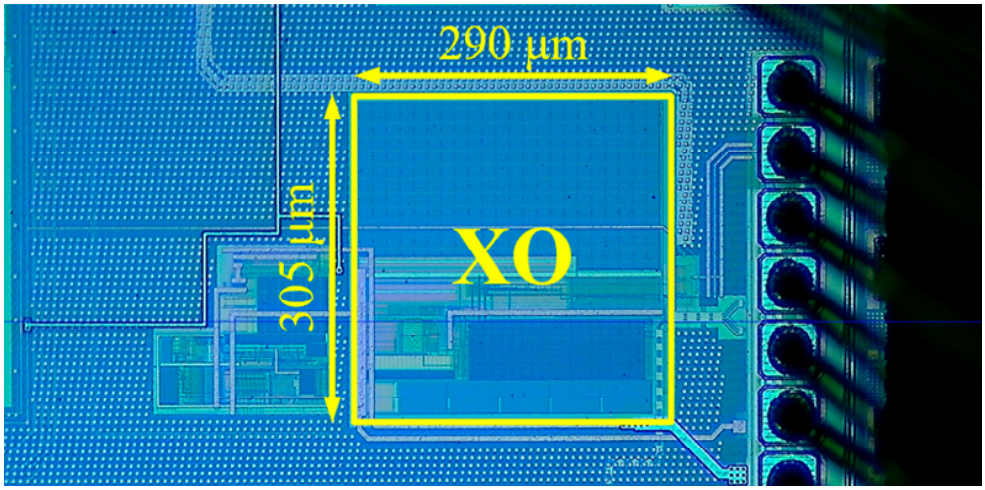


Figure 16. Photomicrograph of the XO chip.

The crystal oscillator chip designed in this study is powered by a 3.3 V external power supply, with 1.2 V generated by an LDO circuit inside the chip specifically for the oscillator. The chip consumes a total of 369.8 µA of power and exhibits a phase noise of −164.36 dBc/Hz at a 100 kHz offset, as illustrated in Figure 14. Additionally, the start-up time test conducted on this crystal chip indicates a value of 0.718 ms, as shown in Figure 17.

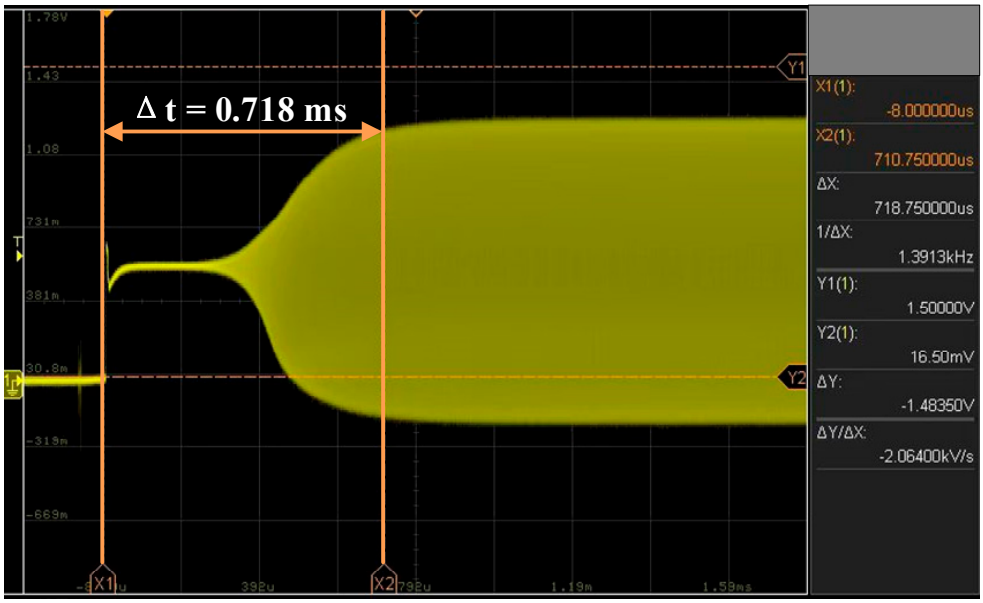


Figure 17. Test Result of start-up time of XO circuit.

The simulation test results of the crystal oscillator designed in this article are summarized in Table 1.

Table 1. Summary of simulation and test results of crystal oscillator.

Index	Data	Unit
Technology	55	nm
Output frequency	40	MHz
Power loss	0.444	mW
Phase noise	−150.45 @10 kHz offset −164.36 @100 kHz offset −166.75 @1 MHz offset	dBc/Hz dBc/Hz dBc/Hz
Start-up time	0.718	ms
Chip area	0.088	mm^2
FoM [1] (@100 kHz offset)	209.93	dBc/Hz

[1] $FoM = |PN| + 20\log_{10}(f_0/\Delta f) - 10\log_{10}10(P_{DC}/1mW)$.

4. Discussion

In the realm of modern electronic information system technology, crystal oscillators are popular choices as reference clock sources. The output phase noise of reference clock sources is now considered a limiting factor for circuit and system performance in several applications, such as satellite communications and radar systems [27,28]. To achieve low phase noise in a crystal oscillator, several measures need to be taken to reduce noise contributions from various sources, such as the amplifier flicker noise, resonator flicker noise, resistor thermal noise, power supply noise, and nonlinear effects of the crystal [29–31]. In the future, researchers can focus on developing crystal oscillators with ultra-low phase noise [32,33], minimal frequency and temperature drift [34,35], fast start-up [36,37], and ultra-low power consumption [38,39], in order to cater to various application scenarios.

Table 2 presents a summary of the performances of the proposed crystal oscillator and a comparison with previous works [22,32,40,41]. A close analysis of the data in the table reveals that the phase noise of the crystal oscillator in this paper surpasses those found in similar research.

Table 2. Comparison with previous works.

Index	VLSI [40]	JSSC [22]	RFIC [41]	JSSC [32]	This Work
Frequency (MHz)	39.00	39.25	38.40	54.00	40.00
Technology (nm)	40	65	65	65	55
Voltage (V)	0.7	3.3	1.4	N/A	1.2
Phase noise (@100 kHz offset) (dBc/Hz)	−151.50	−153.10	−145.00	−144.60	−164.36
Start-up time (ms)	0.259	3.900	1.250	N/A	0.718
Power loss (μW)	9.2	19	5234	8200	443.8
Chip area (mm^2)	0.605	0.088	0.090	0.150	0.088
FoM [1] (@100 kHz offset)	213.68	212.19	179.50	180.11	209.93

[1] $FoM = |PN| + 20\log_{10}(f_0/\Delta f) - 10\log_{10}10(P_{DC}/1mW)$.

5. Conclusions

This study presents a low phase noise crystal oscillator with 40 MHz frequency outputs, fabricated using a 55 nm CMOS process. The oscillator provides a low-noise reference clock source suitable for high-performance PLL and digital circuits. The design employs a self-biased low-voltage common-source common-gate current mirror with a start-up circuit to ensure proper and fast powering up across various process corners and temperatures. In addition, under the condition that the XO circuit can operate properly, the optimal R_3 resistor value is selected to reduce the phase noise. A low-pass filter is also incorporated into the LDO input to minimize the impact of power supply noise on crystal oscillator noise. The crystal oscillator achieves the 40 MHz output phase noise of −164.36 dBc/Hz at 100 kHz offset. Testing verifies normal start-up within 0.718 ms. According to the simulation and test results, the final FOM value calculated in this paper was 209.93 dBc/Hz at 100 kHz offset.

Author Contributions: Methodology, P.W., P.L., X.C., P.C. and J.Z.; software, P.W., P.L., P.C. and J.Z.; validation, P.W., P.L., P.C. and J.Z.; formal analysis, P.W., P.L., X.C. and J.Z.; investigation, P.W., P.L., X.C. and J.Z.; resources, P.W., P.L., P.C. and J.Z.; data curation, P.W., P.L., X.C. and J.Z.; Writing—original draft preparation, P.W. and P.L.; writing—review and editing, P.W., P.L., X.C. and P.C.; visualization, P.W.; supervision, P.W., P.L., P.C. and J.Z.; project administration, P.W., P.L., X.C., P.C. and J.Z.; funding acquisition, P.C. All authors have read and agreed to the published version of the manuscript.

Funding: The project fund comes from Zhejiang CASEMIC Electronics Technology Co., Ltd.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data in this paper are all from simulation and test results of real circuits, and there is no data plagiarism or falsification. Due to project confidentiality requirements, we regret that we cannot release more details of the data at this time.

Conflicts of Interest: The authors declare no conflict of interest.

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