applied sciences

MDPI

Communication

Analysis of Channel Potential Recovery According to the Back Pattern in 3D NAND Flash Memory

Gyunseok Ryu, Hyunju Kim, Jihwan Lee and Myounggon Kang *

Department of Electronics Engineering, Korea National University of Transportation, Room No. 326, Smart ICT Building, 50 Daehak-ro, Chungju-si 27469, Republic of Korea
* Correspondence: mgkang@ut.ac.kr; Tel.: +82-43-841-5164

Abstract: This study analyzed the recovery of channel potential according to the program states of adjacent cells. When the verify operation ended, and all voltages dropped to 0 V and the decreased potential of the floating channel caused by the down-coupling phenomenon was recovered continuously over time, regardless of the program states of adjacent WLs. The extent of channel potential recovery showed a similar tendency to that of the variation in the electron concentration of the floating channel. The electron–hole pair recombination decreased the electron concentration, resulting in channel potential recovery. When the adjacent WLs were programmed in a low state, additional electron–hole pair recombination and hole diffusion occurred in the floating channel. Therefore, the channel potential recovered quickly when the adjacent WLs programmed in a low state compared to when they programmed in a high state.

Keywords: 3D NAND flash memory; channel potential; down-coupling phenomenon (DCP); electron-hole pair recombination; carrier diffusion; TCAD

Citation: Ryu, G.; Kim, H.; Lee, J.; Kang, M. Analysis of Channel Potential Recovery According to the Back Pattern in 3D NAND Flash Memory. *Appl. Sci.* **2023**, *13*, 3388. https://doi.org/10.3390/app13063388

Academic Editor: Antonio Di Bartolomeo

Received: 27 January 2023
Revised: 21 February 2023
Accepted: 23 February 2023
Published: 7 March 2023

1. Introduction

Owing to the increasing demand for semiconductors in various markets, the technology and performance of NAND flash memory has evolved, resulting in improved speed, high density, and low power consumption [1–7]. However, 2D NAND flash memory has certain limitations in terms of technicalities such as device scaling issues and lithography [7–11]. Eventually, 3D NAND flash memory replaced 2D NAND flash memory [11–14]. Compared to 2D NAND flash memory, the capacity of 3D NAND flash memory can be increased by vertically stacking cells. As the cells are stacked vertically, the main cells of 3D NAND flash memory based on the ultra-thin body (UTB) structure are not directly connected to the body. Owing to the floating body effect in vertical string channels, new phenomena such as the down-coupling phenomenon (DCP) and natural local self-boosting (NLSB) have occurred [15–22].

The DCP, which describes channel potential drop, was reported for the first time in 2016 [15]. The channel potential of the program inhibit string becomes negative during verify operation. At the end of the verify operation, the word line (WL) voltage decreases from the pass voltage, V_{pass}, to zero. When the WL voltage reaches the threshold voltage of the programmed cells, the corresponding cells are turned off, and the channel changes to the floating state. The channel potential changes along with the WL voltage owing to the floating channel, which is not connected to the bit line (BL). When the WL voltage reaches 0 V, capacitive coupling occurs between the WLs and the channel, resulting in negative channel potential. The DCP causes poor boosting efficiency in the program inhibit string, which can increase the program disturbance during the program operation. Since the program disturbance affects the reliability of a device, it should be minimized. In a previous paper, research was conducted on phenomena that occur during the program operation, not immediately after the verify operation. However, the negative channel potential of the program inhibit string gradually recovers over time. Therefore, adjusting recovery time could increase boosting efficiency and reduce program disturbance during

the program operation. In this study, we analyzed the transient channel potential recovery in the program inhibit string caused by the DCP using 3D technology computer-aided design (TCAD) simulation (ATLAS Silvaco^{TM}) [23].

2. Structure and Simulation Set-Up

Figure 1a shows the program inhibit string of a 3D NAND flash memory structure comprising 16 WLs, a string select line (SSL), a ground select line (GSL) and a common source line (CSL). Table 1 summarizes the device parameters and voltage bias conditions.

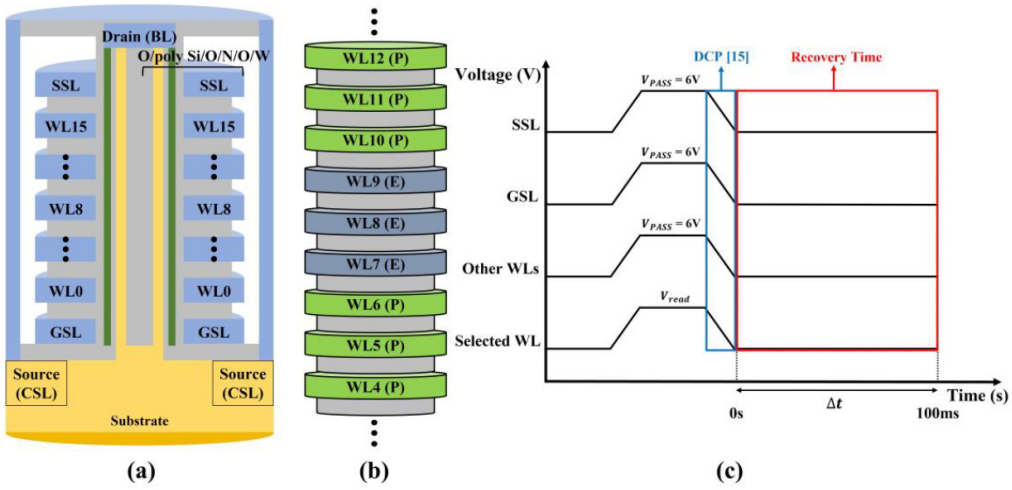

Figure 1. (**a**) 3D NAND string structure used in TCAD simulation with 16 WLs, string select line (SSL), ground select line (GSL) and common source line (CSL). Values of the device parameter are listed in Table 1. (**b**) Cell pattern for each WL. (**c**) The timing diagram of DCP and recovery time. Each voltage bias condition is also listed in Table 1.

Table 1. Device parameters and bias condition used in the TCAD simulation.

Quantity	Value
Gate length (WL)	40 nm
Gate length (SSL, GSL)	150 nm
Gate spacing	30 nm
Gate dielectrics (O/N/O)	4/8/8 nm
Channel hole diameter (3D NAND)	80 nm
Poly-Si channel thickness (3D NAND)	10 nm
Selected WL (WL_{select})	WL8
V_{bl}	0.7 V
V_{pass}, V_{read}	6 V

We used three patterns to analyze the recovery of the channel potential caused by the DCP. The threshold voltage (V_t) pattern of WL was divided into E, P1, P2, P3, and E = −1 V, P1 = 1 V, P2 = 2 V, and P3 = 3 V. Figure 1b shows the approximate pattern used in the simulation. WL 7, 8, and 9 were set as the E pattern, while all the remaining WLs were set to patterns P1, P2, and P3, respectively. In addition, the threshold voltages of the SSL and GSL were set to 1 V for all patterns. Figure 1c shows a pulse diagram of the verify operation and recovery time, where the DCP and recovery time ranged from 0 s to 100 ms. Finally, the inversion layer model from Lombardi was used for the mobility, and the Shockley–Read–Hall (SRH) recombination model was used for the recombination in the TCAD simulation.

3. DCP Recovery Time

At the end of the verify operation, when the WL voltage decreased from V_{pass} to zero, the amounts of down-coupling voltage in WL 7, 8, and 9 were modeled as follows [15]:

$$\Delta V_{down-couple} \fallingdotseq -V_{th,neighborcells}$$

Figure 2a shows the channel potential recovery for each pattern. The channel potential, which dropped to $-V_{th,neighborcells}$, recovered over time in all patterns. In addition, channel potential recovered quickly in the early stage. However, the amount of potential recovery was not very different for each pattern. The variation of potential recovery from 0 s is shown in Figure 2b. The lower the programmed state of all adjacent WLs was, the faster the channel potential recovery in the early stages of recovery was. The amount of potential recovery was similar in all patterns after a sharp change. The amount of potential recovery after 1 µs, 5 µs, and 10 µs compared to that after 100 ms is shown in Figure 2c. P1, P2, and P3 conditions mean that adjacent WLs were programmed to P1, P2, and P3, respectively. The recovery percentage of P1 in the early stage compared to the total recovery amount was 12.4%, which was larger than that of the other patterns. The amount of potential recovery after 5 µs in the P1 pattern and after 10 µs in pattern P2 and P3 are similar. This indicates that the boosting efficiency could be increased by adjusting recovery time before the program operation according to the pattern.

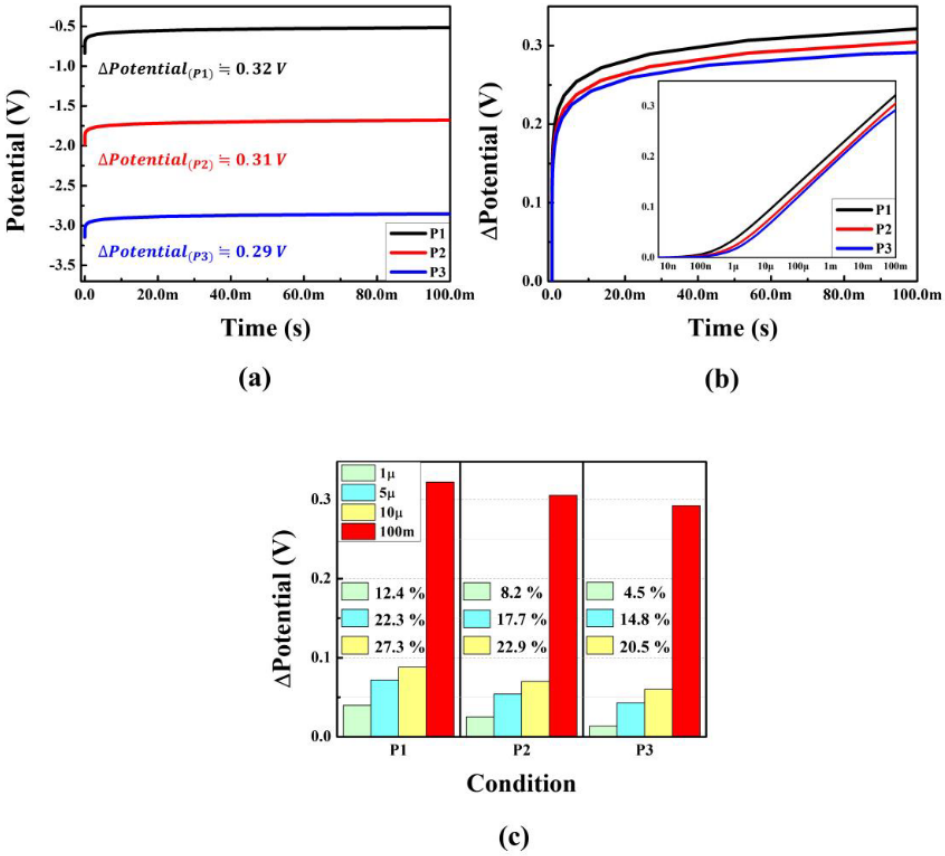

Figure 2. (**a**) Channel potential recovery in the floating channel for each pattern. (**b**) Variation of potential recovery for each pattern compared to 0 s with linear and log plots. (**c**) The amount of potential recovery after 1 µs, 5 µs, and 10 µs and the percentage of it compared to that of 100 ms.

The channel potential dropped owing to the DCP, being recovered as time elapsed when the trapped holes recombined with electrons while the holes diffused toward the center of the string [24]. In addition to electron–hole pair (EHP) recombination, a decrease of the electron concentration of the floating channel and the hole diffusion from the adjacent WLs region can cause the recovery of channel potential [25–31]. Therefore, we analyzed this phenomenon by using the EHP recombination in the floating channel and the carrier diffusion between the floating channel and the adjacent WLs region by the patterns.

The electron concentration of the floating channel at 0 s and after 5 µs are shown in Figure 3a,b, respectively. When the adjacent WLs were programmed in a low state, the

electron concentration of the floating channel was low. In addition, the electron concentration of the floating channel decreased in all patterns. Furthermore, electron diffusion from the floating channel to the adjacent WLs region occurred as a result of the electron concentration of the floating channel being higher than that of the adjacent WLs.

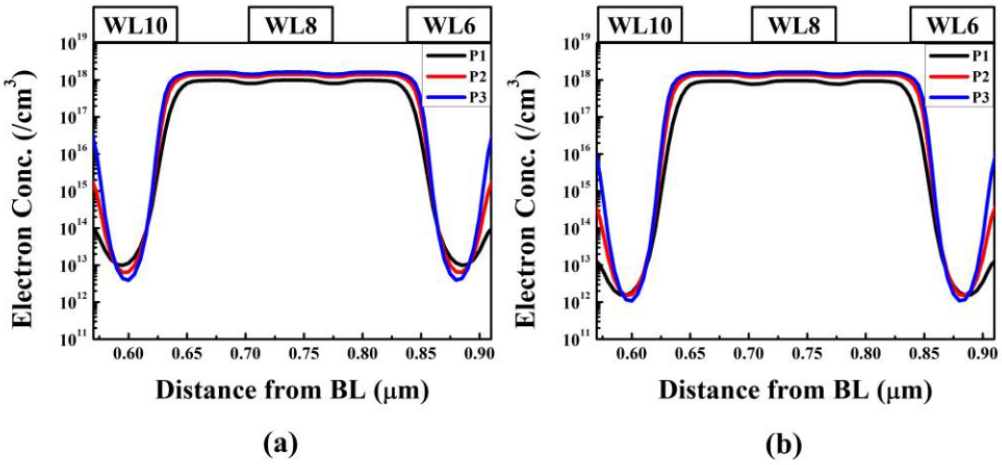

Figure 3. Electron concentration from WL6 to WL10 at (**a**) 0 s and (**b**) 5 μs.

Diffusion is a phenomenon wherein carriers move from a relatively high concentration to a low concentration [29–31]. The flow of the carrier caused by diffusion is called flux. The flux was proportional to the carrier concentration gradient. The equation for the electron diffusion flux is given as:

$$J_{n(diff.)}(x) = qD_n \frac{dn(x)}{dx}$$

where q is the quantity of electric charge, D_n is the diffusion coefficient, and $\frac{dn(x)}{dx}$ is the gradient of the electron concentration. According to the above equation, as the gradient of the concentration increases, the diffusion current increases. Therefore, if the electron diffuses a lot, the concentration of the electron is expected to decrease considerably.

As shown in Figure 4a, when the adjacent WLs were programmed in a low state, less electron diffusion occurred. The reduced electron concentration of the floating channel is shown in Figure 4b. The significant point to note is that the electron concentration variation in WL8 was similar to the recovery of the channel potential shown in Figure 2b. Therefore, this means that the channel potential was recovered owing to the decrease of the electron concentration. In terms of electron diffusion, the electron concentration should decrease slightly when the adjacent WLs are programmed in a low state. However, the electron concentration decreased significantly, even though there was less electron diffusion when the adjacent WLs were programmed in a low state. Therefore, in the early stage, this is inconsistent with the trend of quick channel potential recovery and of many variations in the electron concentration of the floating channel when the adjacent WLs are programmed to a low state as shown in Figures 2b and 4b. This indicates that electron diffusion is not a major cause of channel potential recovery.

The hole concentration of the floating channel at 0 s and after 5 μs are shown in Figure 5a,b, respectively. Although the hole concentration decreased after 5 μs in all patterns, the extent of hole concentration changed significantly in the P1 pattern. If the electron concentration and the hole concentration are high in the floating channel, EHP recombination can occur a lot. EHP recombination in the floating channel was examined, as shown in Figure 5c. When EHP recombination occurred, the hole concentration of the floating channel region decreased. Then, the electrons recombined with the holes, and the electron concentration decreased. Therefore, the channel potential recovery varied in each pattern owing to the extent of EHP recombination. EHP recombination occurred in the order of the patterns P1, P2, and P3, and the EHP recombination of the pattern P1 had the same appearance

as the hole concentration of the pattern P1. This indicates that the EHP recombination had a great impact on the extent of the channel potential recovery in the early stage.

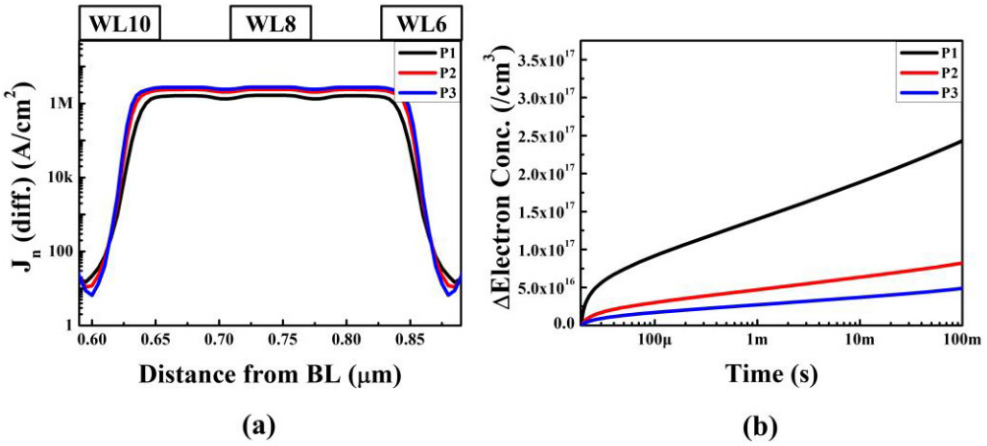

Figure 4. (**a**) Electron diffusion current from WL6 to WL10 at 0 s, which is proportional to the electron concentration at 0 s. (**b**) Variance of electron concentration in WL8 located in the floating channel.

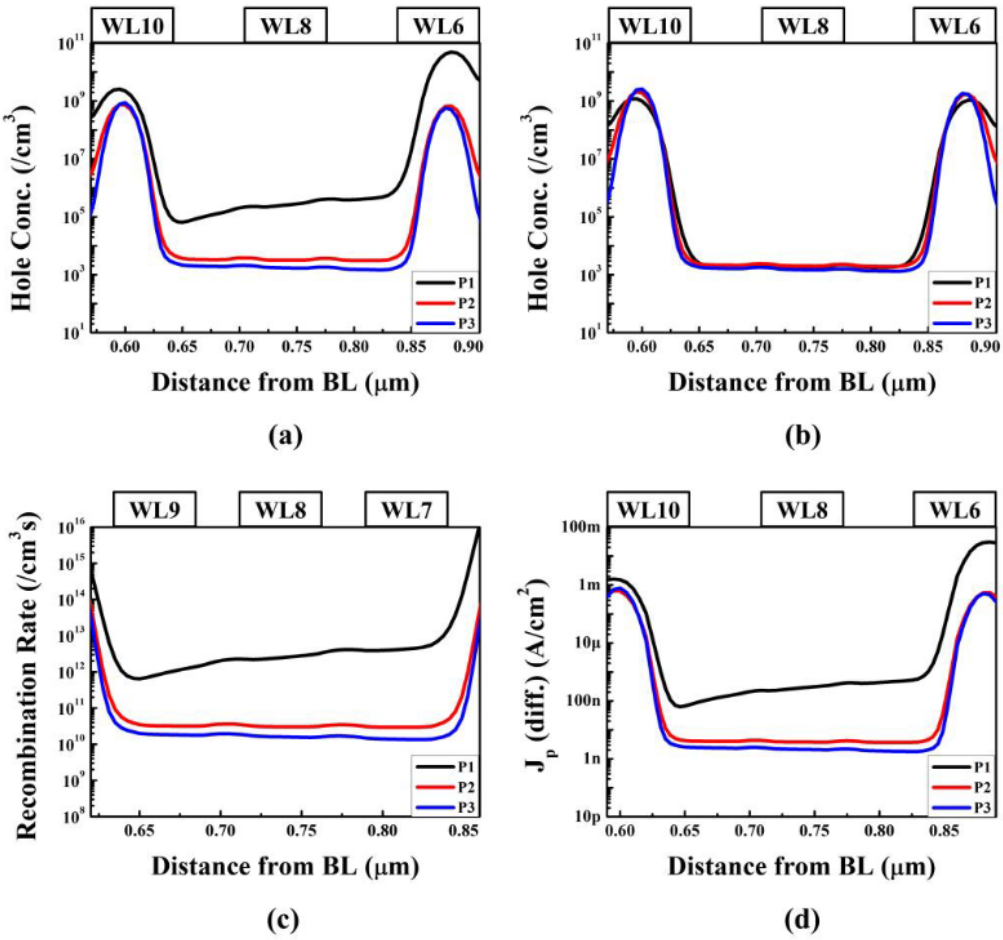

Figure 5. Hole concentration from WL6 to WL10 at (**a**) 0 s and (**b**) 5 μs. (**c**) Recombination rate in the floating channel at 0 s. (**d**) Hole diffusion current from WL6 to WL10 at 0 s, which is proportional to the hole concentration at 0 s.

The adjacent WLs region had higher hole concentrations, and no significant change was observed in the hole concentration although EHP recombination occurred in the patterns P2 and P3. In addition, although much EHP recombination occurred in the pattern

P1, over time, the hole concentration was found to be similar to that of the others. This indicates that the hole diffused from the adjacent WLs to the floating channel. The equation for the hole diffusion flux is given as:

$$J_{p(diff.)}(x) = -qD_p\frac{dp(x)}{dx}$$

where q is the quantity of electric charge, D_p is the diffusion coefficient, and $\frac{dp(x)}{dx}$ is the gradient of the hole concentration. Because the gradient of the hole concentration of the P1 pattern was higher than that of the other patterns, the hole diffusion flux increased, which was similar to when the hole concentration was at 0 s, as shown in Figure 5d. The channel potential can be recovered quickly when a hole diffusion occurs to a great extent toward to the floating channel.

Furthermore, the hole concentration of the adjacent WLs region varies owing to electrons trapped in the nitride layer. The force between the electron and the hole can affect the hole concentration of the adjacent WLs region and the hole diffusion into the floating channel. The process of hole diffusion, including the electron–hole force and EHP recombination in the floating channel, is shown in Figure 6 [32].

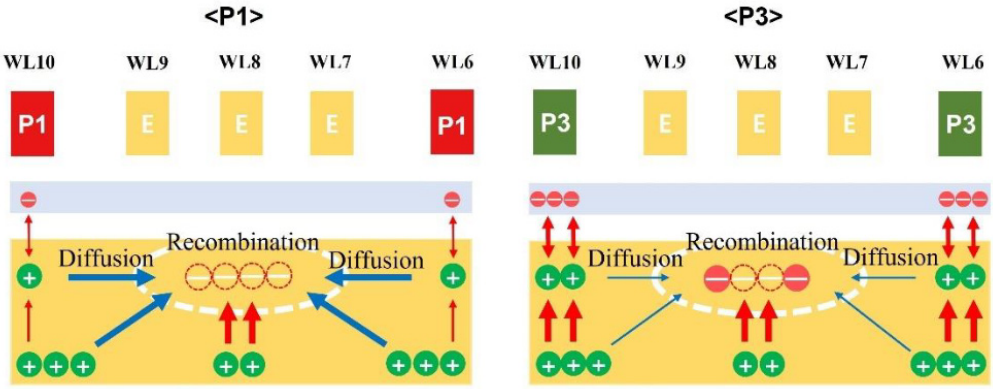

Figure 6. Schematic diagram of hole diffusion from adjacent WLs (WL6, 10) to floating channel region (WL7, 8, 9) and the electron–hole pair recombination in the floating channel region.

The electrons trapped in the nitride layer change according to the programmed state of the adjacent WLs. The trapped electrons affected the movement of the holes owing to the forces that attracted each other. Because the force was weak in the adjacent WLs programmed to P1, it did not significantly interfere with the movement of the hole, such as by causing diffusion. If the force of the trapped electron of the nitride becomes strong, such as the case of the adjacent WLs programmed to P2 and P3, it hinders the movement of the hole. Therefore, the P1 pattern recovered quickly at the beginning of the channel potential recovery because of the relatively higher occurrence of EHP recombination and hole diffusion compared to those of the other patterns.

4. Conclusions

This study analyzed the recovery of channel potential owing to the DCP in the 3D NAND flash memory. During the verify operation, the DCP caused a drop in the channel potential. The channel potential, which depended on the programmed state of the adjacent WLs, recovered differently. At the beginning of the channel potential recovery, the channel potential recovered quickly when the adjacent WLs were programmed in a low state compared to when they were in a high programmed state. Owing to electron–hole recombination, the electron concentration decreased, resulting in recovery in the floating channel. When the programmed state of the adjacent WLs was low, electron–hole recombination occurred to a greater extent, and more holes diffused into the floating channel. However, the higher the programmed state of adjacent WLs was, the greater was the channel potential drop due to the DCP, as well as the resulting slow potential recovery. If sufficient recovery time was given when the adjacent WLs were programmed in a high state, the amount of

potential recovery was similar to the recovered potential over a short period when the adjacent WLs were programmed in a low state. Therefore, to increase boosting efficiency, the recovery time should be appropriately adjusted according to the programmed state of the adjacent WLs before the program operation. Furthermore, since there are various patterns and bias conditions in addition to the conditions in this paper, an analysis of these should also be performed.

Author Contributions: Methodology, paper writing, investigation, conceptualization, G.R.; validation and investigation, H.K. and J.L.; project administration, funding acquisition, editing, and supervision, M.K. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by Institute of Information & communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (2021-0-01764-001, Charge-Storage-Memory-Based PIM Development), and in part by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2018R1A6A1A03023788), and in part by National R&D Program through the National Research Foundation of Korea (NRF) funded by Ministry of Science and ICT (2021M3F3A2A03017693).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Park, K.-T.; Nam, S.; Kim, D.; Kwak, P.; Lee, D.; Choi, Y.-H.; Choi, M.-H.; Kwak, D.-H.; Kim, D.-H.; Kim, M.-S.; et al. Three-Dimensional 128 Gb MLC Vertical nand Flash Memory with 24-WL Stacked Layers and 50 MB/s High-Speed Programming. *IEEE J. Solid-State Circuits* **2015**, *50*, 204–213. [CrossRef]
2. Cheong, W.; Yu, G.; Kim, J.; Park, J.; Song, K.-W.; Park, K.-T.; Cho, S.; Oh, H.; Lee, D.D.; Choi, J.-H.; et al. A flash memory controller for 15 µs ultra-low-latency SSD using high-speed 3D NAND flash with 3 µs read time. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 338–340. [CrossRef]
3. Choi, Y.-J.; Suh, K.-D.; Koh, Y.-N.; Park, J.-W.; Lee, K.-J.; Cho, Y.-J.; Suh, B.-H. A high speed programming scheme for multi-level NAND flash memory. In Proceedings of the 1996 Symposium on VLSI Circuits, Digest of Technical Papers, Honolulu, HI, USA, 13–15 June 1996. [CrossRef]
4. Takeuchi, K.; Tanaka, T.; Tanzawa, T. A multipage cell architecture for high-speed programming multilevel NAND flash memories. *IEEE J. Solid-State Circuits* **1998**, *33*, 1228–1238. [CrossRef]
5. Takeuchi, K. Novel Co-Design of NAND Flash Memory and NAND Flash Controller Circuits for Sub-30 nm Low-Power High-Speed Solid-State Drives (SSD). *IEEE J. Solid-State Circuits* **2009**, *44*, 1227–1234. [CrossRef]
6. Kim, M.-K.; Kim, I.-J.; Lee, J.-S. CMOS-compatible ferroelectric NAND flash memory for high-density, low-power, and high-speed three-dimensional memory. *Sci. Adv.* **2021**, *7*, eabe1341. [CrossRef]
7. Park, C.; Talawar, P.; Won, D.; Jung, M.; Im, J.; Kim, S.; Choi, Y. A High Performance Controller for NAND Flash-based Solid State Disk (NSSD). In Proceedings of the 2006 21st IEEE Non-Volatile Semiconductor Memory Workshop, Monterey, CA, USA, 12–16 February 2006. [CrossRef]
8. Kang, M.; Hahn, W.; Park, I.H.; Song, Y.; Lee, H.; Choi, K.; Lim, Y.; Joe, S.-M.; Chae, D.H.; Shin, H. A Compact Model for Channel Coupling in Sub-30 nm NAND Flash Memory Device. *Jpn. J. Appl. Phys.* **2011**, *50*, 100204. [CrossRef]
9. Kang, M.; Park, I.H.; Chang, I.J.; Lee, K.; Seo, S.; Park, B.-G.; Shin, H. An Accurate Compact Model Considering Direct-Channel Interference of Adjacent Cells in Sub-30-nm nand Flash Technologies. *IEEE Electron Device Lett.* **2012**, *33*, 1114–1116. [CrossRef]
10. Kang, M.; Lee, K.; Chae, D.H.; Park, B.-G.; Shin, H. The Compact Modeling of Channel Potential in Sub-30-nm NAND Flash Cell String. *IEEE Electron Device Lett.* **2012**, *33*, 321–323. [CrossRef]
11. Park, M.; Kim, K.; Park, J.-H.; Choi, J.-H. Direct Field Effect of Neighboring Cell Transistor on Cell-to-Cell Interference of nand Flash Cell Arrays. *IEEE Electron Device Lett.* **2008**, *30*, 174–177. [CrossRef]
12. Kim, Y.; Yun, J.-G.; Park, S.H.; Kim, W.; Seo, J.Y.; Kang, M.; Ryoo, K.-C.; Oh, J.-H.; Lee, J.-H.; Shin, H.; et al. Three-Dimensional nand Flash Architecture Design Based on Single-Crystalline STacked ARray. *IEEE Trans. Electron Devices* **2011**, *59*, 35–45. [CrossRef]
13. Jeong, W.; Im, J.-W.; Kim, D.-H.; Nam, S.-W.; Shim, D.-K.; Choi, M.-H.; Yoon, H.-J.; Kim, D.-H.; Kim, Y.-S.; Park, H.-W.; et al. A 128 Gb 3b/cell V-NAND Flash Memory with 1 Gb/s I/O Rate. *IEEE J. Solid-State Circuits* **2015**, *51*, 204–212. [CrossRef]
14. Kim, Y.; Kang, M.; Park, S.H.; Park, B.-G. Three-Dimensional NAND Flash Memory Based on Single-Crystalline Channel Stacked Array. *IEEE Electron Device Lett.* **2013**, *34*, 990–992. [CrossRef]
15. Kim, Y.; Kang, M. Down-Coupling Phenomenon of Floating Channel in 3D NAND Flash Memory. *IEEE Electron Device Lett.* **2016**, *37*, 1566–1569. [CrossRef]

16. Kang, M.; Kim, Y. Natural Local Self-Boosting Effect in 3D NAND Flash Memory. *IEEE Electron Device Lett.* **2017**, *38*, 1236–1239. [CrossRef]
17. Shim, K.-S.; Choi, E.-S.; Jung, S.-W.; Kim, S.-H.; Yoo, H.-S.; Jeon, K.-S.; Joo, H.-S.; Oh, J.-S.; Jang, Y.-S.; Park, K.-J.; et al. Inherent Issues and Challenges of Program Disturbance of 3D NAND Flash Cell. In Proceedings of the 2012 4th IEEE International Memory Workshop, Milan, Italy, 20–23 May 2012; pp. 1–4. [CrossRef]
18. Zhang, Y.; Jin, L.; Jiang, D.; Zou, X.; Liu, H.; Huo, Z. A Novel Read Scheme for Read Disturbance Suppression in 3D NAND Flash Memory. *IEEE Electron Device Lett.* **2017**, *38*, 1669–1672. [CrossRef]
19. Lee, J.-D.; Lee, C.-K.; Lee, M.-W.; Kim, H.-S.; Park, K.-C.; Lee, W.-S. A New Programming Disturbance Phenomenon in NAND Flash Memory By Source/Drain Hot-Electrons Generated By GIDL Current. In Proceedings of the 2006 21st IEEE Non-Volatile Semiconductor Memory Workshop, Monterey, CA, USA, 12–16 February 2006; pp. 31–33. [CrossRef]
20. Choe, B.-I.; Lee, J.-K.; Park, B.-G.; Lee, J.-H. Suppression of Read Disturb Fail Caused by Boosting Hot Carrier Injection Effect for 3-D Stack NAND Flash Memories. *IEEE Electron Device Lett.* **2013**, *35*, 42–44. [CrossRef]
21. Jeong, Y.; Ham, I.; Han, S.; Kang, M. Optimal dummy word line condition to suppress hot carrier injection phenomenon due to the natural local self-boosting effect in 3D NAND flash memory. *Jpn. J. Appl. Phys.* **2020**, *59*, SGGB17. [CrossRef]
22. Han, S.; Jeong, Y.; Jhon, H.; Kang, M. Investigation of Inhibited Channel Potential of 3D NAND Flash Memory According to Word-Line Location. *Electronics* **2020**, *9*, 268. [CrossRef]
23. Atlas User's Manual, Silvaco Version. 5.19.20. Available online: http://www.silvaco.com/products/tcad/device_simulation/atlas/atlas.html (accessed on 3 February 2020).
24. Giulianini, M.; Malavena, G.; Compagnoni, C.M.; Spinelli, A.S. Time Dynamics of the Down-Coupling Phenomenon in 3-D NAND Strings. *IEEE Trans. Electron Devices* **2022**, *69*, 6757–6762. [CrossRef]
25. Cellere, G.; Paccagnella, A.; Visconti, A.; Bonanomi, M.; Beltrami, S. Single Event Effects in NAND Flash Memory Arrays. *IEEE Trans. Nucl. Sci.* **2006**, *53*, 1813–1818. [CrossRef]
26. Sah, C.-T.; Shockley, W. Electron-Hole Recombination Statistics in Semiconductors through Flaws with Many Charge Conditions. *Phys. Rev.* **1958**, *109*, 1103–1115. [CrossRef]
27. O'Neil, M.; Marohn, J.; McLendon, G. Dynamics of electron-hole pair recombination in semiconductor clusters. *J. Phys. Chem.* **1990**, *94*, 4356–4363. [CrossRef]
28. Moser, J.-E.; Grätzel, M.; Gallay, R. Inhibition of Electron-Hole Recombination in Substitutionally Doped Colloidal Semiconductor Crystallites. *Helvetica Chim. Acta* **1987**, *70*, 1596–1604. [CrossRef]
29. Oh, D.; Lee, B.; Kwon, E.; Kim, S.; Cho, G.; Park, S.; Lee, S.; Hong, S. TCAD Simulation of Data Retention Characteristics of Charge Trap Device for 3-D NAND Flash Memory. In Proceedings of the 2015 IEEE International Memory Workshop (IMW), Monterey, CA, USA, 17–20 May 2015; pp. 1–4. [CrossRef]
30. Goodman, A.M. A Method for the Measurement of Short Minority Carrier Diffusion Lengths in Semiconductors. *J. Appl. Phys.* **1961**, *32*, 2550–2552. [CrossRef]
31. Lun, Z.; Liu, S.; He, Y.; Hou, Y.; Zhao, K.; Du, G.; Liu, X.; Wang, Y. Investigation of retention behavior for 3D charge trapping NAND flash memory by 2D self-consistent simulation. In Proceedings of the 2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Yokohama, Japan, 9–11 September 2014; pp. 141–144. [CrossRef]
32. Kim, H.; Kang, M. "Analysis of DCP and NLSB Recovery Time in 3D NAND Flash Memory", knut Dcollection, February 2023. Available online: http://www.dcollection.net/handler/chains/200000667859 (accessed on 3 February 2020).