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A New Control Scheme for the Buck Converter

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Abstract: In this paper, a new control scheme for buck converters was proposed. The buck converter utilizes the dual control loop to improve transient response and has the constant switching frequency. The control scheme is mainly as follows: (a) The switch-ON time is regulated by the constant frequency mechanism. (b) The switch-OFF time is regulated by the output voltage. The spec/features of the proposed converter are listed as: (1) The buck converter has an output of 1.0–2.5 V for the input of 3.0–3.6 V. The load current ranges from 100 mA to 500 mA. (2) The actual current sensor is not required. (3) The simulation results show that the recovery time is less than 1.6 µs during load changes. (4) The variation in switching frequency is smaller than 1.05% over the output range of 1.0–2.5 V. (5) This circuit can be fabricated in future by UMC 0.18 µm 1P6M CMOS processes. This paper depicts the control scheme, theoretical analysis, and implementation.

Keywords: switched-capacitor (SC) converters; switched-inductor (SL) converters; current mode control (CMC); voltage mode control (VMC); adaptive ON time (AOT); constant ON time (COT); pulse width modulation (PWM); peak current mode (PCM); average current mode (ACM)

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1. Introduction

In recent years, portable devices have become more widespread and even diverse, such as cell phones, laptops, and tablets. All these devices require a power converter, for example, artificial intelligence (AI), Internet of Things (IoT) devices, etc. [1–3]. In order to extend the standby time, especially in cell phones, the efficiency of the power converter is crucial. The dynamic response of power converters is more and more important.

Power converters can be broadly classified as switched-capacitor (SC) converters [4,5] and switched-inductor (SL) converters [6–8]. The SC converters mainly consist of switches, control circuits, and capacitors. Different from the SC converter, the SL converter uses the inductor rather than the capacitor for power conversion. From the application viewpoint, low power converters usually use SC architectures. On the contrary, SL converters are available in applications that range from a fraction of a watt to a few hundred watts [5]. The advantage of the SC converter is that the capacitors have a higher power density and are easier to integrate than the inductors [9]. However, voltage regulation problems can be present in some voltage conversion ratios [5]. In contrast, the SL converters are popular in power conversion because of their application range, high reliability, design flexibility, and low cost.

The common terms used in buck converters include power-conversion topologies, pulse width modulation, discontinuous-conduction mode, and continuous-conduction mode. Firstly, we briefly introduce these common terms, and then present the recent research situation. The basic buck conversion topology is very simple; it only uses the switches (S_1, S_2) and an inductor (L) for power conversion (Figure 1). In power conversion, the key point is the control method, which controls the switches to turn ON or OFF. In

general, common control methods include: pulse width modulation (PWM) and peak current mode (PCM).

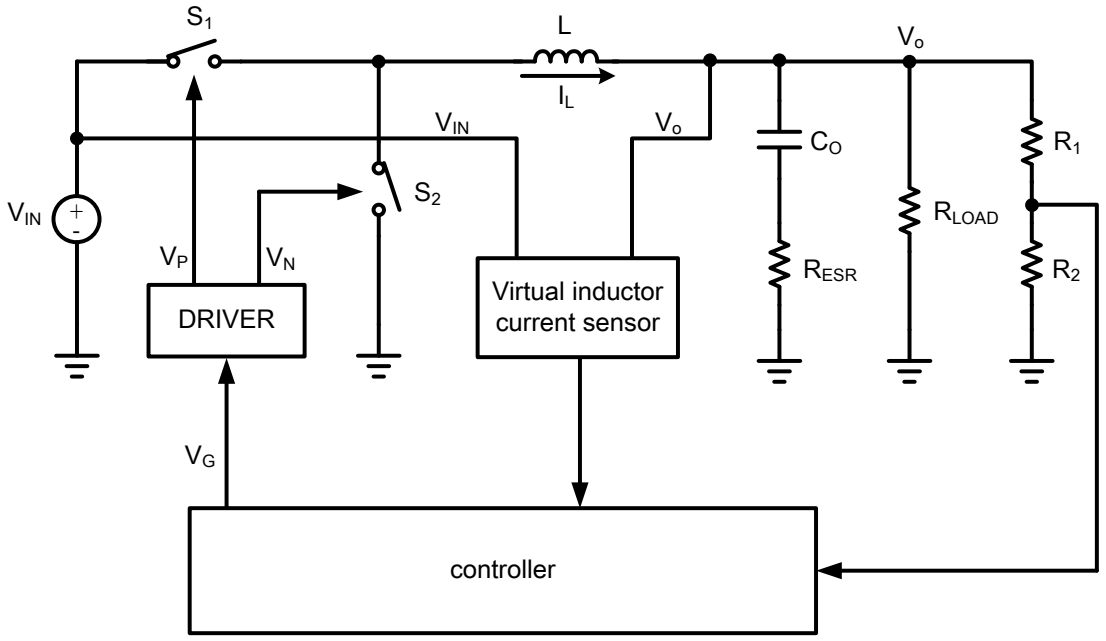


Figure 1. Buck topology with a virtual inductor current sensor.

For PWM, the feature is to fix switching frequency, and then change the pulse width to control the switches (S_1, S_2 in Figure 1). However, PCM usually has a variable switching frequency, and the switches ON/OFF will depend on the inductor current. In addition, whether for PWM or PCM, if the system is in steady state, when the switch (S_1) starts to turn ON (Figure 1), the inductor current is zero. We refer to this as discontinuous-conduction mode. On the contrary, when the switch (S_1) starts to turn ON, and the inductor current is not zero, we refer to this as continuous-conduction mode. In addition, the feedback stability is also an important topic that will be discussed in later sections.

As an overview of the SL converters, the control modes can be classified into voltage mode control (VMC) [10] and current mode control (CMC) [11–14]. In general, since CMC has more feedback paths than VMC, CMC should perform better than VMC in regard to the dynamic response and the voltage regulation. This is the reason why most current control schemes are based on CMC. In the conventional CMC, the control scheme requires a current sensor to get information about the inductor current. Therefore, how to sense inductor current is an important issue and is discussed in much of the literature. The related research has been summarized and analyzed in [15]. Several control modes based on CMC have been revealed to regulate the output voltage, such as: constant on time (COT), average current mode (ACM), constant off time (CFT), peak current mode, and adaptive on time (AOT) [16–19].

The author of [15] uses a virtual inductor current sensor to obtain the inductor current traces instead of the real current sensor (Figure 1). The proposed scheme in [15] can greatly reduce hardware effort. However, it still needs the virtual inductor current sensor. The authors of [20,21] propose a control scheme that does not require the current sensor but only senses the output voltage. In [20], the switch-ON time is regulated by the voltage difference between the input and output voltages (Figure 2). In [21], the switch-ON time (T_{ON}) of S_1 is adaptive and regulated by the output voltage (Figure 3). Different from [20] and [21], in this paper, the switch-ON time is regulated by the constant switching frequency mechanism. In contrast to [22], the constant switching frequency mechanism consists of only a phase frequency detector, a charge pump, and a low pass filter.

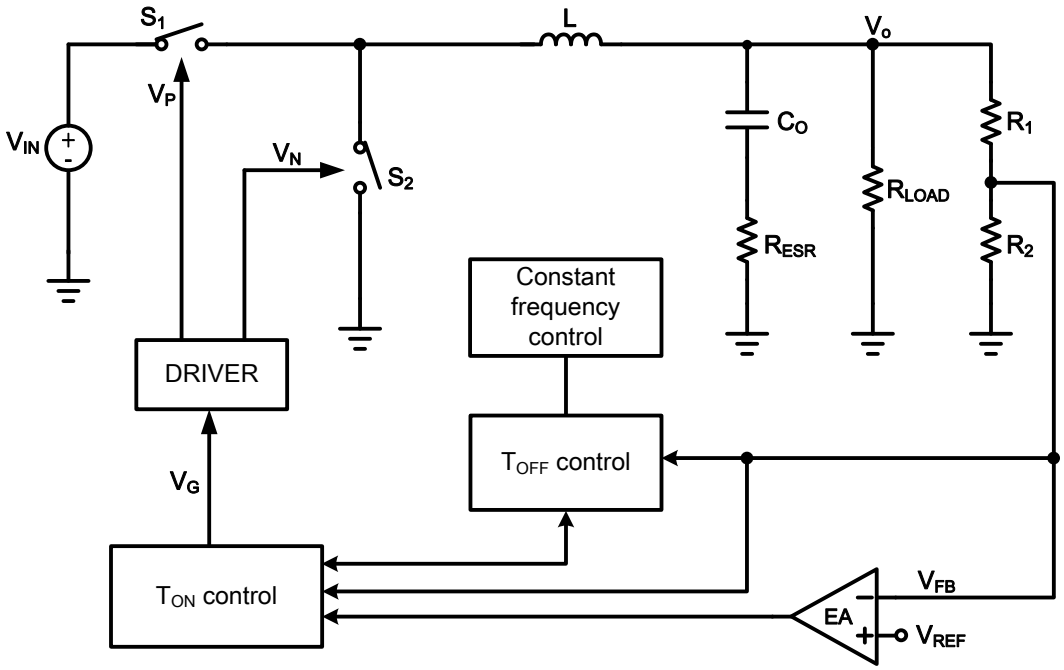


Figure 2. Dual loops control topology for buck converters.

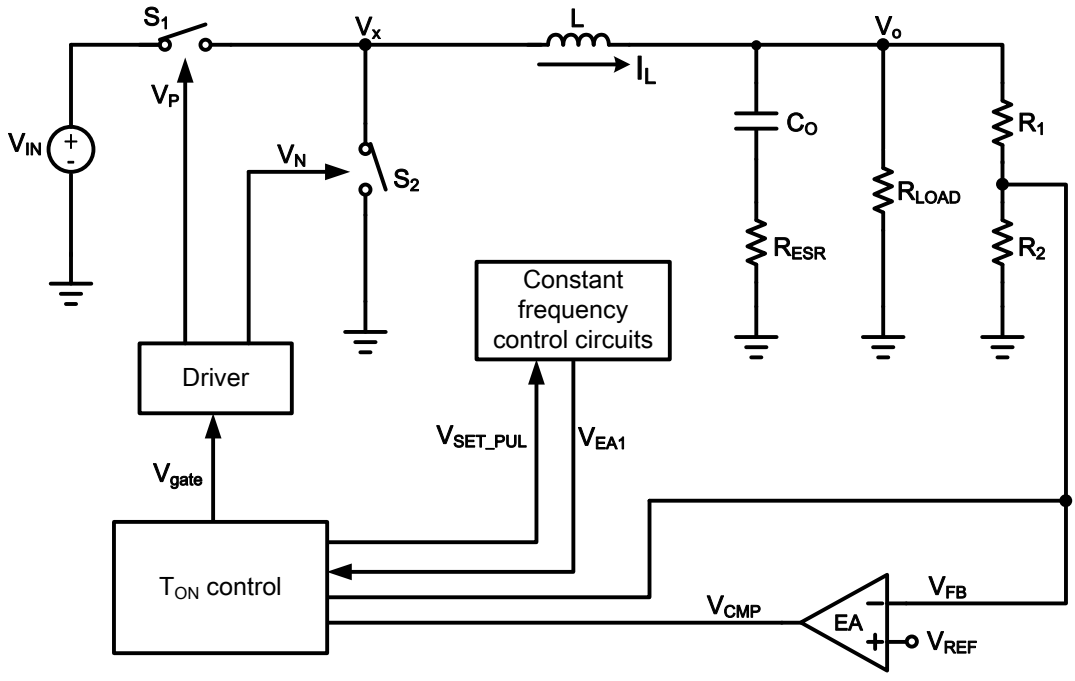


Figure 3. BUCK topology without inductor current sensor.

In this paper, a new SL buck converter with constant switching frequency will be proposed. The importance of the topic and the practical application that the new control scheme can be listed as (a) the practical application of the scheme is suitable for portable devices; (b) the contribution of this solution is that it effectively reduces hardware effort and is suitable for mass production; (c) this scheme provides an alternative solution for buck control in industry applications.

In addition, the merits of the new control scheme are (a) the constant switching frequency, alleviating the EMI issue in applications; (b) the actual current sensor is not required, which makes the overall circuit design simple. In this paper, we have made some

changes in the conventional design where we only detect the voltage difference between the output and the input to obtain the variation of the inductor current. In other words, these differences from conventional designs make the overall circuitry simpler. The organization of this paper is as follows: Section 2 presents the proposed scheme and implementation. Section 3 introduces the mathematical modeling and components selection. Section 4 shows the simulation results of SIMPLIS. Finally, the conclusion is given in Section 5.

2. Proposed Control Methodology

2.1. Scheme and Implementation

Figure 4 shows the proposed scheme. In Figure 4, we can find that (a) the actual current sensor is not needed in this scheme; (b) the constant frequency mechanism controls the switch-ON time; (c) the switch-OFF time is regulated by the error amplifier (EA). The error amplifier would make V_{FB} and V_{REF} equal. In this paper, the ON time of the S_1 is labelled as T_{ON}, and the OFF time of the S_1 is labelled as T_{OFF}.

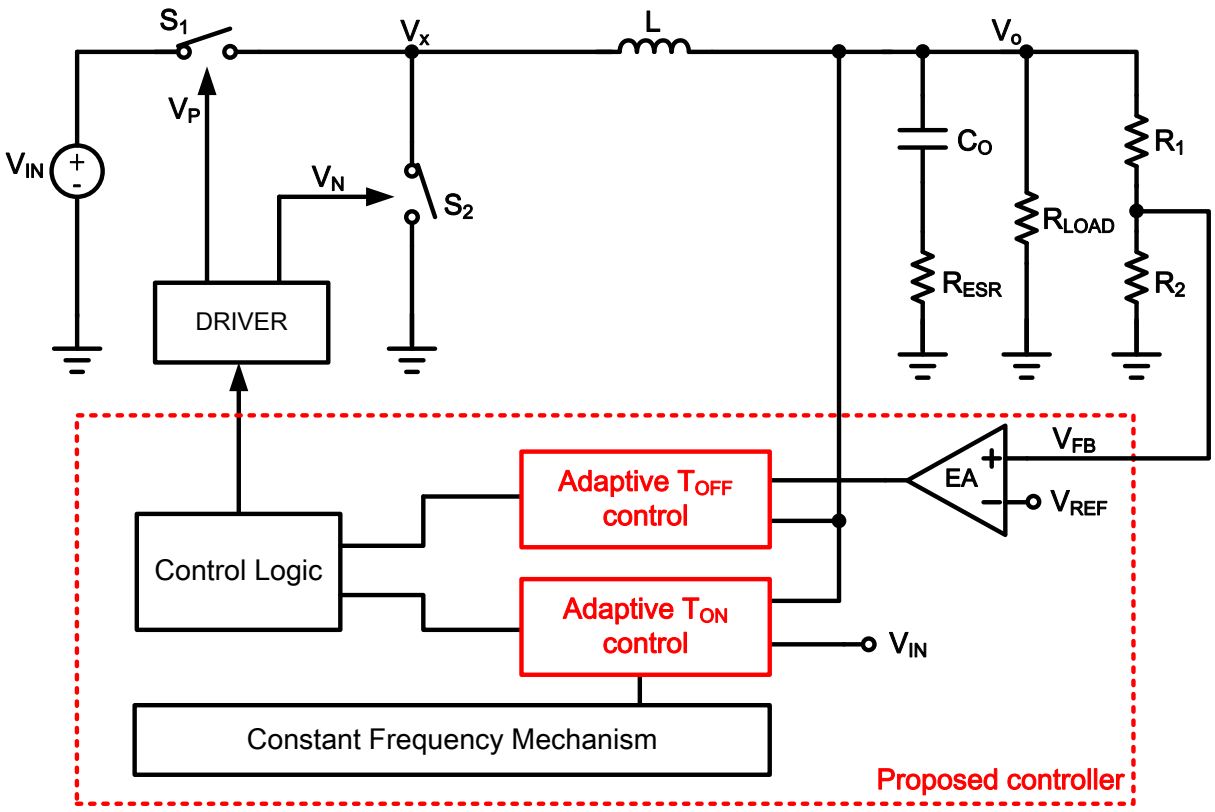


Figure 4. Proposed scheme.

Figure 5 shows the implementation of the proposed scheme. The advantages of Figure 5 are listed as: (a) The proposed controller consists of only common components such as flip-flops, comparators, and error amplifier. No special process is required for fabrication; (b) The architecture of the adaptive T_{ON}/T_{OFF} control is simple, which greatly reduces the hardware effort; (c) Different from [22], the constant frequency mechanism can be effectively used to keep the switching frequency constant.

2.2. Operation Principle

The detailed operation of the converter is listed as follows:

1. When the switch S_1 is ON, and the other switch S_2 is OFF.
2. The inductor (L) is in the charging state, and the ON-time of S_1 is controlled by the adaptive T_{ON} control block. In the adaptive T_{ON} control block, the ON-time is

decided by V_{ramp} and V_{CTR}. The V_{ramp} is the function of V_{IN} and V_o, which replaces the conventional method that requires a current sensor to sense inductor current.

3. When the switch S_1 is OFF, and the other switch S_2 is ON.
4. The inductor (L) is in the discharging state, and the OFF-time of S_1 is controlled by the adaptive T_{OFF} control block. In the adaptive T_{OFF} control block, the OFF-time is decided by V_{ramp2} and V_{CMP}, both of which are the functions of the V_o. Since the V_o controls the OFF-time through two paths, the control scheme has good transient response.
5. The operation of the constant frequency mechanism will make the REF_CLK and the FB_CLK equal. The REF_CLK can be set by the user. In this paper, the REF_CLK is set to 1 MHz.
6. The states of the switches S_1 and S_2 are complementary and non-overlapping. The key waveforms in Figure 5 are drawn in Figure 6.
7. In Figure 6, the I_L is the inductor current. In the steady state, we can find that the I_L is triangle wave, and the mean is I_{avg}. When the S_1 is ON (i.e., V_G is high), the I_L is linearly rising and the inductor (L) is in the charging phase. On the contrary, the S_1 is OFF (i.e., V_G is low), the I_L is linearly falling, and the inductor is in the discharging phase.

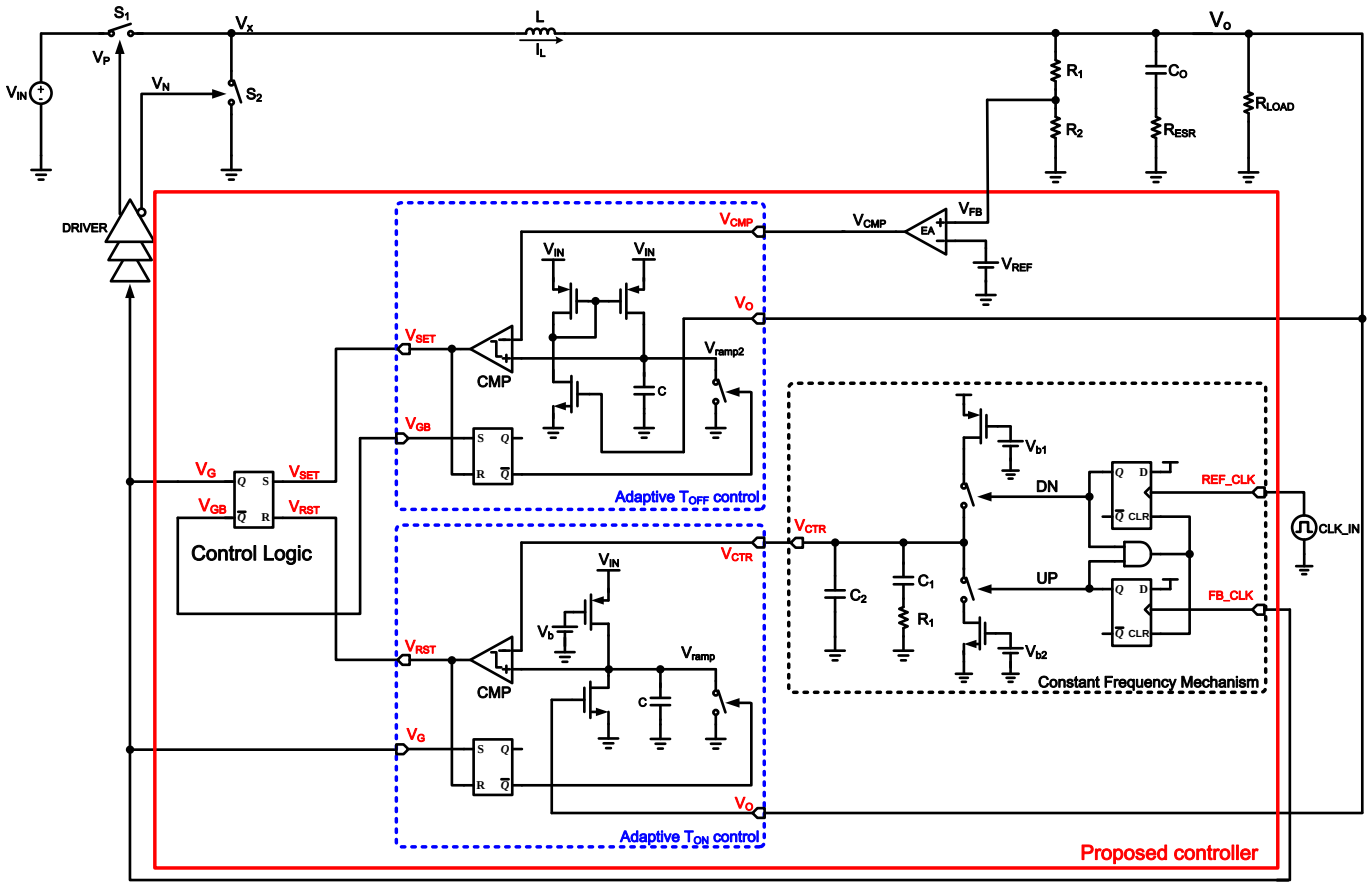


Figure 5. Circuit implementation of the proposed converter.

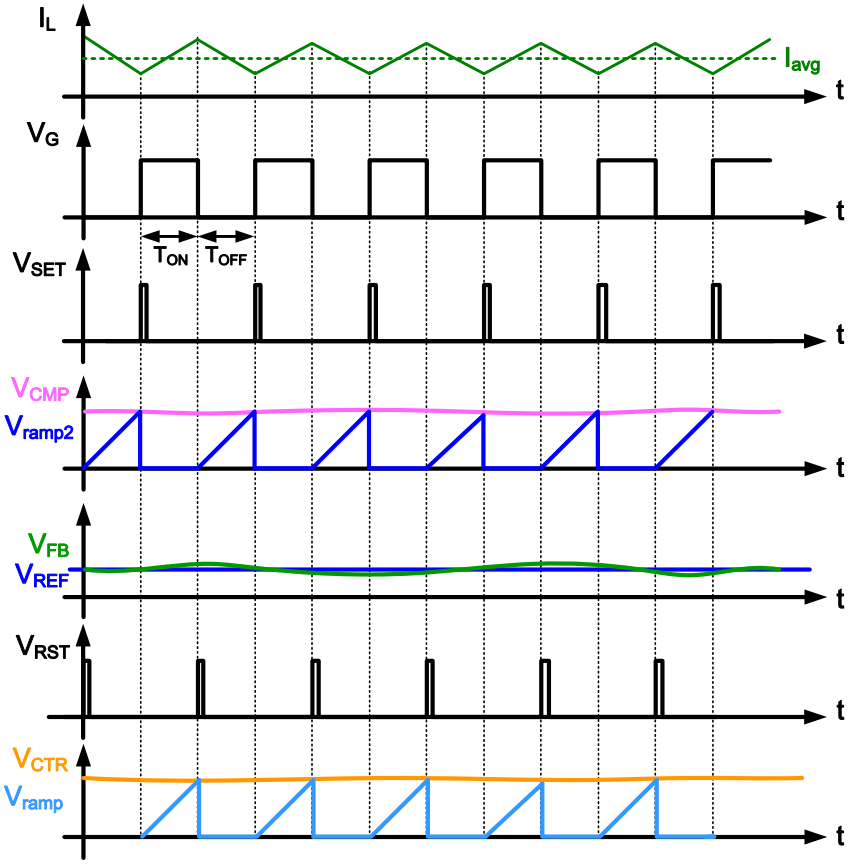


Figure 6. Key waveforms of Figure 5.

3. Mathematical Modeling and Components Selection

3.1. Mathematical Modeling

In order to guarantee the stability of the system, the derivation of the open-loop transfer function is necessary. The literature about the mathematical modeling is presented in [15]. Details of the design procedure can be found in [15]. Figure 7 shows the open-loop structure of Figure 4. Similarly to [20], Equation (1) can be used to represent the open-loop transfer function of Figure 7. The $G_p(s)$ expression in Equation (2) represents the buck converter. The compensation network $A(s)$ with the error amplifier (EA) is represented by Equation (3).

$$\mathrm{T(s)} = \frac{V_o(s)}{V_i(s)} = G_P(s) \cdot A(s) \tag{1}$$

$$G_P(s) = \frac{V_{FB}(s)}{V_i(s)} = \frac{1}{R_i} \cdot \frac{1}{1 + \frac{s}{Q \cdot \omega} + \frac{s^2}{\omega^2}} \cdot \frac{R_{LOAD}(R_{ESR}C_o s + 1)}{(R_{LOAD} + R_{ESR})C_o s + 1} \tag{2}$$

$$A(s) = \frac{V_o(s)}{V_{FB}(s)} = g_m \cdot R_o \cdot \frac{\left(1 + \frac{s}{w_z}\right)}{\left(1 + \frac{s}{w_p}\right)} \tag{3}$$

$$w_z = \frac{1}{R_3 \cdot C_1}, w_p = \frac{1}{R_o \cdot C_1} \tag{4}$$

In Equation (2), $\omega = \frac{\pi}{T_{on}}$ and $Q = \frac{2}{\pi}$, R_i is the gain of the $\mathrm{T_{OFF}}$ ramp generator.

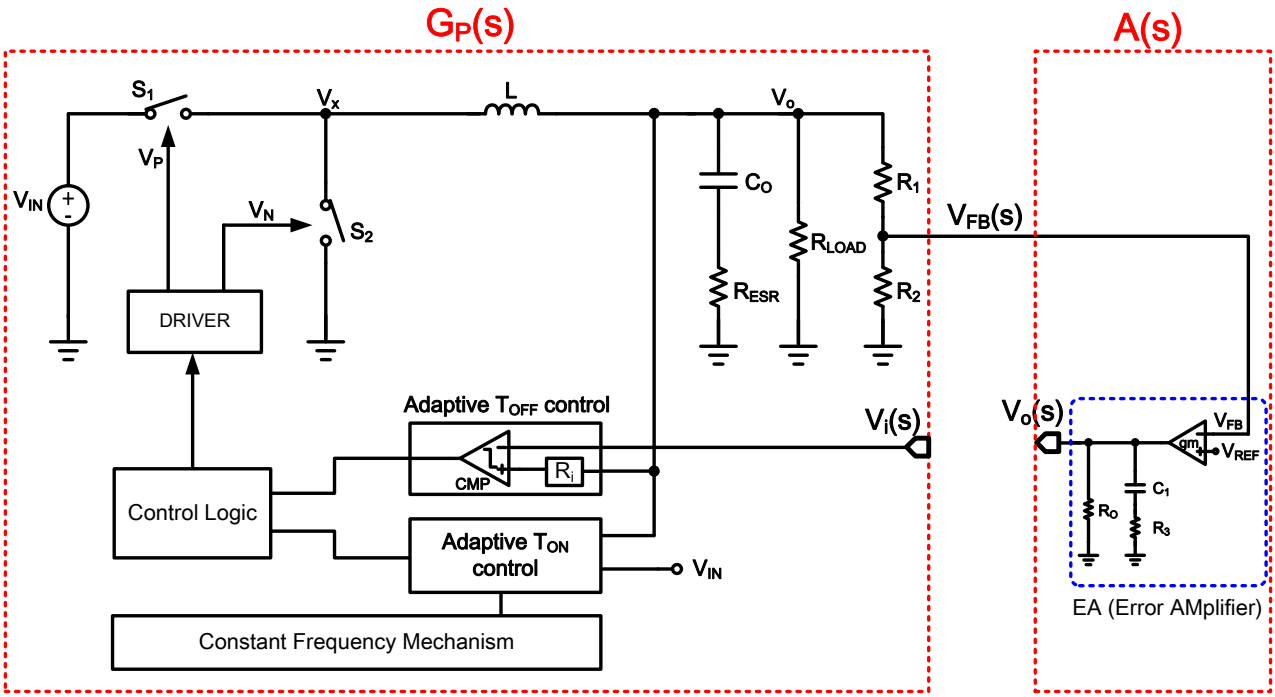


Figure 7. Open loop structure of the proposed converter.

3.2. Components Selection

Based on the above mathematical model, we can find out the relevant parameters with the mathematical tools "MathCAD" [15,20]. Table 1 lists the components/parameters of the scheme. (Figure 7)

Table 1. Component parameters.

Components	Value	Unit
C_o	10	μF
L	4.7	μH
R_{ESR}	5	mΩ
R_{LOAD}	3.6/18 (for load switching)	Ω
R_1	10	MΩ
R_2	10	MΩ
R_o	1	MΩ
R_3	400	kΩ
C_1	300	pF

3.3. Implementation Processes

The future possible implementation processes can be explained as follows: (a) using UMC 0.18 μm 1P6M CMOS processes for fabrication; (b) the switches (S_1, S_2) are integrated in the chip; (c) UMC 0.18 μm 1P6M CMOS processes provide 1.8 V and 3.3 V MOS devices for selection. For simplicity, the whole circuit uses the 3.3 V MOS devices for implementation. In the future, a combination design with 3.3 V/1.8 V MOS devices can be considered.

4. Simulation Results

4.1. SIMPLIS Schematic

The proposed converter was verified by SIMPLIS. Figure 8 shows its schematic.

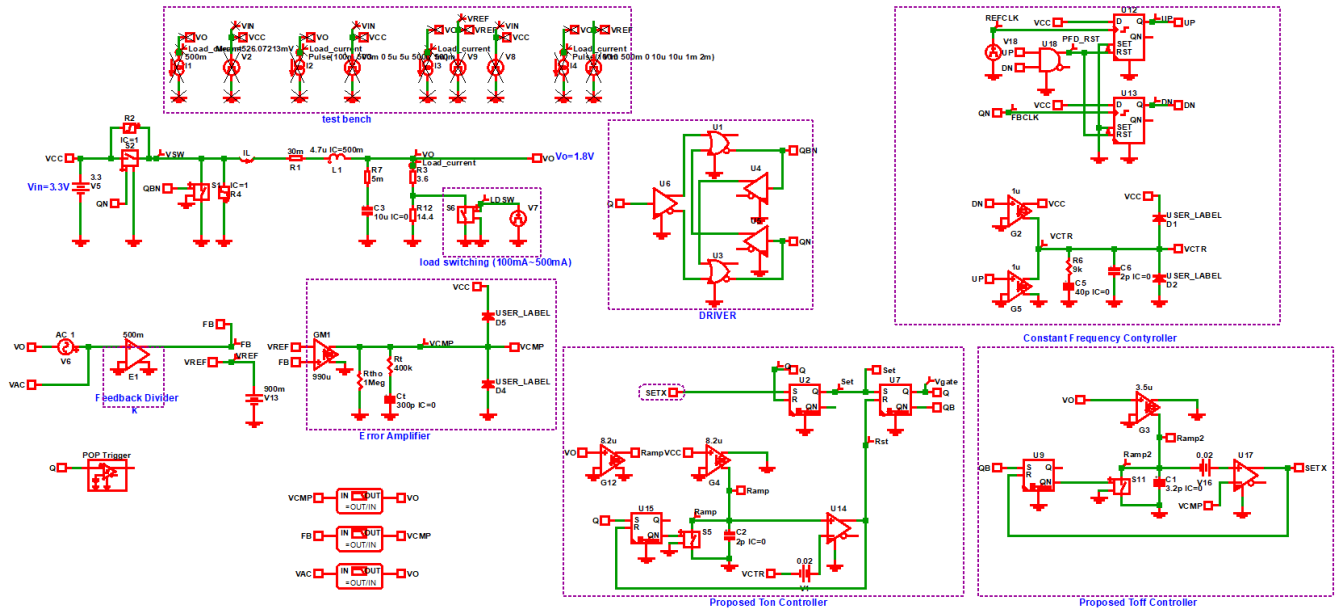


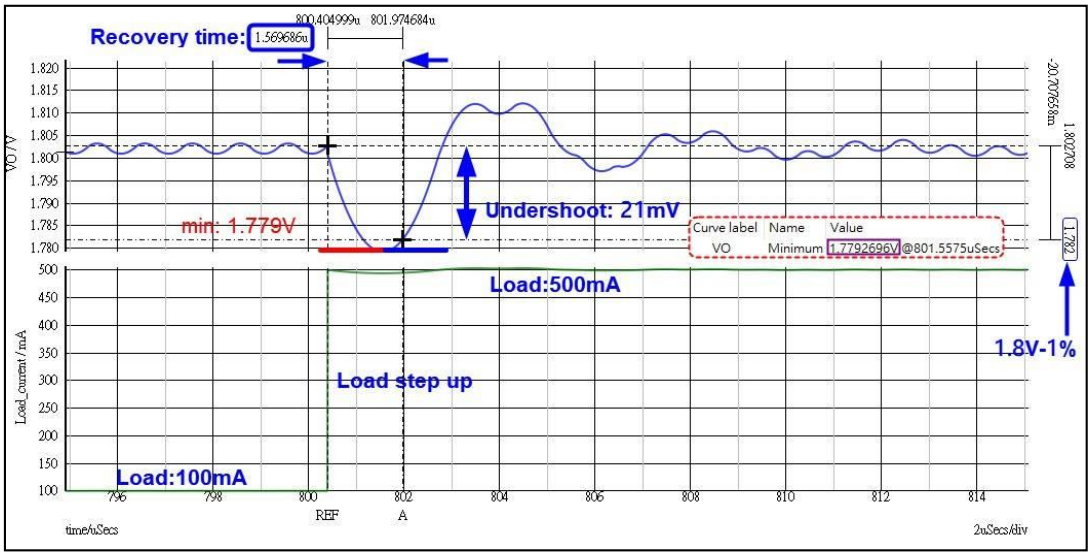
Figure 8. SIMPLIS schematic for the proposed converter.

4.2. Transient Response

The same measurement conditions as in [20,21] are given below. (a) The load current transition is between 0.1 A and 0.5 A at 3.3 V/1.8 V input/output voltage. (b) The recovery time is defined as within 1% of the 1.8 V output voltage at load transition.

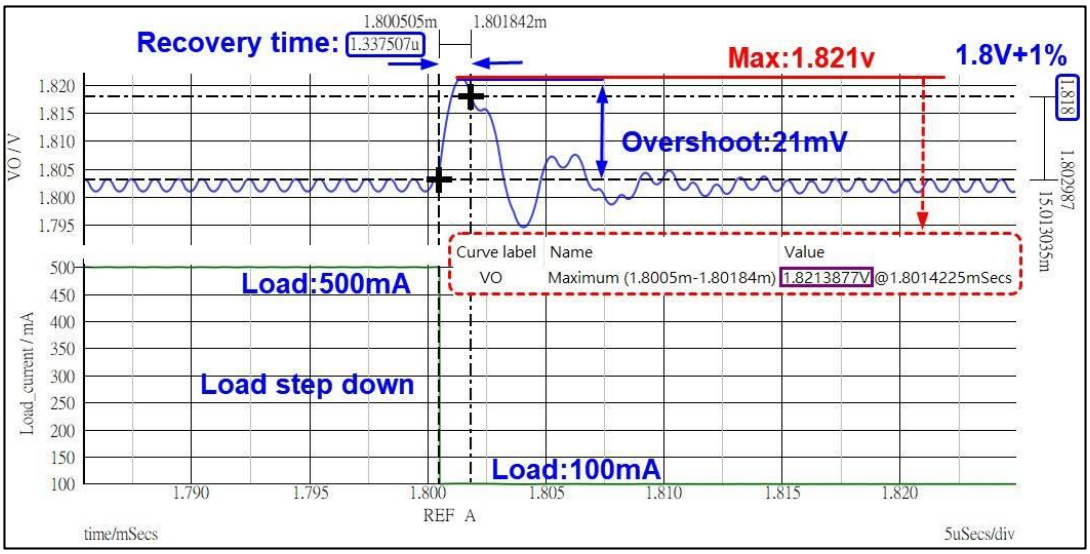
Figure 9 shows the load transient response. From Figure 9, the transient performance is as follows: (a) The recover times for the step-up/step-down load current transition are 1.57 µs and 1.34 µs, respectively. (b) The overshoot/undershoot voltages are 21 mV/21 mV, both within the range of 21 mV.

Figure 10 shows that the converter can operate in V_{in} range of 3.0–3.6 V, while output can be set in the range of 1.0–2.5 V. In V_{in} range of 3.0–3.6 V, the maximum ripple voltage for V_o is 2.2 mV, which occurred at V_{in} of 3.6 V and V_o of 2.5 V.



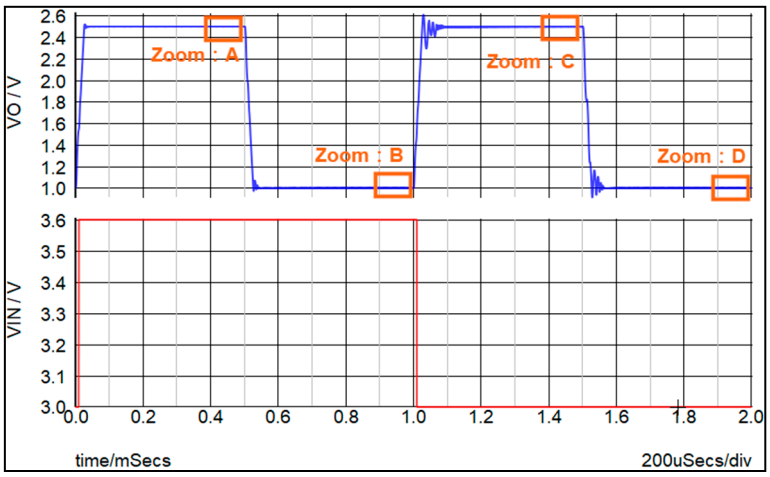
(**a**) Light load to heavy load

Figure 9. *Cont.*

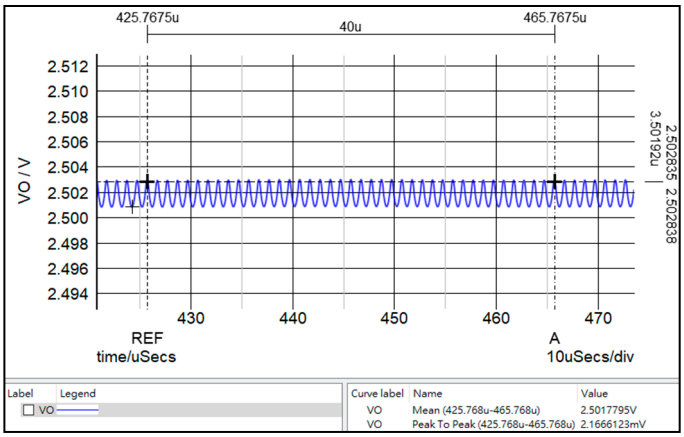


(**b**) Heavy load to light load

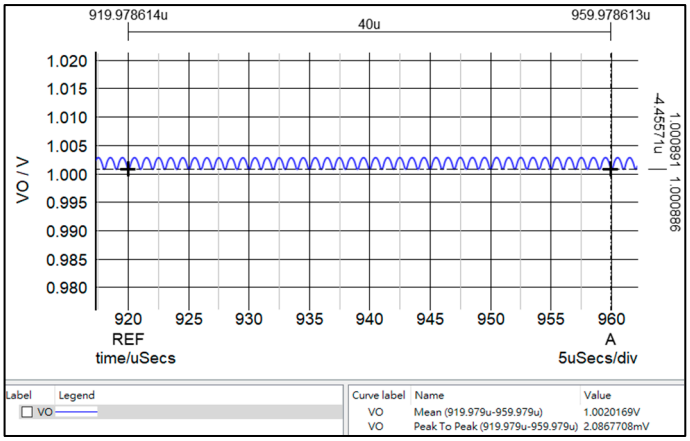
Figure 9. Recovery times for load current transition (100–500 mA).



(**a**) Output performance for input margin operation

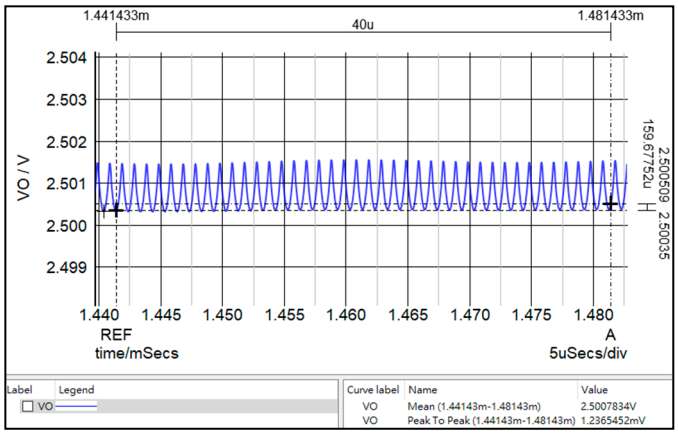


(**b**) Zone A of (a)

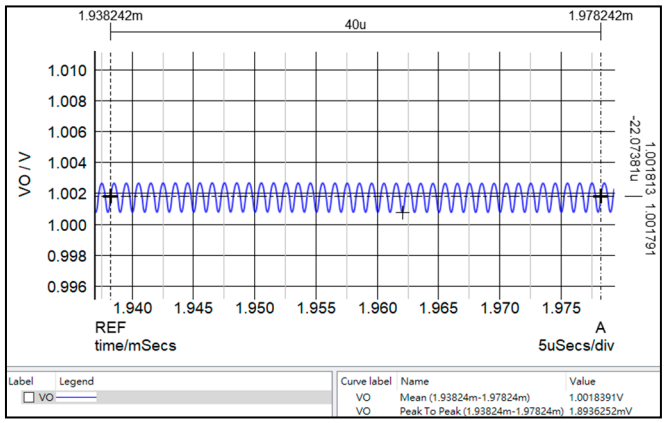


(**c**) Zone B of (a)

Figure 10. *Cont.*



(**d**) Zone C of (a)



(**e**) Zone D of (a)

Figure 10. Performance of the converter for V_{in} range of 3.0–3.6 V.

4.3. Load Regulation

The load regulation is defined as Equation (5). Similarly to [20,21], the specification of the load regulation is measured at an input/output voltage of 3.3 V/1.8 V and a load current varying from 0.5 A to 0.1 A. From the simulation results shown in Figure 11, the load regulation is 0.01% through Equation (5).

$$\text{Load Regulation} = \frac{V_{o@0.1A\ load\ current} - V_{o@0.5A\ load\ current}}{V_{o@0.5A\ load\ current}} \cdot 100\% \quad (5)$$

where $V_{o@0.5A\ load\ current}$ is the output voltage at a load current of 0.5 A, and $V_{o@0.1A\ load\ current}$ is the output voltage at a load current of 0.1 A.

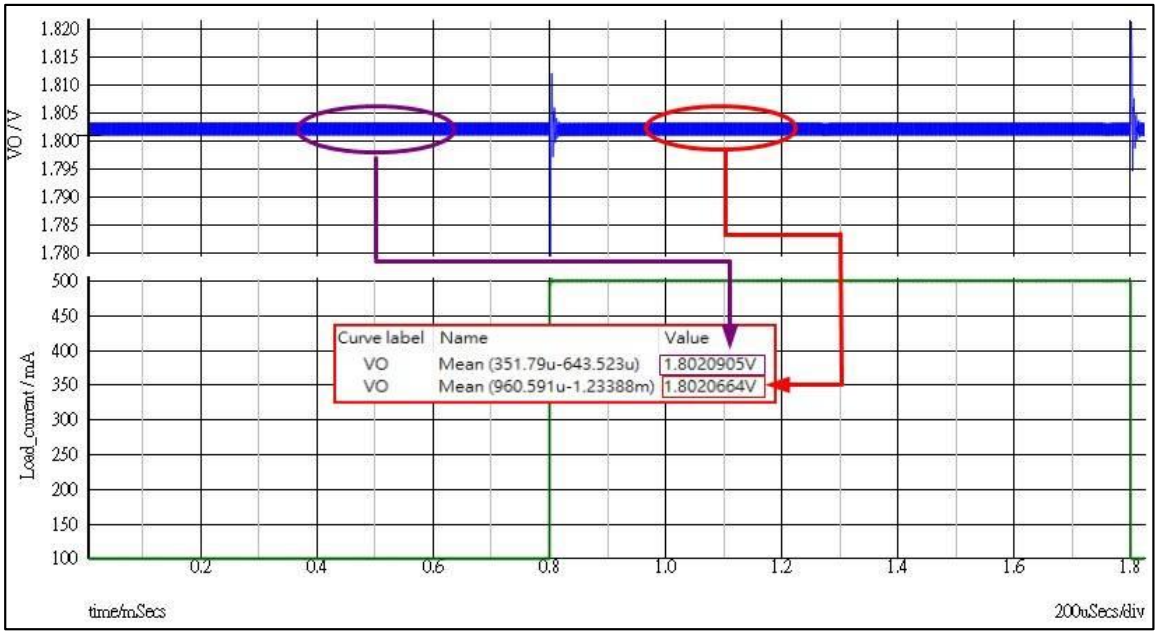


Figure 11. Load regulation.

4.4. Switching Frequency Regulation

By using the constant frequency mechanism, the converter can keep the switching frequency constant. The switching frequency at different output voltages (1.0–2.5 V) is shown in Figure 12. The measurement results in Figure 12 show that the switching

frequency can be maintained at around 1 MHz for different output voltages and max load current (500 mA).

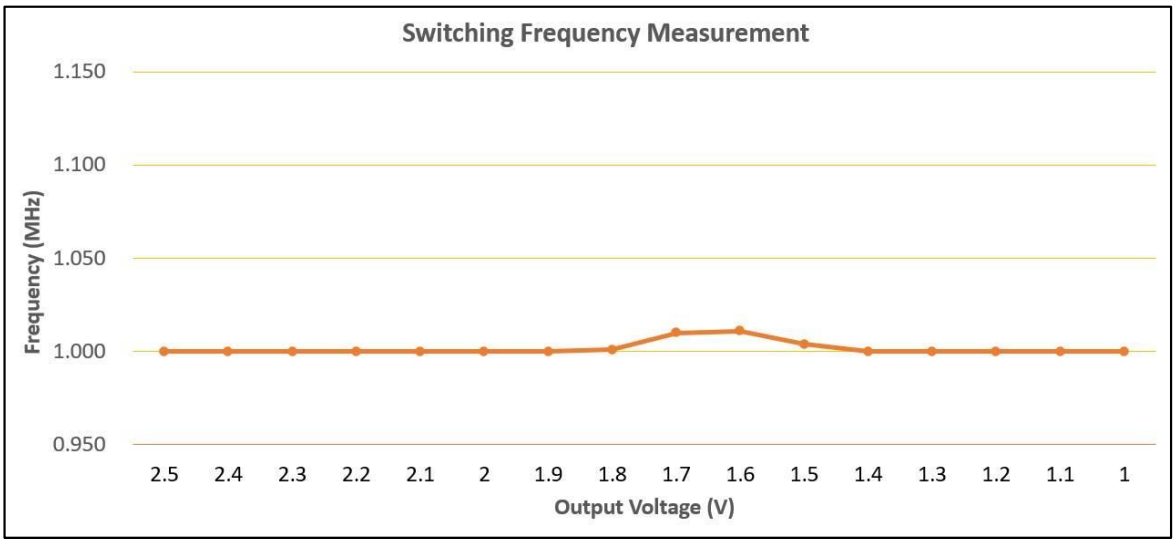


Figure 12. The measurements of the switching frequency.

4.5. Performance Summary

The performance of the proposed converter is listed in Table 2. As Table 2 shows, for the current transition between the 100 mA and 500 mA, the recovery time is less than 1.6 µs. At the same time, the converter has good performance at an input voltage of 3.0 V–3.6 V and an output voltage of 1.8 V. Finally, the performance comparison with the presented converters is listed in Table 3.

Table 2. Performance of Proposed Converter.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output capacitor	C_o	ESR: 5 mΩ		10		µF
Inductor	L	DCR *: 30 mΩ		4.7		µH
Output voltage	V_o		1.0		2.5	V
Input supply voltage	V_{in}		3.0		3.6	V
Load current	I_{load}		100		500	mA
Output ripple	V_{pp}	V_{in} = 3.6 V, V_o = 2.5 V			2.2	mV
Switching frequency	f_{sw}	Load current: 500 mA @ V_{in} = 3.3 V, V_o = 1.0–2.5 V		1		MHz
Recovery time (step-up)	T_{step_up}	Load current: 100 mA to 500 mA @ V_{in} = 3.3 V, V_o = 1.8 V		1.57		µs
Recovery time (step-down)	T_{step_dn}	Load current: 500 mA to 100 mA @ V_{in} = 3.3 V, V_o = 1.8 V		1.34		µs
Overshoot	$V_{ovshoot}$	Load current: 500 mA to 100 mA @ V_{in} = 3.3 V, V_o = 1.8 V		21		mV
Undershoot	$V_{unshoot}$	Load current: 100 mA to 500 mA @ V_{in} = 3.3 V, V_o = 1.8 V		21		mV

* DCR: DC resistance of inductor.

The comparisons in Table 3 are briefly discussed as follows:

(a) For the parameter in recovery time, we can find that the proposed scheme is better than the simulation results of [15,21–25]. The measurement results of [11,26–28] are worse than the proposed scheme, and the numerical differences are large. For this

purpose, one is the measurement result, and the other is the simulation result. This is the major difference.

(b) For the parameter in undershoot/overshoot: this parameter is greatly affected by the load conditions and the output capacitor. For example, if the output capacitor is large, then the undershoot/overshoot is small. Or, if the load current step of the load conditions is small, then the undershoot/overshoot is small. Therefore, under the same test conditions, the performance of the proposed scheme is better than [15,21,22].

(c) For the parameter in switching frequency, we can find that in most of the literature, the switching frequency is designed around 1 MHz.

(d) For the parameter in switching frequency variation, we can find that the discussion on switching frequency variation is a minority in all the comparison literature, and only appears in [11,21,22]. The switching frequency variation of the proposed scheme is less than 1.2%.

Table 3. Performance Comparisons with Reported Converters.

References	**2018 [23]**	**2020 [24]**	**2021 [15]**	**2021 [22]**	**2022 [21]**	**This Work**
Results	simulation	simulation	simulation	simulation	simulation	simulation
Control scheme	AOT	AOT	AOT	AOT	AOT	AOT
Process (μm)	0.35	0.18	0.35 *	0.18 *	0.35 *	0.18 *
Input voltage (V)	12	3.3–5.0	3.0–3.6	3.0–3.6	3.0–3.6	3.0–3.6
Output voltage (V)	1.2	1.8	1.0–2.5	1.0–2.5	1.0–2.5	1.0–2.5
Inductor (μH)	1	1.5	4.7	4.7	4.7	4.7
Output Capacitor (μF)	47	20	10	10	10	10
Switching Frequency (MHz)	1	1	1	1	1	1
Switching frequency variation (%)	N/A	N/A	N/A	1	3.5	1.2
Max. Load current (mA)	5000	2000	500	500	500	500
Load current step (mA)	4000	800	400	400	400	400
Undershoot/Overshoot (mV)	20/26	13/14	23/26	20/24	21/30	21/21
Recovery time (μs) (rise/fall)	<3	6/2	1.98/1.6	1.69/1.62	1.8/1.5	1.57/1.34
References	2019 [25]	2021 [11]	2021 [26]	2021 [27]	2022 [28]	
Results	measurement	measurement	measurement	measurement	measurement	
Control scheme	Current-Mode Hysteretic	Hysteretic PLL	COT	COT	AOT	
Process (μm)	0.065	0.35	0.13	0.18	0.18	
Input voltage (V)	3.3	3.3–3.6	7–15	4.25–15	1.6–2.2	
Output voltage (V)	0.6–2.0	0.9–2.5	5–7	1.1	0.4–1.2	
Inductor (μH)	2.2	4.7	2.2	0.47	0.33	
Output Capacitor (μF)	10	10	10	47*3	10	
Switching Frequency (MHz)	1	1	2	0.5–1.25	3	
Switching frequency variation (%)	N/A	1	N/A	42	N/A	
Max. Load current (mA)	1500	600	2000	5000	500	
Load current step (mA)	900	400	2000	5000	450	
Undershoot/Overshoot (mV)	106/87	30/60	85/72	30/15.7	20/20	
Recovery time (μs) (rise/fall)	3.4/3.6	2.6/2.2	3/2.7	80/45	3.4/3.6	

* This work is system level simulation with SIMPLIS.

5. Conclusions

In this paper, a new control scheme of the buck converter was proposed. This converter uses an alternative method to control the T_{ON}, and T_{OFF}. The converter has three features/advantages. First, the T_{OFF} is controlled to keep the switching frequency constant. The constant switching frequency feature can alleviate the EMI issue in applications. In addition, it is not difficult to implement, requiring only the PFD, charge pump, and low pass filter. Second, the control method is based on CMC technique, but does not require the actual current sensor, which greatly reduces the complexity of the circuit. Third, the circuit is easy to realize and does not have special layout considerations; thus, it is suitable for mass production. Finally, the converter was verified by SIMPLIS. From the simulation results, the control topology has good transient performance. In future, the scheme can be implemented with UMC 0.18 μm 1P6M CMOS processes.

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