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Variable Multiple Interleaved Bi-Directional DC/DC Converter with Current Ripple Optimization

Jiandong Duan [1], Shuai Wang [1], Yiming Xu [1], Shaogui Fan [2,*], Ke Zhao [1] and Li Sun [1]

[1] Department of Electrical Engineering, Harbin Institute of Technology, Harbin 150001, China
[2] Yantai Research Institute, Harbin Engineering University, Yantai 265615, China
* Correspondence: fanshaogui2008@hrbeu.edu.cn

Abstract: In order to reduce the current ripple and improve the power density of the system, the multiple structure design is generally adopted by the traditional bidirectional DC/DC converter. However, the fixed multiplicity design can't make the DC/DC power converter always output the smallest current ripple under different duty ratios. Through this research, it is found that the current ripple is related to duty cycle and parallel multiplicity, and then a variable multiplicity bidirectional DC/DC power converter is proposed. Firstly, the relationship between the current ripple and parallel multiplicity and duty cycle is deduced, and the basic topology of variable multiplicity bidirectional DC/DC power converter is determined; Secondly, the average value model and AC small signal model of the system are established based on the topological structure, and then the state equation is obtained. Thirdly, the current compensation control method is designed based on the state equation. Finally, the experimental platform of variable multiplicity bidirectional DC/DC power converter is built.

Keywords: bidirectional DC/DC converter; current ripple optimization; constant current control

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1. Introduction

Energy storage systems have been widely used to improve the power distribution between renewable power generation, large power grids, and user loads [1–3]. As the power transmission channel between the DC bus and the energy storage system, the bidirectional DC/DC converter can realize bidirectional energy flow and improve energy distribution efficiency [4–6]. However, the DC/DC converter may introduce a large current ripple to the DC bus, which affects the quality of the power supply [7,8].

Many researchers have proposed different methods to reduce the current ripple, each of which has its advantages [9–11]. At present, the current ripple optimization methods of DC/DC converter mainly include: input parallel output series (IPOS) DC/DC converter, ripple current injection DC/DC converter, resonant ripple absorption DC/DC converter, DC/DC converter using coupled inductor technology, multiple DC/DC converter, etc. Reference [12] studied an IPOS DC/DC converter, which could offset the current ripple to a certain extent, but has the problem of low voltage gain. The DC/DC converter with ripple current injection proposed in [13] artificially injects ripple current at both ends of the inductor to eliminate the ripple current. The ripple suppression effect is good, but the circuit is more complicated. Reference [14] proposed a resonant ripple absorption DC/DC converter that uses the LC devices to generate resonance to optimize the current ripple, but the ripple suppression capability for dynamic loads is poor due to the fixed system parameters. The DC/DC converter with coupled inductor technology [15] replaces the inductor in the traditional DC/DC converter with a coupled inductor. When the coupling coefficient of the coupled inductor is selected reasonably, a better ripple suppression effect can be achieved, however, the switching stress is larger due to the influence of leakage inductance. The multiple DC/DC converter adopts multiple structure and has

high power grade. The increase in converter multiplicity can reduce the current ripple, reduce the switching stress, improve the equivalent switching speed, improve the dynamic performance, and then improve the power quality [16–23].

The above current ripple optimization methods of DC/DC converters mainly have the problems of large switching stress and low voltage gain, so they are difficult to be applied to high power energy storage systems, while the traditional multiple DC/DC converters can not only reduce switching stress, but also achieve better current ripple suppression through continuous improvement, so they are widely used in high power energy storage systems [18,19]. Energy storage systems (especially battery energy storage systems) are highly sensitive to current ripples, and excessive current ripples will affect the service life of the system. Reducing the current ripple of the converter is of great significance for improving the quality of the power supply, prolonging the service life of the system. However, the existing research mostly studies improving the circuit structure of the multiplexed DC/DC converter to optimize the current ripple, such as using the coupled inductor instead of the traditional inductor [15] and using the new SiC device [24], the working model of the multiplexed converter is also limited to the fixed multiplicity model, and there are few studies on the influence of changing the parallel multiplicity on the current ripple. In fact, related researches find the multiplicity of parallel circuits also has an important influence on the magnitude of current ripple, and there is always a parallel multiplicity corresponding to the minimum current ripple under different duty cycle [20–23]. The main contribution of this paper is to propose a current ripple optimization method for bidirectional DC/DC converters by changing the multiplicity of parallel circuits. In reference [25], increasing the switching frequency can reduce the current ripple, but this will inevitably increase the loss and reduce the efficiency. The biggest feature of the method in this paper is that the actual operating multiplicity of the multiplexed DC/DC converter will be dynamically changed according to the duty cycle, as a result, the current ripple is optimized without changing the switching frequency. The improvements are shown as follows: Firstly, the relationship between the current ripple and parallel multiplicity and duty cycle is studied. Secondly, a control method that can change the parallel multiplicity of the DC/DC converter to optimize the current ripple is proposed. Thirdly, considering there are many similar circuits in the multiplex DC/DC converter, there will be the problem of uneven current distribution due to the differences in devices. Although automatic master control overcomes the vulnerability of the master-slave method, where the master is auto-selected by the maximum, it can trigger larger fluctuations in the output current [26]. In this paper, automatic master control and current compensation control are combined, compared with the single automatic master control, this method can better realize the current balance distribution and optimize fluctuations on the output current when the parallel multiple is switching.

This paper is organized as follows: In Section 2, the relationship between the current ripple and parallel multiplicity and duty cycle is deduced, and the basic topology of variable multiplicity bidirectional DC/DC power converter is determined. In Section 3, the average value model and AC small signal model of the system are established. In Section 4, the current compensation control is designed. In Section 5, the simulation model and the experimental platform of variable multiplicity interleaving bidirectional DC/DC power converter is built. The simulation and experiment results show that the optimization of the current ripple of the variable multiplicity bidirectional DC/DC converter is obvious.

2. The Principle of Current Ripple Optimization

Assuming that the bidirectional DC/DC converter operates in Buck mode, the topology of the converter is shown in Figure 1.

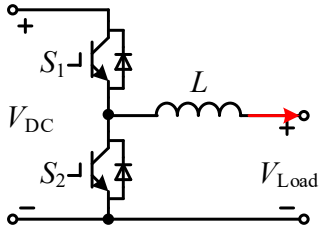


Figure 1. Bidirectional DC/DC converter in Buck mode.

The relationship among load-side voltage U_{Load}, DC bus voltage, and duty cycle D is shown as follows:

$$V_{Load} = DV_{DC} \tag{1}$$

For inductance L, the slope of the current rising phase is defined as k_{up}, and the slope of the current decreasing phase is defined as k_{down}.

$$\begin{cases} k_{up} = \frac{V_{DC} - V_{Load}}{L} \\ k_{down} = \frac{V_{Load}}{L} \end{cases} \tag{2}$$

In same-phase driving mode, i_{L1}, i_{L2}, i_{L3}, i_{L4}, and so on are exactly equal, then the peak-to-peak value of the ripple of total current can be shown as:

$$\Delta i_{Ls} = \Delta i_{L1} + \Delta i_{L2} + \ldots + \Delta i_{Ln} = nDk_{up}T \tag{3}$$

In the phase-shift control, the relationship between the current and time is established by setting the current i_{L1} as the zero point at the initial time of a switching cycle [0,T]. The current i_{L1}, i_{L2}, i_{L3}, i_{L4}, and so on are shown in Figure 2.

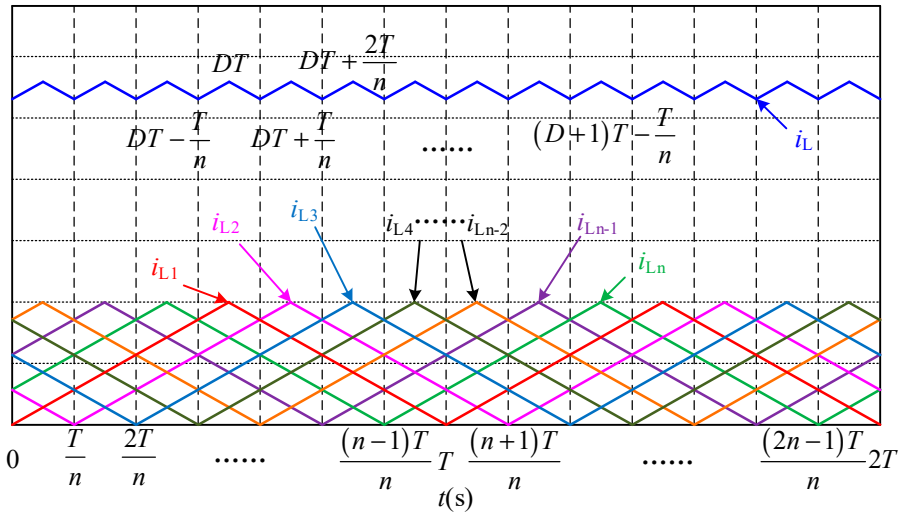


Figure 2. Multiple inductor current and total current waveform.

Assuming that the slope of n_{down}-fold inductor current at the initial stage is k_{down}, and satisfies $n_{down} + n_{up} = n$. Then the following relationship can be obtained.

$$\begin{cases} \lceil (1-D)n - 1 \rceil = n_{down} \\ \lfloor Dn + 1 \rfloor = n_{up} \end{cases} \tag{4}$$

Then, the duty cycle has the following relationship: $1 - \frac{n_{down}+1}{n} \leq D \leq 1 - \frac{n_{down}}{n}$. Assuming that D is 50%, and $n_{down} = \frac{n}{2}$ or $n_{down} = \frac{n-1}{2}$ can be obtained according to the parity of n.

The expression of the first inductance current is shown as:

$$\begin{cases} i_{L1} = k_{up}t & t \in [0, DT] \\ i_{L1} = k_{down}(t - T) & t \in [DT, T] \end{cases} \tag{5}$$

The expression of the second inductance current can be shown as:

$$\begin{cases} i_{L2} = k_{down} \cdot \left(t - \frac{T}{n}\right) & t \in \left[0, \frac{T}{n}\right] \\ i_{L2} = k_{up} \cdot \left(t - \frac{T}{n}\right) & t \in \left[\frac{T}{n}, DT + \frac{T}{n}\right] \\ i_{L2} = k_{down} \cdot \left(t - \frac{n+1}{n}T\right) & t \in \left[DT + \frac{T}{n}, T\right] \end{cases} \tag{6}$$

The expression of the third inductance current can be shown as:

$$\begin{cases} i_{L3} = k_{down} \cdot \left(t - \frac{2T}{n}\right) & t \in \left[0, \frac{2T}{n}\right] \\ i_{L3} = k_{up} \cdot \left(t - \frac{2T}{n}\right) & t \in \left[\frac{2T}{n}, DT + \frac{2T}{n}\right] \\ i_{L3} = k_{down} \cdot (t - \frac{n+2}{n}T) & t \in \left[DT + \frac{2T}{n}, T\right] \end{cases} \tag{7}$$

The expression of the n-th inductance current can be shown as:

$$\begin{cases} i_{Ln} = k_{up} \cdot \left(t + \frac{T}{n}\right) & t \in \left[0, DT - \frac{T}{n}\right] \\ i_{Ln} = k_{down} \cdot \left(t - \frac{n-1}{n}T\right) & t \in \left[DT - \frac{T}{n}, \frac{n-1}{n}T\right] \\ i_{L3} = k_{up} \cdot \left(t - \frac{n-1}{n}T\right) & t \in \left[\frac{n-1}{n}T, T\right] \end{cases} \tag{8}$$

According to Kirchhoff's law, the expression of the i_L in a switching cycle can be obtained and can be extended to the n-th cycle, which is shown in (9).

$$\begin{cases} i_L = (n_{up}k_{up} + n_{down}k_{down})t + \frac{n_{up}k_{up}T}{2n}(n_{up} - 1) & \\ \quad - \frac{n_{down}k_{down}T}{2n}(n_{down} + 1) & t \in \left[0, DT - \frac{n_{up}-1}{n}T\right] \\ i_L = \left((n_{up} - 1)k_{up} + (n_{down} + 1)k_{down}\right)t & \\ \quad + \frac{k_{up}(n_{up}-1)(n_{up}-2)}{2n}T - \frac{k_{down}(n_{down}+1)(n_{down}+2)}{2n}T & t \in \left[DT - \frac{n_{up}-1}{n}T, \frac{T}{n}\right] \\ i_L = \left((n_{up} - 1)k_{up} + (n_{down} + 1)k_{down}\right)t & \\ \quad + \frac{k_{up}(n_{up}-1)(n_{up}-4)}{2n}T - \frac{k_{down}(n_{down}+1)(n_{down}+4)}{2n}T & t \in \left[DT - \frac{n_{up}-2}{n}T, \frac{2T}{n}\right] \\ \quad \vdots & \\ i_L = (n_{up}k_{up} + n_{down}k_{down})t & \\ \quad + \frac{n_{up}k_{up}T}{2n}(n_{up} - 2n + 1) - \frac{n_{down}k_{down}T}{2n}(n_{down} + 2n - 1) & t \in \left[\frac{n-1}{n}T, DT + \frac{n_{down}T}{n}\right] \\ i_L = \left((n_{up} - 1)k_{up} + (n_{down} + 1)k_{down}\right)t & \\ \quad + \frac{k_{up}(n_{up}-1)(n_{up}-2n)}{2n}T - \frac{k_{down}(n_{down}+1)(n_{down}+2n)}{2n}T & t \in \left[DT + \frac{n_{down}T}{n}, T\right] \end{cases} \tag{9}$$

According to (5)–(9) and Figure 2, when phase shift control is applied to the n-fold DC/DC converter, the total ripple of the current flowing through the inductor L is shown in (10):

$$\begin{aligned} \Delta i_{Lm} &= \left(n_{up}k_{up} + n_{down}k_{down}\right) \cdot \left(DT - \frac{n_{up}-1}{n}T\right) \\ &= \frac{TV_{DC}}{L} \cdot \frac{[(1-D)(\lfloor Dn+1 \rfloor) - D(\lceil (1-D)n-1 \rceil)] \cdot [Dn - (\lfloor Dn+1 \rfloor) + 1]}{n} \end{aligned} \tag{10}$$

Define k_{Lm} as the ripple coefficient, which is shown in (11).

$$k_{Lm} = \frac{[(1-D)(\lfloor Dn+1 \rfloor) - D(\lceil (1-D)n-1 \rceil)] \cdot [Dn - (\lfloor Dn+1 \rfloor) + 1]}{n} \tag{11}$$

The expression of (11) can be rewritten to.

$$\Delta i_{\mathrm{Lm}} = \frac{TV_{\mathrm{DC}}}{L} \cdot k_{\mathrm{Lm}} \tag{12}$$

It can be seen from (11) that the ripple coefficient k_{Lm} is affected by the duty cycle D and the number of parallel multiplicity n. When the bidirectional DC/DC converter operates in Buck mode, the relationship between the ripple coefficient k_{Lm}, the duty cycle D, and the number of parallel channel multiplicity n is shown in Figure 3. It can be seen from Figure 3 that there is a point where the ripple coefficient k_{Lm} is 0 when different numbers of parallel multiplicity n and different duty cycle D are taken.

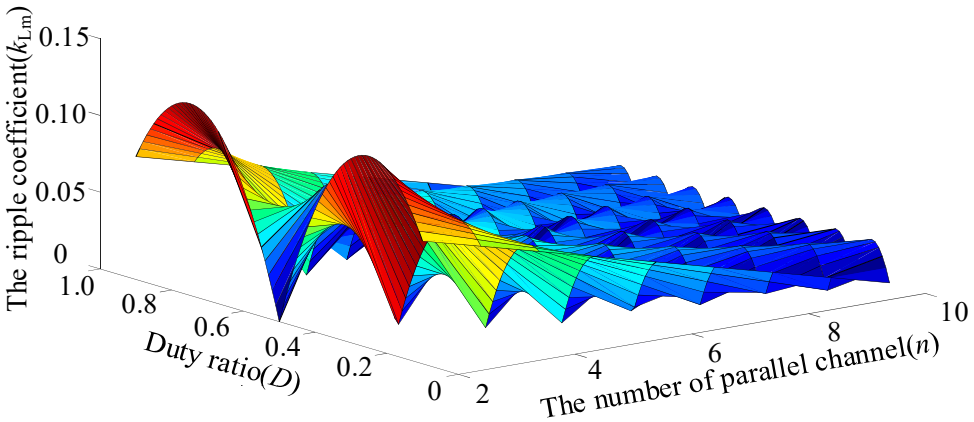


Figure 3. The relationship among k_{Lm}, D, and n of bidirectional DC/DC converter in Buck mode.

According to (11), the relationship between ripple coefficient k_{Lm} and duty cycle D can be obtained, shown in Figure 4, when the number of multiplicities is different. It can be seen from Figure 4 that there are $n-1$ points where the ripple coefficient is zero for the n-multiplicity bidirectional DC/DC power converter.

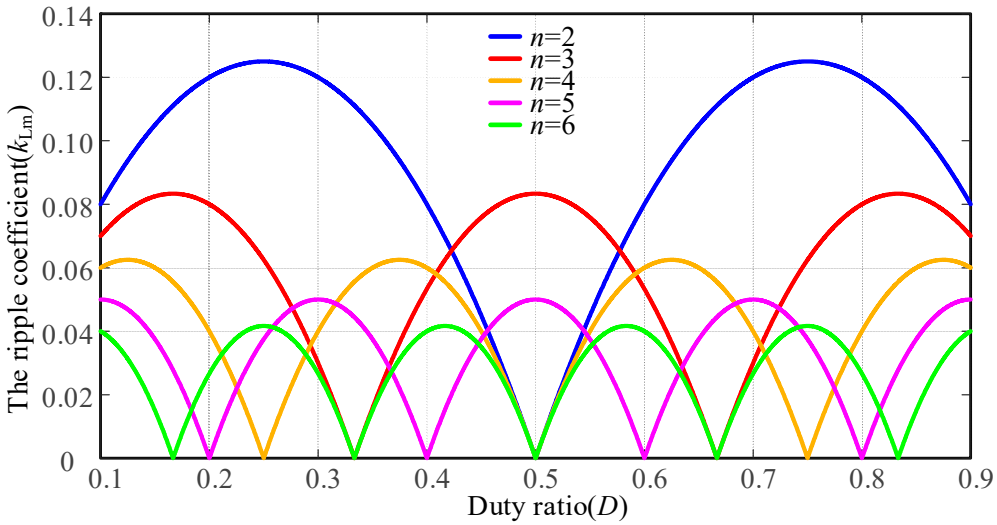


Figure 4. Relationship between k_{Lm} and D with different parallel multiplicity.

As can be seen from Figure 4, under the condition of different duty cycles, it is not that the more parallel multiplicity, the smaller the current ripple coefficient. Although the ripple coefficient generally decreases with the increase of parallel multiplicity, considering that too many parallel multiplicities will increase the complexity of the circuit; and more when the number of parallel multiplicities is greater than six, the increase of parallel multiplicity has no obvious effect on the reduction of current ripple. The principle of the variable

multiplicity bidirectional DC/DC power converter is to automatically select the working number of parallel multiplicities according to the current duty cycles of the system. The number of parallel multiplicities that should be used for the minimum current ripple when the duty cycle is in the range of 0.1–0.9 is shown in Table 1. For example, when the duty cycle of the system is 0.25, the quadruple parallel structure should be adopted, and the controller outputs four PWM signals with a 90-degree phase shift in each multiplicity.

Table 1. The number of parallel multiplicities corresponding to different duty cycles.

Range of Duty Cycles	Number of Parallel Multiplicities
0.1000~0.1835	6
0.1835~0.2254	5
0.2254~0.2887	4
0.2887~0.3675	6
0.3675~0.4772	5
0.4772~0.5528	6
0.5528~0.6324	5
0.6324~0.7113	6
0.7113~0.7746	4
0.7746~0.8165	5
0.8165~0.9000	6

Figure 5 shows the number of parallel multiplicities that should be taken to minimize the current ripple. For example, when the duty cycle is 0.2, a five-fold parallel structure should be adopted, and the current ripple is the smallest; when the duty cycle is 0.25, a four-fold parallel structure should be adopted. Thus, a curve with the smallest current ripple can be obtained in Figure 5. By calculating the intersection point of the minimum current ripple carve in Figure 5, the corresponding relationship between the parallel multiplicity and the duty range can be obtained, as shown in Table 1.

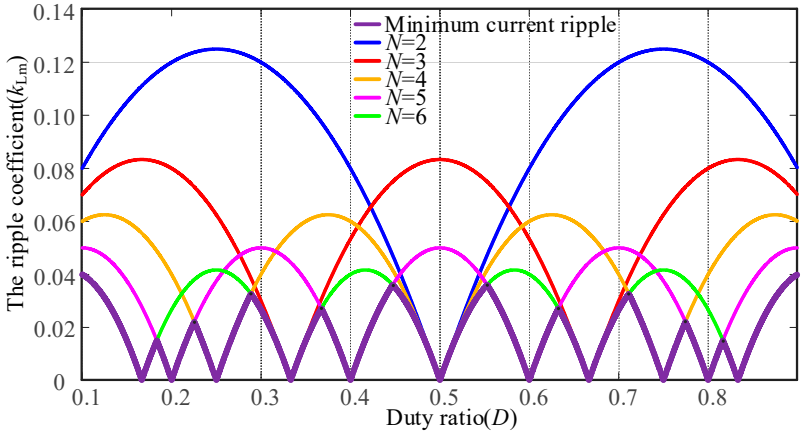


Figure 5. Parallel multiplicity corresponding to the minimum current ripple coefficient under different duty cycles.

3. The Model of Variable Multiplicity Interleaving Bidirectional DC/DC Power Converter

3.1. The Mean Value Model

In Figure 6, V_{DC} is DC side voltage, i_{DC} is DC side current, i_{Lk} ($1 \leq k \leq n$) is inductor current, R_k ($1 \leq k \leq n$) is the resistance of the inductor, V_L is inductor voltage, V_{Load} is load-side voltage, i_{Load} is load-side current, and D is duty cycle.

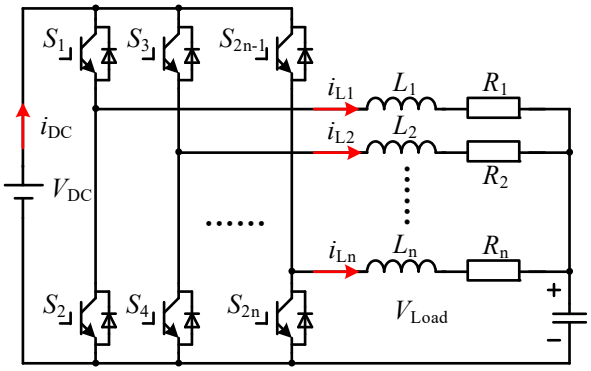


Figure 6. The topology of variable multiplicity bidirectional DC/DC power converter.

The DC side current is shown as:

$$i_{DC} = \sum_{k=1}^{n} D_k i_{Lk} \tag{13}$$

When the lower arm is turned off and the upper arm is turned on, the voltages at both ends of each inductance can be shown as:

$$\begin{cases} V_{L1} = L_1 \frac{di_{L1}}{dt} = V_{DC} - V_{Load} - i_{L1} R_1 \\ V_{L2} = L_2 \frac{di_{L2}}{dt} = V_{DC} - V_{Load} - i_{L2} R_2 \\ \vdots \\ V_{Ln} = L_n \frac{di_{Ln}}{dt} = V_{DC} - V_{Load} - i_{Ln} R_n \end{cases} \tag{14}$$

When the lower arm is turned on and the upper arm is turned off, the voltages at both ends of each inductance can be shown as:

$$\begin{cases} V_{L1} = L_1 \frac{di_{L1}}{dt} = -V_{Load} - i_{L1} R_1 \\ V_{L2} = L_2 \frac{di_{L2}}{dt} = -V_{Load} - i_{L2} R_2 \\ \vdots \\ V_{Ln} = L_n \frac{di_{Ln}}{dt} = -V_{Load} - i_{Ln} R_n \end{cases} \tag{15}$$

Because the switching period T_s is very small, it can be considered that V_{DC} and V_{Load} are continuous and constant in a switching period. They can be expressed by their average values in a period.

$$\begin{cases} V_{DC} = \langle V_{DC} \rangle_{T_s} \\ V_{Load} = \langle V_{Load} \rangle_{T_s} \end{cases} \tag{16}$$

According to the volt-ampere characteristics and volt-second balance principle of the inductor, the average voltage of the inductor shown in (17) in a switching cycle can be obtained by dealing with Equations (14)–(16).

$$\begin{cases} \langle v_{L1}(t) \rangle_{T_s} = \frac{1}{T_s} \left[\int_0^{D_1 T_s} v_{L1}(t) dt + \int_{D_1 T_s}^{T_s} v_{L1}(t) dt \right] = D_1 \langle V_{DC} \rangle_{T_s} - \langle V_{Load} \rangle_{T_s} - \langle i_{L1} \rangle_{T_s} R_1 \\ \langle v_{L2}(t) \rangle_{T_s} = \frac{1}{T_s} \left[\int_0^{D_2 T_s} v_{L2}(t) dt + \int_{D_2 T_s}^{T_s} v_{L2}(t) dt \right] = D_2 \langle V_{DC} \rangle_{T_s} - \langle V_{Load} \rangle_{T_s} - \langle i_{L2} \rangle_{T_s} R_2 \\ \vdots \\ \langle v_{Ln}(t) \rangle_{T_s} = \frac{1}{T_s} \left[\int_0^{D_n T_s} v_{Ln}(t) dt + \int_{D_n T_s}^{T_s} v_{Ln}(t) dt \right] = D_n \langle V_{DC} \rangle_{T_s} - \langle V_{Load} \rangle_{T_s} - \langle i_{Ln} \rangle_{T_s} R_n \end{cases} \tag{17}$$

According to the volt-ampere characteristics of the capacitor and Kirchhoff's current law, the average current flowing through the load capacitor in a switching cycle can be obtained.

$$\begin{aligned} \langle i_{\mathrm{Load}}(t)\rangle_{T_s} &= C\frac{d\langle v_{\mathrm{Load}}(t)\rangle_{T_s}}{dt} \\ &= \langle i_{\mathrm{L1}}(t)\rangle_{T_s} + \langle i_{\mathrm{L2}}(t)\rangle_{T_s} + \cdots + \langle i_{\mathrm{Ln}}(t)\rangle_{T_s} \end{aligned} \tag{18}$$

The characteristic equation of inductance after averaging treatment is.

$$\begin{cases} \langle v_{\mathrm{L1}}(t)\rangle_{T_s} = L_1\frac{d\langle v_{\mathrm{L1}}(t)\rangle_{T_s}}{dt} \\ \langle v_{\mathrm{L2}}(t)\rangle_{T_s} = L_2\frac{d\langle v_{\mathrm{L2}}(t)\rangle_{T_s}}{dt} \\ \vdots \\ \langle v_{\mathrm{Ln}}(t)\rangle_{T_s} = L_n\frac{d\langle v_{\mathrm{Ln}}(t)\rangle_{T_s}}{dt} \end{cases} \tag{19}$$

Substitute Equation (19) into Equation (17), and the following Equation (20) can be obtained.

$$\begin{cases} L_1\frac{d\langle v_{\mathrm{L1}}(t)\rangle_{T_s}}{dt} = D_1\langle V_{\mathrm{DC}}\rangle_{T_S} - \langle V_{\mathrm{Load}}\rangle_{T_S} - \langle i_{\mathrm{L1}}\rangle_{T_S}R_1 \\ L_2\frac{d\langle v_{\mathrm{L2}}(t)\rangle_{T_s}}{dt} = D_2\langle V_{\mathrm{DC}}\rangle_{T_s} - \langle V_{\mathrm{Load}}\rangle_{T_s} - \langle i_{\mathrm{L2}}\rangle_{T_s}R_2 \\ \vdots \\ L_n\frac{d\langle v_{\mathrm{Ln}}(t)\rangle_{T_s}}{dt} = D_n\langle V_{\mathrm{DC}}\rangle_{T_s} - \langle V_{\mathrm{Load}}\rangle_{T_s} - \langle i_{\mathrm{Ln}}\rangle_{T_s}R_n \end{cases} \tag{20}$$

According to Equations (18) and (20), the average value model of the variable multiplicity bidirectional DC/DC power converter in Buck mode can be obtained, as shown in Figure 7.

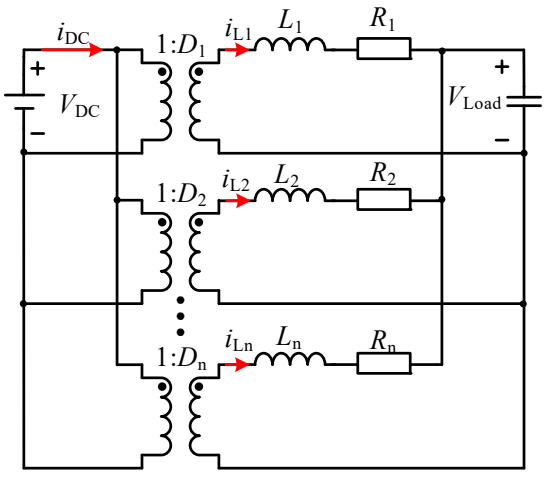


Figure 7. The average value model of the variable multiplicity bidirectional DC/DC power converter in Buck mode.

3.2. The AC Small Signal Model

Equations (17) and (18) obtained in the mean value model are nonlinear equations, so it is complex to solve them directly. However, there are DC components and low-frequency small signal components in the variable, which can be solved in approximate ways. The specific idea is to study the state of the DC/DC power converter near the steady-state working point, where the linearization is satisfied, and the equation can be linearized to separate the DC components and small signal components [27]. Conditions are as follows: the interleaved bidirectional DC/DC power converters should satisfy the low-frequency assumption, small ripple assumption, and small signal assumption in the process of modeling the AC small signal model [27,28].

$$|\hat{x}(t)| \ll |X| \tag{21}$$

In Equation (21) [27], $|\hat{x}(t)|$ is the amplitude of the AC component, while $|X|$ is the amplitude of the DC component.

In a switching cycle, any variable can be divided into DC components and AC small signal components, which is shown in (22).

$$\begin{cases} \langle i_{\mathrm{Lk}} \rangle_{T_s} = I_{\mathrm{Lk}} + \hat{i}_{\mathrm{Lk}}(t) \\ \langle D_{\mathrm{k}} \rangle_{T_s} = D_{\mathrm{k}} + \hat{d}_{\mathrm{k}}(t) \\ \langle v_{\mathrm{Load}} \rangle_{T_s} = V_{\mathrm{Load}} + \hat{v}_{\mathrm{Load}}(t) \\ \langle v_{\mathrm{DC}} \rangle_{T_s} = V_{\mathrm{DC}} + \hat{v}_{\mathrm{DC}}(t) \\ \langle i_{\mathrm{Load}} \rangle_{T_s} = I_{\mathrm{Load}} + \hat{i}_{\mathrm{Load}}(t) \end{cases} \quad (1 \le k \le 6, k \text{ is integer}) \tag{22}$$

Equation (22) being brought into Equation (20) can get (23).

$$\begin{cases} L_1 \frac{d\left[I_{\mathrm{L1}} + \hat{i}_{\mathrm{L1}}(t)\right]}{dt} = \left[D_1 + \hat{d}_1(t)\right]\left[V_{\mathrm{DC}} + \hat{v}_{\mathrm{DC}}(t)\right] - \left[V_{\mathrm{Load}} + \hat{v}_{\mathrm{Load}}(t)\right] - \left[I_{\mathrm{L1}} + \hat{i}_{\mathrm{L1}}(t)\right]R_1 \\ L_2 \frac{d\left[I_{\mathrm{L2}} + \hat{i}_{\mathrm{L2}}(t)\right]}{dt} = \left[D_2 + \hat{d}_2(t)\right]\left[V_{\mathrm{DC}} + \hat{v}_{\mathrm{DC}}(t)\right] - \left[V_{\mathrm{Load}} + \hat{v}_{\mathrm{Load}}(t)\right] - \left[I_{\mathrm{L2}} + \hat{i}_{\mathrm{L2}}(t)\right]R_2 \\ \vdots \\ L_{\mathrm{n}} \frac{d\left[I_{\mathrm{Ln}} + \hat{i}_{\mathrm{Ln}}(t)\right]}{dt} = \left[D_{\mathrm{n}} + \hat{d}_{\mathrm{n}}(t)\right]\left[V_{\mathrm{DC}} + \hat{v}_{\mathrm{DC}}(t)\right] - \left[V_{\mathrm{Load}} + \hat{v}_{\mathrm{Load}}(t)\right] - \left[I_{\mathrm{Ln}} + \hat{i}_{\mathrm{Ln}}(t)\right]R_{\mathrm{n}} \end{cases} \tag{23}$$

Ignoring the DC components and the second-order AC small signal components in Equation (23), the above equation can be transformed into the following form.

$$\begin{cases} L_1 \frac{d\hat{i}_{\mathrm{L1}}(t)}{dt} = D_1\hat{v}_{\mathrm{DC}}(t) + V_{\mathrm{DC}}\hat{d}_1(t) - \hat{v}_{\mathrm{Load}}(t) - \hat{i}_{\mathrm{L1}}(t)R_1 \\ L_2 \frac{d\hat{i}_{\mathrm{L2}}(t)}{dt} = D_2\hat{v}_{\mathrm{DC}}(t) + V_{\mathrm{DC}}\hat{d}_2(t) - \hat{v}_{\mathrm{Load}}(t) - \hat{i}_{\mathrm{L2}}(t)R_2 \\ \vdots \\ L_{\mathrm{n}} \frac{d\hat{i}_{\mathrm{Ln}}(t)}{dt} = D_{\mathrm{n}}\hat{v}_{\mathrm{DC}}(t) + V_{\mathrm{DC}}\hat{d}_{\mathrm{n}}(t) - \hat{v}_{\mathrm{Load}}(t) - \hat{i}_{\mathrm{Ln}}(t)R_{\mathrm{n}} \end{cases} \tag{24}$$

Solving Equations (22) and (18) simultaneously, the following equation can be obtained.

$$\hat{i}_{\mathrm{Load}}(t) = C\frac{d\hat{i}_{\mathrm{Load}}(t)}{dt} = \hat{i}_{\mathrm{L1}}(t) + \hat{i}_{\mathrm{L2}}(t) + \cdots + \hat{i}_{\mathrm{Ln}}(t) \tag{25}$$

According to Equations (24) and (25), the AC small signal model of the variable multiplicity bidirectional DC/DC power converter in Buck mode can be obtained, which is shown in Figure 8.

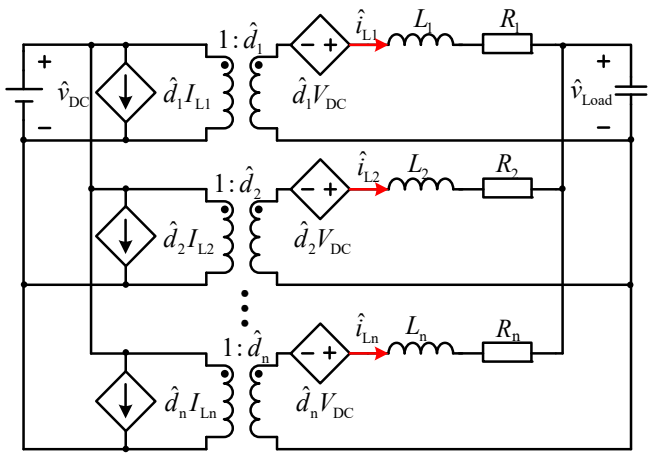


Figure 8. The AC small signal model of the variable multiplicity bidirectional DC/DC power converter in Buck mode.

4. The Design of Control Strategy for the Variable Multiplicity Interleaving Bidirectional DC/DC Power Converter

4.1. The Analysis of the Open-Loop Characteristic of the Variable Multiplicity Interleaving Bidirectional DC/DC Power Converter

In order to simplify the analysis, it is assumed that the parameters of each corresponding component in the variable multiplicity interleaving bidirectional DC/DC power converter are entirely equal.

$$\begin{cases} L_1 = L_2 = \cdots = L_n = L \\ L_{L1} = L_{L2} = \cdots = L_{Ln} = L_L \\ D_1 = D_2 = \cdots = D_n = D \\ R_1 = R_2 = \cdots = R_n = R \end{cases} \tag{26}$$

The equation of the frequency domain is obtained by the Laplace transform of Equations (24) and (25).

$$\begin{cases} sL\hat{i}_L(s) = D\hat{v}_{DC}(s) + V_{DC}\hat{d}(s) - \hat{v}_{Load}(s) - \hat{i}_L(s)R \\ \hat{i}_{Load}(s) = sC\hat{v}_{Load}(s) = n\hat{i}_L(s) \end{cases} \tag{27}$$

In order to control the load voltage V_{Load}, the input can be assumed to be the ideal voltage source,$\hat{v}_{DC}(s) = 0$. Then, the transfer function G_{id}(s) between duty cycle d(s) and inductance current i_L(s) can be obtained by simplifying Equation (27).

$$G_{id}(s) = \left.\frac{\hat{i}_L(s)}{\hat{d}(s)}\right|_{\hat{v}_{DC}(s)=0} = \frac{sCV_{DC}}{s^2LC + sCR + n} \tag{28}$$

The transfer function G_{vd}(s) between duty cycle d(s) and load voltage V_{Load} (s) can be obtained.

$$G_{vd}(s) = \left.\frac{\hat{v}_{Load}(s)}{\hat{d}(s)}\right|_{\hat{v}_{DC}(s)=0} = \frac{nV_{DC}}{s^2LC + sCR + nV_{DC}} \tag{29}$$

The transfer function G_{vi}(s) between inductance current i_L(s) and load voltage V_{Load} (s) can be obtained according to Equations (28) and (29).

$$G_{vi}(s) = \frac{G_{vd}(s)}{G_{id}(s)} = \frac{n\left(s^2LC + sCR + nV_{DC}\right)}{s^3C^2L + s^2C^2R + nsCV_{DC}} \tag{30}$$

Bring the data in Table 2 into Equation (28), and the transfer function G_{id}(s) can be obtained.

$$G_{id}(s) = \frac{sCV_{DC}}{s^2LC + sCR + n} = \frac{6s}{1.8 \times 10^{-4}s^2 + 6 \times 10^{-3}s + n} \tag{31}$$

Table 2. Parameters of variable multiplicity interleaving bidirectional DC/DC converter.

Parameter	Value
DC voltage V_{DC}	30 V
Switching period T_S	0.0001 s (10 kHz)
Inductance L	3 mH
Inductance resistance R	0.1 Ω
Load capacitance C	0.06 F
Initial voltage of load capacitor V_{C0}	5 V
Load current I_{Load}	6 A
Maximum number of parallel channels N	6

The Bode diagram corresponds to G_{id}(s) when the working multiples are 4, 5, and 6 respectively, as shown in Figure 9. It can be seen from the figure that the shapes of the Bode diagrams under different multiplicities are the same, so the transfer function of the

five multiplicities is selected as the research object, and the current compensation network is designed.

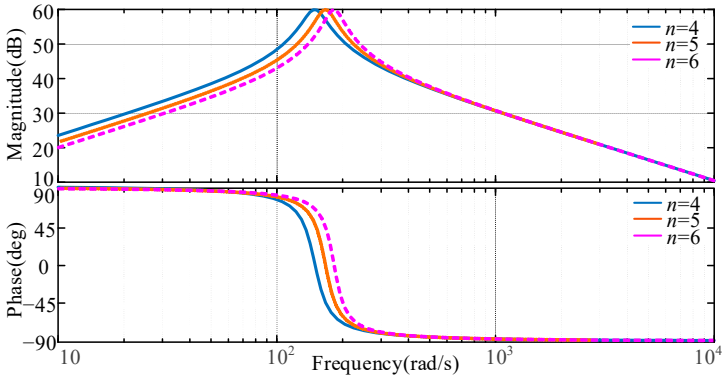


Figure 9. The Bode diagrams when the working number of the parallel multiplicity is 4, 5, or 6.

As can be seen from Figure 9, the amplitude-frequency characteristic curve is rising in the low-frequency band, there is a large steady-state error in the system. In the middle-frequency band, the crossover frequency is very high, and the system may be affected by switching frequency, harmonics, parasitic oscillation, and so on, unable to work stably. The high-frequency band declines slowly, and the system is vulnerable to high-frequency noise [29].

4.2. The Design of the Current Compensation Network

Due to the output current of variable multiplicity interleaving bidirectional DC/DC power converter being constant, the single current closed-loop control can be adopted, and the control strategy diagram is shown in Figure 10.

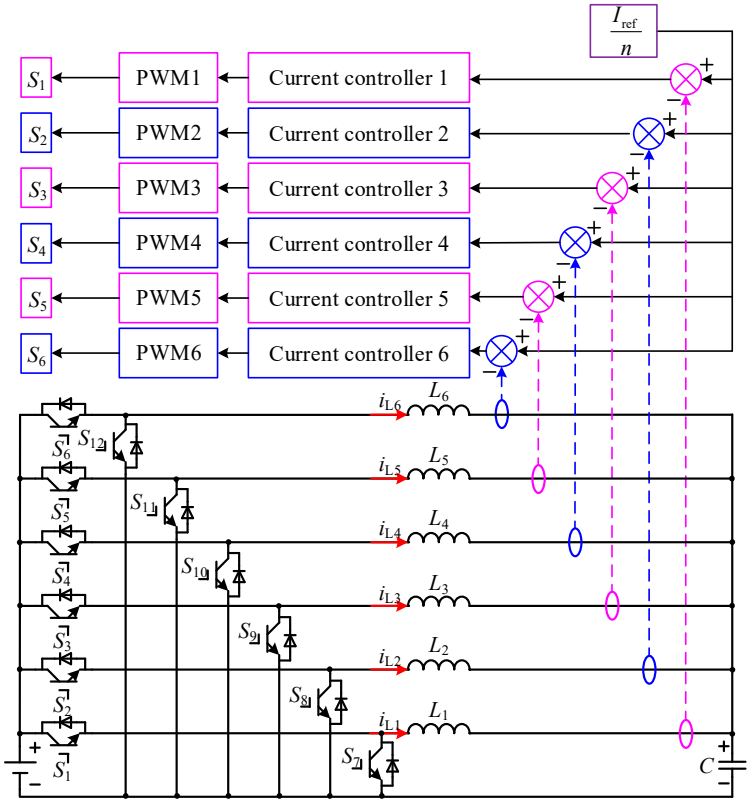


Figure 10. Control strategy diagram of variable multiplicity interleaving bidirectional DC/DC power converter.

When the converter is operating in Buck mode, and the number of working multiplicities is 5, then the transfer function of the current-loop-controlled object can be shown as.

$$G_{\mathrm{id}}(s) = \frac{6s}{1.8 \times 10^{-4}s^2 + 6 \times 10^{-3}s + 5} \tag{32}$$

Through the analysis of the above Bode diagram, it can be seen that there are at least two integral links in the compensation link so that the amplitude-frequency characteristic curve can decrease at the slope of −20 dB/dec in the low-frequency band. In order to make the system have a strong ability to suppress high-frequency noise, the high-frequency band of the amplitude-frequency characteristic curve should decrease at the slope of 40 dB/dec [29].

The transfer function of the current compensation network is:

$$G_{\mathrm{idc}}(s) = \frac{K(s + \omega_{Z1})(s + \omega_{Z2})}{s^2(s + \omega_{\mathrm{p}})} \tag{33}$$

The aim of introducing two integral links into the above formula is to make the amplitude-frequency characteristic curve decrease at the slope of −20 dB/dec in the low-frequency band. ω_{Z1} and ω_{Z2} are introduced to offset the two conjugate poles in the original transfer function. The ω_{p} can ensure that the corrected system has enough phase angle margin, at the same time, the amplitude-frequency characteristic curve can decrease at the slope of −40 dB/dec in the high-frequency band to suppress the high-frequency noise [29].

The transfer function of the current compensation link is:

$$G_{\mathrm{idc}}(s) = \frac{3 \times 10^6 \times \left(1.8 \times 10^{-4}s^2 + 6 \times 10^{-3}s + 5\right)}{s^2 \times (s + 4500)} \tag{34}$$

The Bode diagram of the current compensation link is shown in Figure 11.

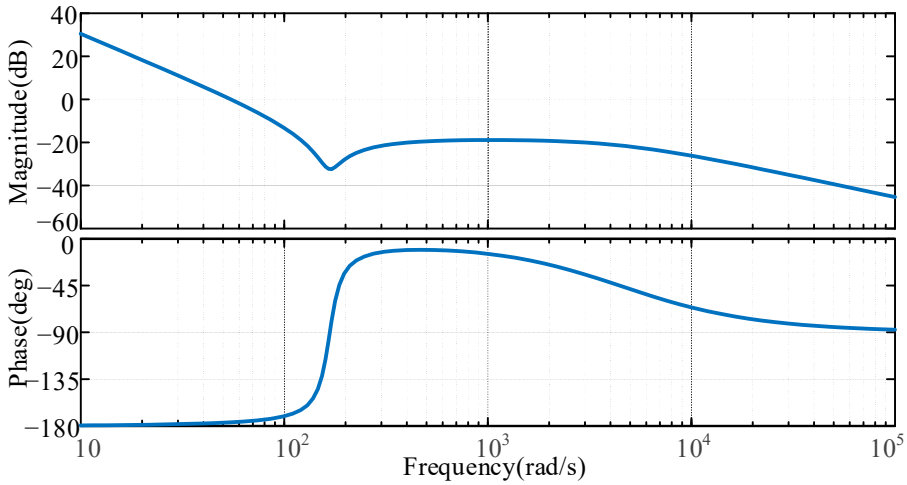


Figure 11. The Bode diagram of the current compensation link.

The open-loop transfer function of the corrected system is shown as.

$$G_{\mathrm{A}}(s) = G_{\mathrm{id}}(s)G_{\mathrm{idc}}(s) = \frac{1.8 \times 10^7}{s(s + 4500)} \tag{35}$$

The open-loop amplitude-frequency characteristic curve of the corrected system is shown in Figure 12. It can be seen from the figure that, after correction, the amplitude-frequency characteristic curve of the corrected system decreases at the slope of 20 dB/dec in the low-frequency band, and the steady-state error of the system is zero; The phase angle margin in the middle-frequency band is 54.2°, which meets the stability requirement.

The crossing frequency is 3.24×10^3rad/s ($f_c \approx 515.7$Hz). The amplitude-frequency characteristic curve of the corrected system decreases at the slope of -40 dB/dec in the high-frequency band, and the system has a good ability to suppress the high-frequency noise. To sum up, the corrected system meets the design requirements.

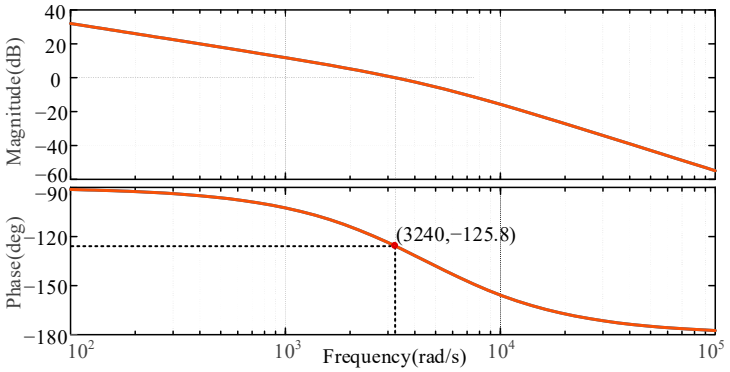


Figure 12. The Bode diagram of the corrected system.

4.3. The Simulation of the Variable Multiplicity Interleaving Bidirectional DC/DC Power Converter

Based on the analysis of the previous chapters, the simulation model is built, and then the parameters in Table 2 are brought into the model. The simulation model is operated to extract the current ripples of different parallel numbers when the duty cycle is 0.25, 0.33, 0.40, and 0.5, which are shown in Figures 13–16 (In each Figure, a is the current ripples in four parallel multiplicities; b is the current ripples in five parallel multiplicities; c is the current ripples in six parallel multiplicities.). Figure 13 shows the output current ripples when the duty cycle is 0.25, and the current ripple is the smallest when the parallel number is four; Figure 14 shows the output current ripples when the duty cycle is 0.33, and the current ripple is the smallest when the parallel number is six; Figure 15 shows the output current ripples when the duty cycle is 0.4, and the current ripple is the smallest when the parallel number is five; Figure 16 shows the output current ripples when the duty cycle is 0.50, and the current ripple is the smallest when the parallel number is six. The above simulation results are consistent with the conclusion in Table 1, which is obtained from the previous analysis, this is when the duty cycle is different, the number of parallel multiplicities with the smallest current ripples is different, and so the DC/DC converter needs to flexibly choose to turn on or turn off some parallel branches according to the current ripple optimization law.

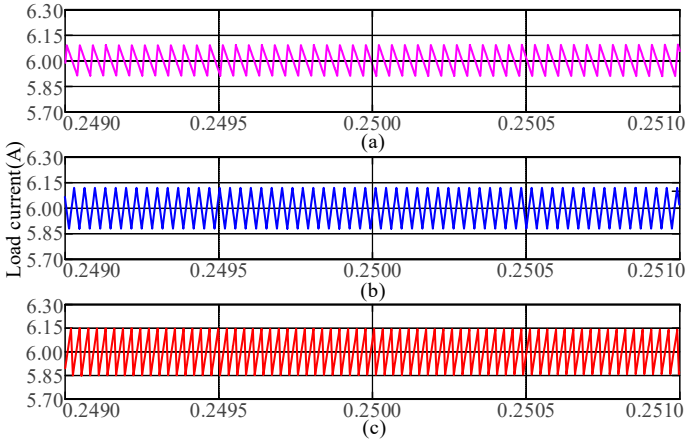


Figure 13. Output current ripples of DC-DC converter with 0.25 duty cycle under the 6A output current. (**a**) The current ripples in four parallel multiplicities; (**b**) The current ripples in five parallel multiplicities; (**c**) The current ripples in six parallel multiplicities.

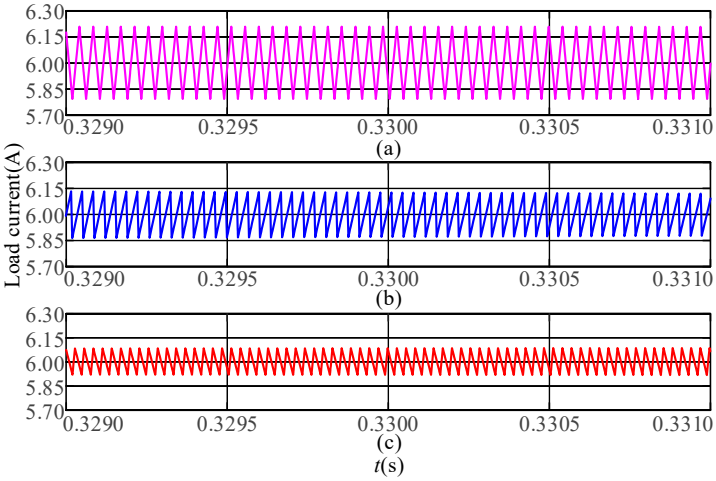


Figure 14. Output current ripples of DC-DC converter with 0.33 duty cycle under the 6A output current. (**a**) The current ripples in four parallel multiplicities; (**b**) The current ripples in five parallel multiplicities; (**c**) The current ripples in six parallel multiplicities.

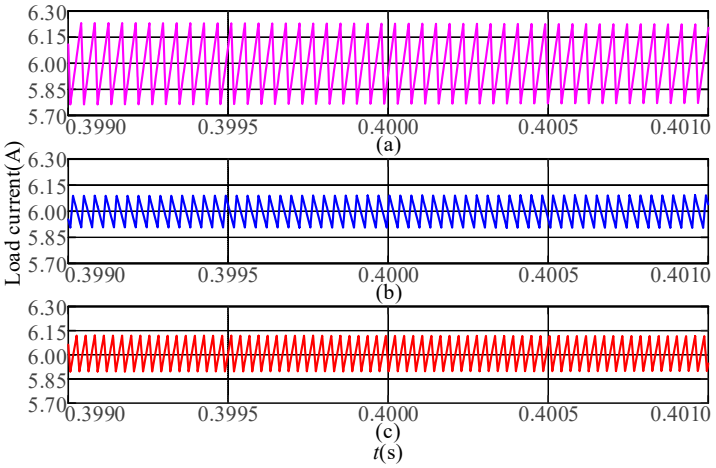


Figure 15. Output current ripples of DC-DC converter with 0.40 duty cycle under the 6A output current. (**a**) The current ripples in four parallel multiplicities; (**b**) The current ripples in five parallel multiplicities; (**c**) The current ripples in six parallel multiplicities.

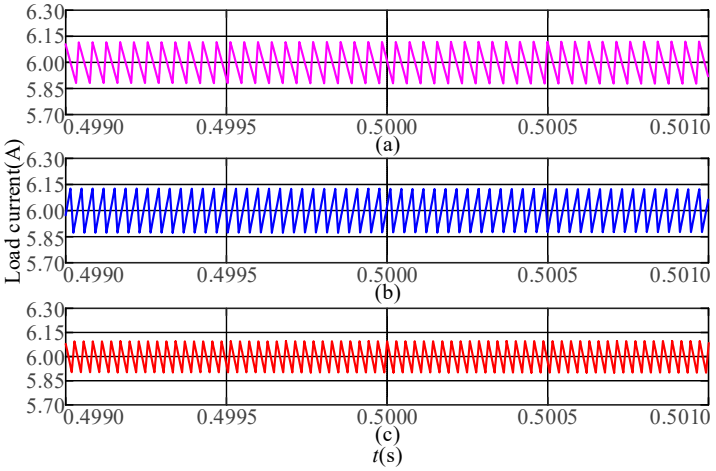


Figure 16. Output current ripples of DC-DC converter with 0.50 duty cycle under the 6A output current. (**a**) The current ripples in four parallel multiplicities; (**b**) The current ripples in five parallel multiplicities; (**c**) The current ripples in six parallel multiplicities.

5. The Experiment and Results

5.1. Experimental Platform

The experimental platform is shown in Figure 17, it can be divided into a control module, power module, output module, power supply, and programmable load. The TMS320F28377 microcontroller is used to control the whole system, and the XC3S500E-PQ208 is used to generate the PWM signal with the specific phase shift angle. The PWM signal is transmitted to the power module through the optical fiber. In the experiment, the 30 V bus voltage is generated by the DC stabilized power supply, the load capacitance C is replaced by a programmable load, the switching frequency is set to 10 KHz, the value of filter inductance is 3 mH, the output current is 6 A.

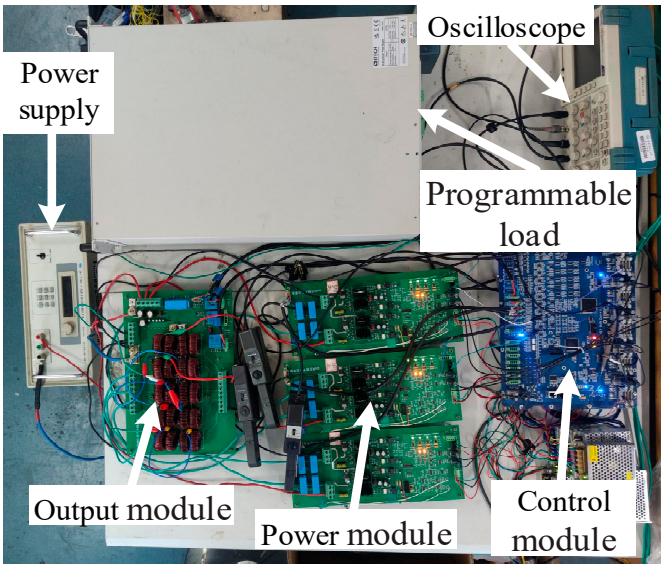


Figure 17. Experimental platform.

5.2. The Experimental Results of the Current Ripple Optimization in Variable Channel Interleaving Bidirectional DC/DC Power Converter

The current ripples of the 6 A output current of the DC-DC converter are shown in Figure 18. Figure 18a–l represents the current ripples which are corresponding to different multiplicities in parallel when the duty cycles are 0.25, 0.33, 0.4, and 0.5, respectively. As can be seen in Figure 18a–c, when the duty cycle is 0.25, the maximum current ripples are 80 mA, 100 mA, and 120 mA when the number of parallel multiplicities is 4, 5, and 6, respectively. As can be seen in Figure 18d–f, when the duty cycle is 0.33, the maximum current ripples are 160 mA, 145 mA, and 65 mA, when the number of parallel multiplicities is 4, 5, and 6, respectively. As can be seen in Figure 18g–y, when the duty cycle is 0.4, the maximum current ripples are 200 mA, 90 mA, and 100 mA, when the number of parallel multiplicities is 4, 5, and 6, respectively. As can be seen in Figure 18j–l, when the duty cycle is 0.5, the maximum current ripples are 130 mA, 140 mA, and 120 mA when the number of parallel multiplicities is 4, 5, and 6, respectively.

All optimization results of current ripples under different duty cycles and parallel multiplicities in Figure 18 are identical to not only the simulation results above but also the analytical results in Table 1, which demonstrate that the optimization method proposed in this paper is precise and practical.

The three pictures of the same line in Figure 18 clearly show the size of the current ripple under a different number of parallel channels with the same duty cycle. By extracting the data in Figure 18, Table 3 can be obtained. Compared with Figure 18, Table 3 is more intuitive and convincing in numerical representation. Table 3 intuitively illustrates the number of parallel branches that should be taken to minimize the current ripple under experimental conditions.

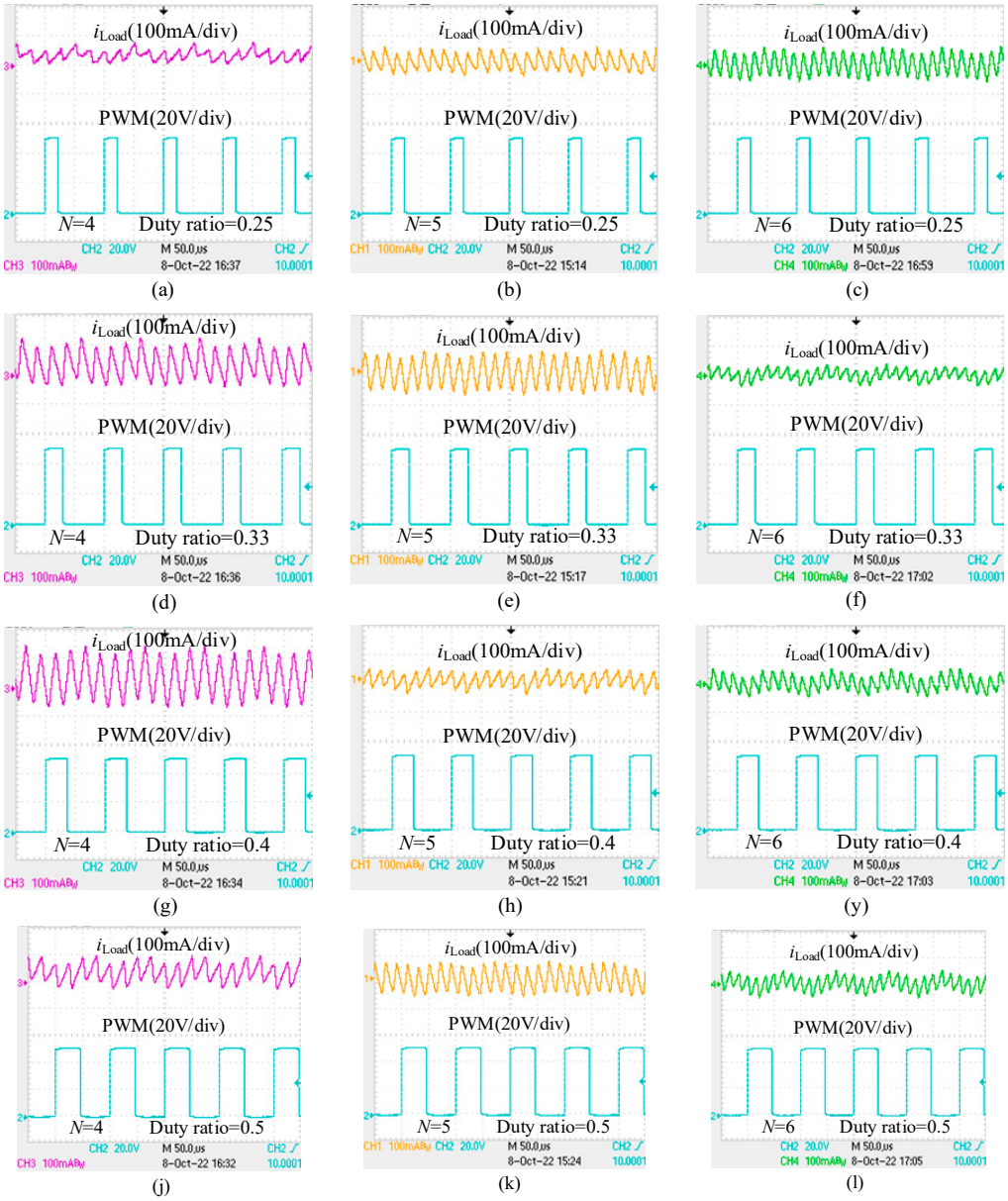


Figure 18. Output current ripples of DC-DC converter with different duty cycles under the same output current. (**a**–**c**) The current ripples of different parallel multiplicities when the duty cycle is 0.25; (**d**–**f**) The current ripples of different parallel multiplicities when the duty cycle is 0.33; (**g**–**y**) The current ripples of different parallel multiplicities when the duty cycle is 0.4; (**j**–**l**) The current ripples of different parallel multiplicities when the duty cycle is 0.5.

Table 3. Output current ripples of DC-DC converter with different duty cycles under the same output current.

Duty Cycles	The Maximum Current Ripple of the Number of *N* Multiple Parallel Channels/mA			The Number of Parallel Channels to Be Used
	N = 4	*N* = 5	*N* = 6	
0.25	80	100	120	4
0.33	160	145	65	6
0.40	200	90	100	5
0.50	130	140	120	6

In order to simplify the analysis process, only the current ripples corresponding to duty cycles 0.25 and 0.5 are adopted. Figure 19a–f shows the current ripples of the first three channels when the parallel multiplicity is 4, 5, and 6. It can be seen that the larger the

duty cycle, the longer the rise time and the shorter the fall time, the peak value of the ripple peak of a single brand is also increasing, and the total output current ripple is composed of multiple brand parallel outputs, so the total output current ripple cannot be judged only by the size of a single brand current ripple. The current of each channel is not completely coincident, mainly due to the measurement error of the sensor. Even if the current sharing control method is taken, the current imbalance caused by the inconsistent parameters of each channel cannot be fully compensated.

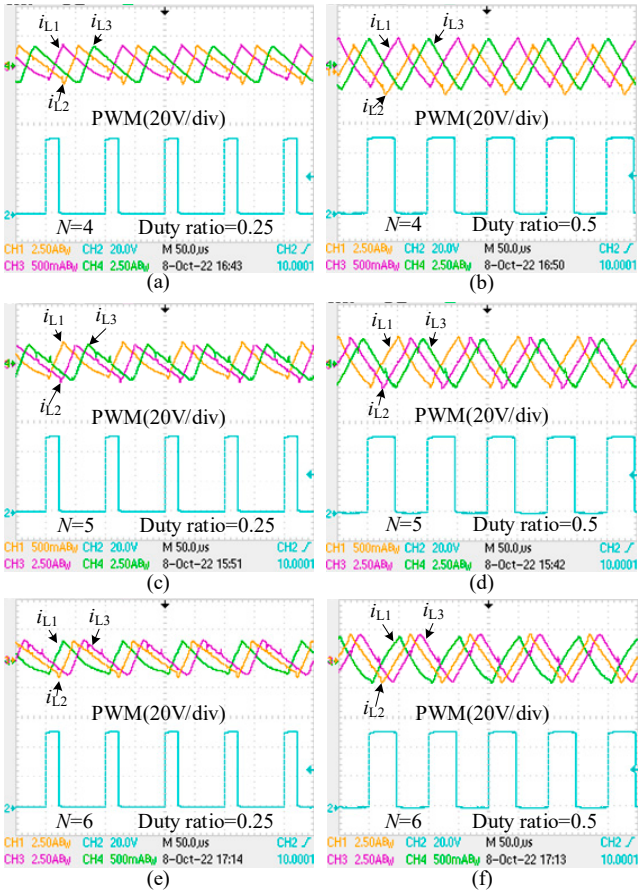


Figure 19. Current ripples of the first three channels under partial duty cycle when the parallel multiplicity is 4, 5, and 6. (**a**,**c**,**e**) The current ripples of the first three channels with the duty cycle of 0.25 when the parallel multiplicity is 4, 5, and 6; (**b**,**d**,**f**) The current ripples of the first three channels with the duty cycle of 0.5 when the parallel multiplicity is 4, 5, and 6.

6. Conclusions

The main contribution of this paper is to propose a variable multiplicity control method of multiple interleaving bidirectional DC/DC power converters to optimize the current ripple, that is, dynamically adjust the number of parallel multiplicities in the actual operation of the circuit according to the duty cycles, so that the output current ripple is as small as possible. First, the relationship between the current ripple and the number of parallel multiplicities and the duty cycle is analyzed and deduced and the switching logic that can generate the minimum current ripple is designed. Second, the average value model and the AC small signal model of variable multiplicity interleaving bidirectional DC/DC power converter are established, and the transfer function of the system is obtained. Third, according to the transfer function of the system, the control system of the converter is designed. Simulation and experimental results show that the control method proposed in this paper can effectively further reduce the current ripple of the traditional multiple DC/DC converter, and to a certain, reduce the switching loss caused by a blind increase of switching frequency to optimize current ripple, so it is of great significance. All in all, the

current ripple optimization algorithm proposed in this paper is suitable for occasions that require low current ripple, such as battery energy storage systems, electric vehicles, etc. However, due to multiple interleaving DC/DC converters using more parallel branches, the cost is relatively high. Further research on improving reliability and reducing costs is needed in the future.

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