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Design of Dual-Notch-Filter-Based Controllers for Enhancing the Dynamic Response of Universal Single-Phase Grid-Connected Power Converters

Sahar Borafker, Pavel Strajnikov and Alon Kuperman *

Applied Energy Laboratory, School of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beer-Sheva 8410501, Israel; sahar37@gmail.com (S.B.); strajnik@post.bgu.ac.il (P.S.)
* Correspondence: alonk@bgu.ac.il; Tel.: +972-8-6461599

Abstract: Trade-off between transient response and grid-side current quality is a well-known issue of single-phase mains-connected power converters. A dual-loop control structure (usually based on PI or type-II controllers) is typically employed in such systems to regulate the DC link voltage to a constant reference (in order to maintain power balance) while forcing the grid-side current to have a specific shape (in order to comply with power quality requirements). Introducing notch term/s (tuned to certain multiple/s of the mains base frequency) into one of the loops allows either for the improvement of the dynamic performance without worsening the total harmonic distortion of grid-side current or for the enhancement of the current quality without impairing the dynamic response. Since the maximum tolerable value of total harmonic distortion is typically imposed by a certain power quality standard, it is desirable to enhance the transient response of the power converter system as much as possible while keeping the total harmonic distortion at the maximum allowed value. However, universal off-grid operating power conversion systems must support both 50 Hz and 60 Hz mains; consequently, tuning the notch term/s to 50 Hz multiple/s would not be sufficient for a 60 Hz mains operation and vice-versa. Consequently, this work examines the possibility of introducing a dual-notch term into the control loop in order to cover both above-mentioned base frequencies. It is demonstrated that under typical base frequency uncertainty values, the performances of dual-notch terms are nearly decoupled so that the term tuned to a 50 Hz frequency (and optionally to its multiples) has nearly no influence at a 60 Hz mains operation and vice-versa. Consequently, the methodology allows for the improvement of the dynamics of universal grid-connected power converters without total harmonic distortion (THD) deterioration. A stability analysis of the proposed control structure is carried out and quantitative design guidelines, allowing for the attainment of an optimized dynamic response for a given maximum tolerable total harmonic distortion, minimum allowed phase margin and a certain base frequency uncertainty, are established. It is shown that a DC link voltage loop bandwidth of 52 Hz may be attained while keeping the grid-side current THD below 5%. Simulations and experimental results support well the proposed design methodology.

Keywords: single-phase grid-connected converter; transient response; total harmonic distortion; notch filter; control system

Citation: Borafker, S.; Strajnikov, P.; Kuperman, A. Design of Dual-Notch-Filter-Based Controllers for Enhancing the Dynamic Response of Universal Single-Phase Grid-Connected Power Converters. *Appl. Sci.* **2023**, *13*, 10144. https://doi.org/10.3390/app131810144

Academic Editors: Minsung Kim and Byeongcheol Han

Received: 8 August 2023
Revised: 3 September 2023
Accepted: 7 September 2023
Published: 8 September 2023

1. Introduction

Mains-interfacing power conversion systems are typically obliged by power quality standards to interchange sinusoidal-shaped current with the utility grid [1–3]. As a result, alternating instantaneous power is exchanged between the two entities, formed by a DC component and a power component pulsating at twice the mains base frequency [4–6]. While the DC component is transferred to/from the load/source in order to carry the energy, the pulsating power constituent should not be allowed to reach the load/source to avoid lifetime reduction and excessive losses [7–9]. Consequently, DC link capacitors are typically employed to compensate instantaneous power mismatch between grid-side and

load/source-side both in steady state and during transients [10–12]. This is accomplished by regulating the average DC link capacitor voltage (reflecting the stored energy) to a constant reference value employing a PI or type-2 compensator [13–16] without counteracting the pulsating power component. As a result, pulsating current flows through the DC link capacitor, giving rise to an uncontrolled DC link voltage ripple [17,18], which is proportional to the total power processed and inversely proportional to the DC link capacitance value and DC link voltage reference value [19,20]. Upon sensing the DC link voltage and feeding it back to the regulation loop, the ripple distorts the grid-side current magnitude reference signal (created by the loop compensator), leading to an increased total harmonic distortion (THD) of utility-side current [21,22]. In order to limit the THD, the gain of DC link voltage loop compensator should be restricted in the vicinity of double the base utility frequency [23], implying a trade-off between AC-side current THD and DC link voltage dynamics in case compensators with monotonically decreasing frequency response characteristics (e.g., PI or type-2) are employed [24–26]. Typically, around 10 Hz DC link voltage loop bandwidth is attained under 5% grid-side current THD restriction. Such a relatively low bandwidth imposes a high value of the required DC link capacitance in order to cope with sharp load-side power variations, since the DC link voltage value should always remain above the maximum of grid-side voltage to retain converter controllability [22,24].

Many solutions aiming to improve the trade-off have been suggested. Utilizing line voltage and/or load current feedforward to compensate against parameter variations does not increase the DC voltage loop bandwidth, yet it requires additional sensors [27–30]. The ripple estimation and cancellation techniques proposed in [31–36] indicated an improved performance, yet requiring a relatively complex circuitry and a significantly increased computational burden. The implementation of approaches based on nonlinear and/or time-varying control proposed in [37–40] call for a high-performance microcontroller. On the other hand, linear filtering-based methods proposed in [41–47] seem to be much simpler in terms of analysis and implementation. In particular, compensators combining a PI or type-II term with a notch filter may be easily realized either digitally or by a simple analog network. As mentioned above, the value of DC link voltage loop gain should be restricted in the vicinity of double the base utility frequency in order to limit the THD. A notch filter was combined with the current loop controller in [48] to enhance transient responses at both the DC bus voltage and the output current. Introducing a notch filter tuned to double the mains base frequency allows for local DC-link voltage loop gain minimization without restricting the corresponding PI or type-II controller gain, thus attaining an increased crossover frequency. Disturbance observer-based approaches, employing notch terms, were shown to yield a similar effect [49,50]. Design guidelines for obtaining PI + Notch controller coefficients based on the maximum tolerable grid-side current THD and transient DC link voltage deviation were established in [51].

Nevertheless, neither of the above-mentioned notch-filter-based solutions took into account the fact that a universal grid-connected converter must be capable of supporting both 50 Hz and 60 Hz grid frequencies. Moreover, utilizing transient DC link voltage deviation may yield non-optimal performance in terms of phase margin "overkill". Recently, a disturbance observer-based approach [50] was extended to employ dual-notch-based action in [52], yet the methodology may only be applied to existing systems with slow PI or type-II controllers and cannot be employed in from-scratch designs. In addition, the control structures of disturbance observer-based methods are quite complex and not easy to implement.

Consequently, the main contributions of this work are as follows:

1. It is suggested to combine a PI term with two notch filters, tuned to 50 Hz and 60 Hz, respectively, in order to support universal grid interfacing without the need for controller redesign.
2. The minimum allowed phase margin is used as the second performance merit (along with the maximum tolerable grid-side current THD) rather than the maximum tolerable transient DC link voltage deviation. Such an approach allows the optimization of

the latter rather than setting a desired value a priori (which may lead to a non-existing solution, requiring further iterations).

An explicit process of deriving coefficients of the proposed PI + N^2 controller employed for regulating the DC-link voltage of single-phase converters interfacing either 50 Hz or 60 Hz mains is proposed in this work. The proposed methodology allows for the optimization of the DC-link voltage transient caused by step-like load changes while attaining prescribed values of grid-side current THD and DC-link voltage loop phase margin under the prescribed mains frequency uncertainty range.

The rest of the paper is organized as follows. The essentials of single-phase grid-connected power conversion system operation are brought forward in Section 2. The steady-state performance of the system in terms of total harmonic distortion and its dynamic response in terms of DC-link voltage deviation upon step-like load variation are revealed analytically in Sections 3 and 4, respectively. Guidelines for the proposed controller coefficient derivation are established in Section 5. The simulations and experiments of the proposed methodology applied to a 500 W grid-connected converter are demonstrated in Section 6. The paper is then concluded in Section 7.

2. Single-Phase Grid-Connected Power Conversion System

Consider a typical dual-stage off-grid operating power conversion system depicted in Figure 1a, formed by a mains-interfacing AC/DC converter and a downstream DC-DC converter, interconnected via a DC link capacitance C_{DC}. The grid is assumed to act as energy source in the subsequent discussion, yet the methodology remains valid in case the energy flows from the DC side to the AC side. Moreover, all the variables below are switching-cycle-average, i.e., free from switching components. Considering harmonic-free mains and unity power factor operation for brevity (yet without loss of generality), the grid-side voltage and current are given by [52]

$$v_G(t) = v_M(t)\sin(\int \omega(t)dt), \quad i_G(t) = i_M(t)\sin(\int \omega(t)dt) \tag{1}$$

with ω denoting the instantaneous base frequency of the grid and v_M, i_M representing the corresponding magnitudes. In steady state, the above quantities are constant so that

$$v_M(t) = V_M, \quad i_M(t) = I_M, \quad \omega(t) = \omega_G. \tag{2}$$

In steady state, the base frequency of the mains may attain the following values,

$$\omega_G = \alpha \cdot \begin{cases} 100\pi, & 50\text{ Hz } mains \\ 120\pi, & 60\text{ Hz } mains \end{cases} \tag{3}$$

with $\alpha \in [\alpha_{\min} < 1, \alpha_{\max} > 1]$ representing the corresponding deviation from nominal values (i.e., $|1-\alpha|$ indicates the corresponding uncertainty). On the other hand, DC-side variables are also constant in steady state so that

$$v_L(t) = V_L, \quad i_L(t) = I_L. \tag{4}$$

Assuming lossless conversion, a functional diagram of the power conversion system is shown in Figure 1b with

$$p_L(t) = v_L(t)i_L(t), \quad p_G(t) = v_G(t)i_G(t), \quad v_{DC}(t)i_{DC}(t) = p_G(t) - p_L(t), \tag{5}$$

where $v_{DC}(t)$ and $i_{DC}(t)$ represent the voltage across the DC link capacitance C_{DC} and the corresponding current, respectively. Combining (1) with (5) yields [10]

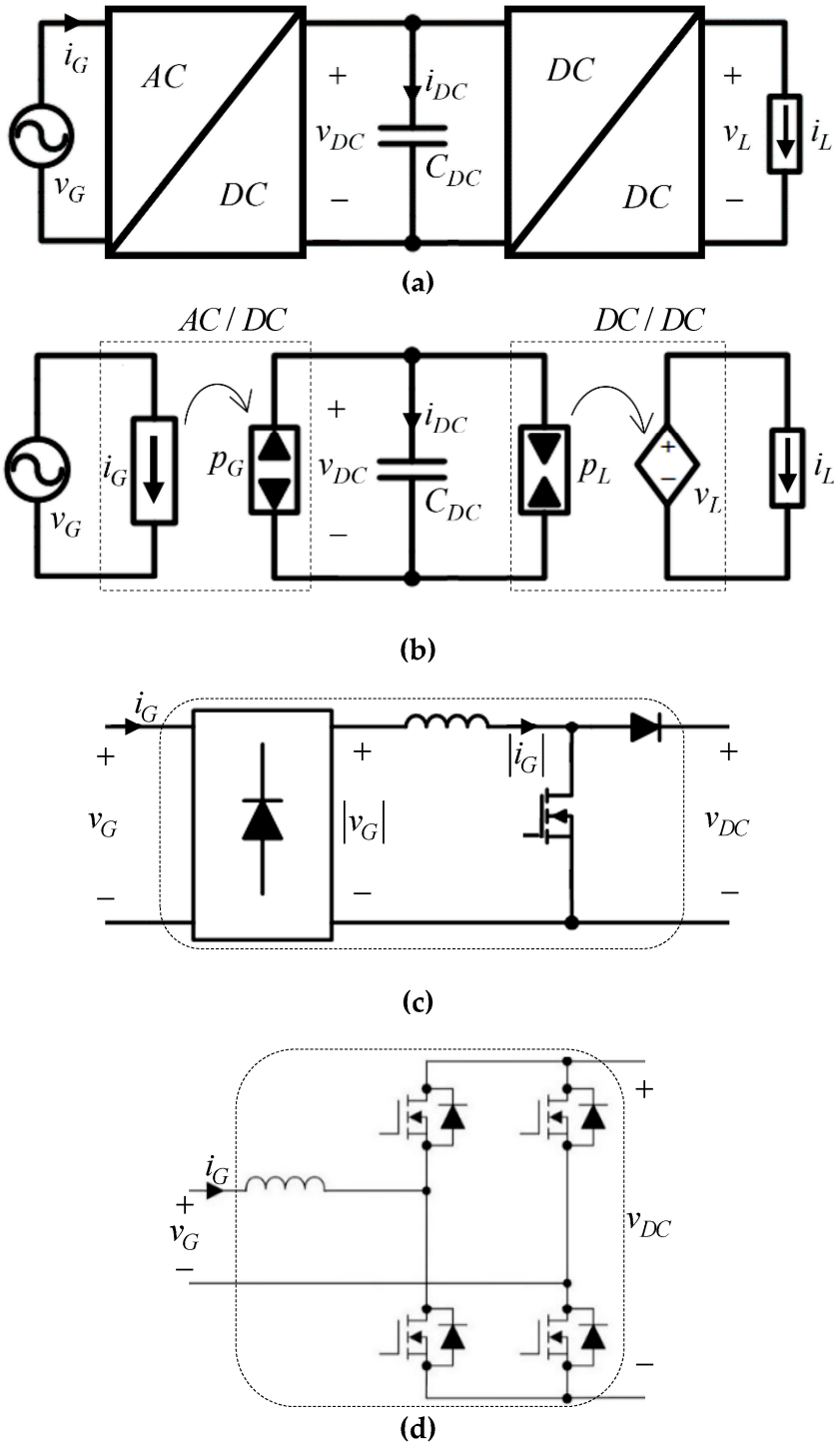

Figure 1. Typical single-phase dual-stage grid-connected power conversion system. (**a**) Generalized topology; (**b**) low-frequency functional diagram; (**c**) bridge-rectifier-based AC/DC converter; (**d**) bridgeless rectifier/inverter.

$$v_{DC}(t)i_{DC}(t) = v_{DC}(t)\underbrace{C_{DC}\frac{dv_{DC}(t)}{dt}}_{i_{DC}(t)} = 0.5v_M(t)i_M(t) - 0.5v_M(t)i_M(t)\cos\left(2\int \omega(t)dt\right) - v_L(t)i_L(t), \quad (6)$$

reducing in steady state to

$$C_{DC} v_{DC}^{ss}(t) \frac{dv_{DC}^{ss}(t)}{dt} = 0.5 V_M I_M - 0.5 V_M I_M \cos(2\omega_G t) - V_L I_L, \quad (7)$$

which may be split into

$$0.5 V_M I_M = V_L I_L \quad (8)$$

and

$$C_{DC} v_{DC}^{ss}(t) \frac{dv_{DC}^{ss}(t)}{dt} = -0.5 V_M I_M \cos(2\omega_G t), \quad (9)$$

respectively. Consequently, the steady-state expressions of grid-side current and DC link voltage are given by

$$I_M = \frac{2P_L}{V_M}, \quad P_L = V_L I_L \quad (10)$$

and

$$v_{DC}^{ss}(t) = V_{DC}^* \sqrt{1 - \frac{P_L}{\omega_G \left(V_{DC}^*\right)^2 C_{DC}} \sin(2\omega_G t)}, \quad (11)$$

respectively, with V_{DC}^* denoting the DC link voltage set point value. In practice,

$$\frac{P_L}{\omega_G \left(V_{DC}^*\right)^2 C_{DC}} << 1 \quad (12)$$

typically holds; hence, (11) may be further reduced to [11]

$$v_{DC}^{ss}(t) \cong V_{DC}^* - \Delta v_{DC}(t), \quad \Delta v_{DC}(t) = \Delta V_{DC} \sin(2\omega_G t), \quad \Delta V_{DC} = \frac{P_L}{2\omega_G V_{DC}^* C_{DC}}. \quad (13)$$

Consequently, steady-state DC link voltage would always be formed by the dominating DC component and the significantly smaller double-base-frequency pulsating ripple component, proportional to the load power and inversely proportional to the DC link capacitance, DC link voltage set point, and base frequency of the mains.

It must be emphasized that two typical realizations of the grid-interfacing AC/DC converter exist in practice. In case of unidirectional AC-to-DC power conversion, a grid-interfacing converter is often realized by a diode bridge rectifier followed by a boost DC-DC converter, as shown in Figure 1c. In case of DC-to-AC energy flow, the grid-interfacing converter operates as an inverter and should be realized in a bridgeless manner, e.g., as shown in Figure 1d. It should be mentioned, however, that unidirectional rectifiers may also be realized by bridgeless topology circuits. The corresponding control structures are depicted in Figure 2. In case a bridge-rectifier-based topology is utilized, all the measurements are taken at the DC side of the converter. The outer (voltage) loop regulates the DC link voltage by feeding the difference between the corresponding set point V_{DC}^* and the measured value v_{DC} into the voltage controller C_V, which calculates the mains current magnitude value I_M^* required to maintain the power balance (cf. (10)). On the other hand, the rectified mains voltage $|v_G|$ is sensed and the corresponding unity magnitude template $\left|sin \int \omega(t) dt\right|$ is extracted and multiplied by I_M^* in order to generate the reference signal for the rectified grid-side current $|i_G|^*$. The inner (current) loop regulates the rectified grid-side current by feeding the difference between the corresponding reference $|i_G|^*$ and the measured value $|i_G|$ into the current controller C_I, which calculates the required modulating signal. The output of the PWM modulator is then fed to the switch of the boost DC-DC converter (cf. Figure 1c).

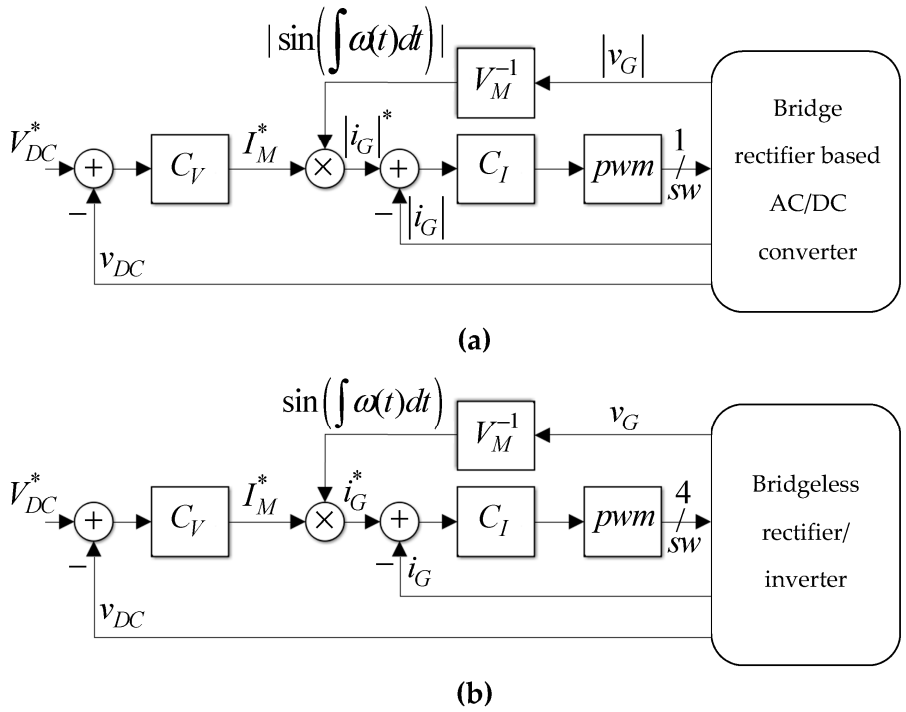

Figure 2. Typical dual-loop control structures for (**a**) a bridge-rectifier-based AC/DC converter, and (**b**) a bridgeless rectifier/inverter.

In case a bridgeless topology is utilized, grid-side measurements are required. While the outer (voltage) loop is similar to that of the bridge-rectifier-based topology, here the mains voltage v_G is sensed and the corresponding unity magnitude template $sin \int \omega(t)dt$ is extracted and multiplied by I_M^* in order to generate the reference signal for the grid-side current i_G^*. The inner (current) loop regulates the grid-side current by feeding the difference between the corresponding reference i_G^* and the measured value i_G into the current controller C_I, which calculates the required modulating signal. The outputs of the PWM modulator are then fed to the switches of the AC/DC converter (cf. Figure 1d).

It was shown in [53] that the attainable bandwidth ω_{CI} of a typical current loop is given by

$$\omega_{CI} \cong \frac{0.5\pi - PM_I^*}{T_d}, \tag{14}$$

where PM_I^* is the desired phase margin of the current loop and T_d is the total switching and sampling delay, the worst case of which equals 1.5 times the sampling period. Considering the typical values of $PM_I^* = \frac{\pi}{4}$ and switching frequency of 50 kHz, the attainable current loop bandwidth would be $2\pi{\cdot}4167$ rad/s, which is about two decades higher than the attainable voltage loop bandwidth. Consequently, it may be assumed that

$$i_G(t) = i_G^*(t), \quad |i_G(t)| = |i_G(t)|^* \tag{15}$$

with a high degree of accuracy. Noticing that

$$v_G(t)i_G(t) = |v_G(t)||i_G(t)| = p_G(t). \tag{16}$$

holds for (1) and combining (15) with (6) while taking Figures 1b and 2 into account, the corresponding simplified closed-loop system representations are depicted in Figure 3 [51].

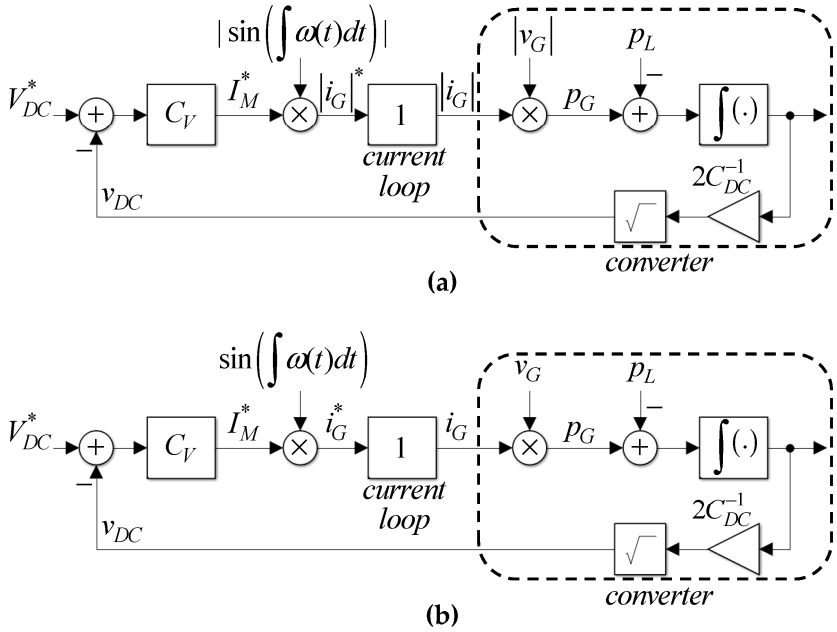

Figure 3. Simplified control structures for (**a**) a bridge-rectifier-based AC/DC converter; and (**b**) a bridgeless rectifier/inverter.

In this paper, the controller C_V is realized by a cascaded proportional-integral–dual-notch (PI + N^2) structure

$$C_V(s) = \underbrace{K\frac{\tau s+1}{s}}_{PI(s)} \cdot \underbrace{\underbrace{\frac{s^2+(200\pi)^2}{s^2+2\xi_f(200\pi)s+(200\pi)^2}}_{NF_1(s)} \cdot \underbrace{\frac{s^2+(240\pi)^2}{s^2+2\xi_f(240\pi)s+(240\pi)^2}}_{NF_2(s)}}_{N^2(s)} \tag{17}$$

with $0 \leq \xi_f \leq 1$, proposed by the authors in [54]. There are three parameters to be determined (namely K, τ and ξ_f) according to the desired phase margin of the voltage loop PM_V^*, the maximum tolerable total harmonic distortion value THD^* and the expected deviation of base frequencies from their nominal values α.

3. Total Harmonic Distortion

According to (10), (13) and Figure 3, there is

$$I_M^* = \frac{2P_L}{V_M} - \Delta V_{DC}|C_V(2\omega_G)|\sin(2\omega_G t + \arg C_V(2\omega_G)) \tag{18}$$

in steady state. Consequently (cf. (15)), there is

$$|i_G(t)| = I_M^*|\sin\omega_G t| = \frac{2P_L}{V_M}\left(1 - \frac{V_M\Delta V_{DC}}{2P_L}|C_V(2\omega_G)|\sin(2\omega_G t + \arg C_V(2\omega_G))\right)|\sin\omega_G t| \tag{19}$$

in case of a diode bridge-based rectifier. If

$$\frac{V_M\Delta V_{DC}}{2P_L}|C_V(2\omega_G)| << 1 \tag{20}$$

then (19) implies grid current [51]

$$\begin{aligned} i_G(t) &= \frac{2P_L}{V_M}\left(1-\frac{V_M\Delta V_{DC}}{2P_L}|C_V(2\omega_G)|\sin(2\omega_G t+\arg C_V(2\omega_G))\right)\sin\omega_G t \\ &= \frac{2P_L}{V_M}\begin{pmatrix} \sin\omega_G t+\frac{V_M\Delta V_{DC}}{4P_L}|C_V(2\omega_G)|\cos(\omega_G t+\arg C_V(2\omega_G))- \\ -\frac{V_M\Delta V_{DC}}{4P_L}|C_V(2\omega_G)|\sin(3\omega_G t+\arg C_V(2\omega_G)) \end{pmatrix}, \end{aligned} \tag{21}$$

formed by the first and the third harmonic components only. Note that (21) also holds in the case of bridgeless grid-interfacing converter implementation. Consequently, the grid-side current THD is given by (cf. (20))

$$THD \cong \frac{V_M\Delta V_{DC}}{4P_L}|C_V(2\omega_G)|. \tag{22}$$

Furthermore, (20) may be reformulated as

$$2\cdot THD << 1, \tag{23}$$

which is typically true since THD values of 5% and below are typically considered. Hence, (20) is justified and (21) is a valid approximation.

It may be concluded from (21) that the pulsating ripple component of the DC link voltage (13) imposes a non-zero grid-side current THD. Denoting the maximum tolerable THD value as *THD**, the combination of (13) and (21) yields the following constraint

$$\frac{V_M}{8\omega_G V_{DC}^* C_{DC}}|C_V(2\omega_G)| = THD^* \Rightarrow |C_V(2\omega_G)| = \frac{4(2\omega_G)V_{DC}^* C_{DC}}{V_M}THD^*, \tag{24}$$

which must be satisfied within the region given by the following union (cf. (3))

$$(2\alpha_{\min}\cdot 100\pi \le 2\omega_G \le 2\alpha_{\max}\cdot 100\pi)\cup(2\alpha_{\min}\cdot 120\pi \le 2\omega_G \le 2\alpha_{\max}\cdot 120\pi). \tag{25}$$

Considering (23) with (17) yields

$$\begin{aligned} &K\frac{\sqrt{(2\omega_G\tau)^2+1}}{2\omega_G}\times \\ &\frac{(200\pi)^2-(2\omega_G)^2}{\sqrt{\left((200\pi)^2-(2\omega_G)^2\right)^2+\left(4\omega_G\xi_f(200\pi)\right)^2}}\frac{(240\pi)^2-(2\omega_G)^2}{\sqrt{\left((240\pi)^2-(2\omega_G)^2\right)^2+\left(4\omega_G\xi_f(240\pi)\right)^2}} \\ &= \frac{4(2\omega_G)V_{DC}^* C_{DC}}{V_M}THD^*. \end{aligned} \tag{26}$$

Combining (26) with (3) leads to

$$\begin{aligned} &K\frac{\sqrt{(2\omega_G\tau)^2+1}}{2\omega_G}\times \\ &\frac{1}{\sqrt{1+4\xi_f^2\frac{\alpha^2}{(1-\alpha^2)^2}}}\frac{1}{\sqrt{1+4\xi_f^2\frac{\left(\frac{5}{6}\alpha\right)^2}{\left(1-\left(\frac{5}{6}\alpha\right)^2\right)^2}}} = \frac{4(2\omega_G)V_{DC}^* C_{DC}}{V_M}THD^*, \quad \omega_G = \alpha 100\pi \\ &K\frac{\sqrt{(2\omega_G\tau)^2+1}}{2\omega_G}\times \\ &\frac{1}{\sqrt{1+4\xi_f^2\frac{\alpha^2}{(1-\alpha^2)^2}}}\frac{1}{\sqrt{1+4\xi_f^2\frac{\left(\frac{6}{5}\alpha\right)^2}{\left(1-\left(\frac{6}{5}\alpha\right)^2\right)^2}}} = \frac{4(2\omega_G)V_{DC}^* C_{DC}}{V_M}THD^*, \quad \omega_G = \alpha 120\pi \end{aligned} \tag{27}$$

unified as

$$K\frac{\sqrt{(2\omega_G\tau)^2+1}}{2\omega_G}f(\alpha)=\frac{4(2\omega_G)V_{DC}^{*}C_{DC}}{V_M}THD^{*} \tag{28}$$

with

$$f(\alpha)=\frac{1}{\sqrt{1+4\xi_f^2\frac{\alpha^2}{(1-\alpha^2)^2}}}\cdot\begin{cases}\dfrac{1}{\sqrt{1+4\xi_f^2\frac{\left(\frac{5}{6}\alpha\right)^2}{\left(1-\left(\frac{5}{6}\alpha\right)^2\right)^2}}}, & \omega_G=\alpha 100\pi\\ \dfrac{1}{\sqrt{1+4\xi_f^2\frac{\left(\frac{6}{5}\alpha\right)^2}{\left(1-\left(\frac{6}{5}\alpha\right)^2\right)^2}}}, & \omega_G=\alpha 120\pi\end{cases} \tag{29}$$

denoting the multiplication of tuned and un-tuned notch term gains, respectively. Plots of $f(\alpha)$ versus $0.99\le\alpha\le 1.01$ (signifying 1% mains frequency uncertainty) are depicted in Figure 4 for different values of ξ_f. As expected, the gain of the notch term is zero at nominal frequency (theoretically implying $THD=0$), increasing with detuning. Moreover, the highest total $f(\alpha)$ is attained at $\alpha_{\min}$ for 50 Hz mains and at $\alpha_{\max}$ for 60 Hz mains. Nevertheless, since the magnitude response of the PI term in (17) monotonically decreases until the effect zero begins to kick in, the gain at $\omega_G=\alpha_{\min}\cdot 100\pi$ may be expected as the worst case one. In addition, it is well-evident that increasing ξ_f improves robustness to frequency variations. It should be emphasized that if $\xi_f=0$ is selected, the control structure in (17) reduces to the typical PI regulator.

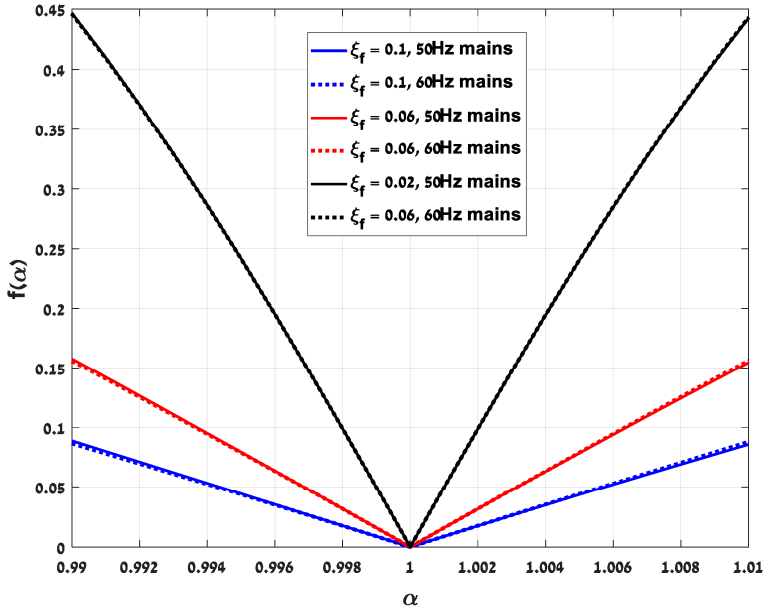

Figure 4. Plots of $f(\alpha)$ for different base frequencies and values of ξ_f.

4. Dynamic Response

Reformulating (6) as

$$C_{DC}v_{DC}(t)\frac{dv_{DC}(t)}{dt}=0.5v_M(t)i_M(t)-p_L(t)-\underbrace{0.5v_M(t)i_M(t)\cos\left(2\int\omega(t)dt\right)}_{p_2(t)} \tag{30}$$

and linearizing around the operating point by substituting

$$\begin{gathered}v_{DC}(t)=V_{DC}^{*}+\tilde{v}_{DC}(t),\quad i_M(t)=\tfrac{2P_L}{V_M}+\tilde{i}_M(t),\quad v_M(t)=V_M+\tilde{v}_M(t),\\ p_L(t)=P_L+\tilde{p}_L(t),\quad p_2(t)=P_L\cos(2\omega_G t)+\tilde{p}_2(t),\end{gathered} \tag{31}$$

into (31) and neglecting high-order small-signal terms yields

$$C_{DC}V_{DC}^{*}\frac{d\widetilde{v}_{DC}(t)}{dt} = 0.5V_M\widetilde{i}_M(t) + \frac{P_L}{V_M}\widetilde{v}_M(t) - \widetilde{p}_L(t) - \widetilde{p}_2(t). \tag{32}$$

The resultant control structure is depicted in Figure 5 [22].

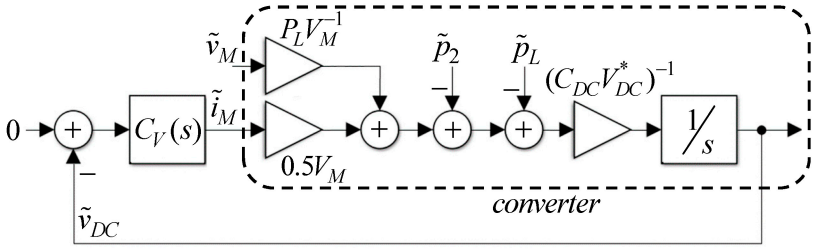

Figure 5. Linearized simplified control structure.

The corresponding loop gain is obtained as

$$\begin{aligned} L(s) = \frac{0.5V_M}{C_{DC}V_{DC}^{*}s}C_V(s) = \\ \frac{0.5V_MK}{C_{DC}V_{DC}^{*}}\frac{\tau s+1}{s^2}\frac{s^2+(200\pi)^2}{s^2+2\xi_f(200\pi)s+(200\pi)^2}\frac{s^2+(240\pi)^2}{s^2+2\xi_f(240\pi)s+(240\pi)^2} = \\ \omega_n^2\frac{2\frac{\xi_n}{\omega_n}s+1}{s^2}NF_1(s)NF_2(s), \quad \omega_n = \sqrt{\frac{0.5KV_M}{C_{DC}V_{DC}^{*}}}, \quad \xi_n = \omega_n\frac{\tau}{2}. \end{aligned} \tag{33}$$

Denoting the crossover frequency of the voltage loop as ω_{CV}, the corresponding phase and gain contributions of the notch terms are given by

$$\begin{aligned} &\arg NF_1(\omega_{CV}) = -\tan^{-1}\left(\frac{2\xi_f}{\frac{200\pi}{\omega_{CV}}-\frac{\omega_{CV}}{200\pi}}\right), \quad \arg NF_2(\omega_{CV}) = -\tan^{-1}\left(\frac{2\xi_f}{\frac{240\pi}{\omega_{CV}}-\frac{\omega_{CV}}{240\pi}}\right), \\ &|NF_1(\omega_{CV})| = \sqrt{\frac{1}{1+\frac{4\xi_f^2}{\left(\frac{200\pi}{\omega_{CV}}-\frac{\omega_{CV}}{200\pi}\right)^2}}}, \quad |NF_2(\omega_{CV})| = \sqrt{\frac{1}{1+\frac{4\xi_f^2}{\left(\frac{240\pi}{\omega_{CV}}-\frac{\omega_{CV}}{240\pi}\right)^2}}}, \end{aligned} \tag{34}$$

respectively. The Bode diagram of dual-notch term $NF_1(s)\cdot NF_2(s)$ is depicted in Figure 6 for different values of ξ_f and $\omega < 200\pi$ (since $\omega_{CV} < 200\pi$ in practice). It is well-evident that increasing the value of ξ_f escalates both the phase and gain contributions of the dual-notch term.

It is well-evident that the gain contribution may be neglected within the whole frequency range considered, thus

$$|L(\omega_{CV})| \cong \frac{\omega_n^2}{\omega_{CV}^2}\sqrt{\left(2\xi_n\frac{\omega_{CV}}{\omega_n}\right)+1} = 1 \tag{35}$$

should be satisfied at the crossover frequency ω_{CV}, yielding the crossover frequency

$$\omega_{CV} = \underbrace{\xi_n\sqrt{2+2\sqrt{1+\frac{1}{4\xi_n^4}}}}_{\theta_n}\omega_n = \theta_n\omega_n. \tag{36}$$

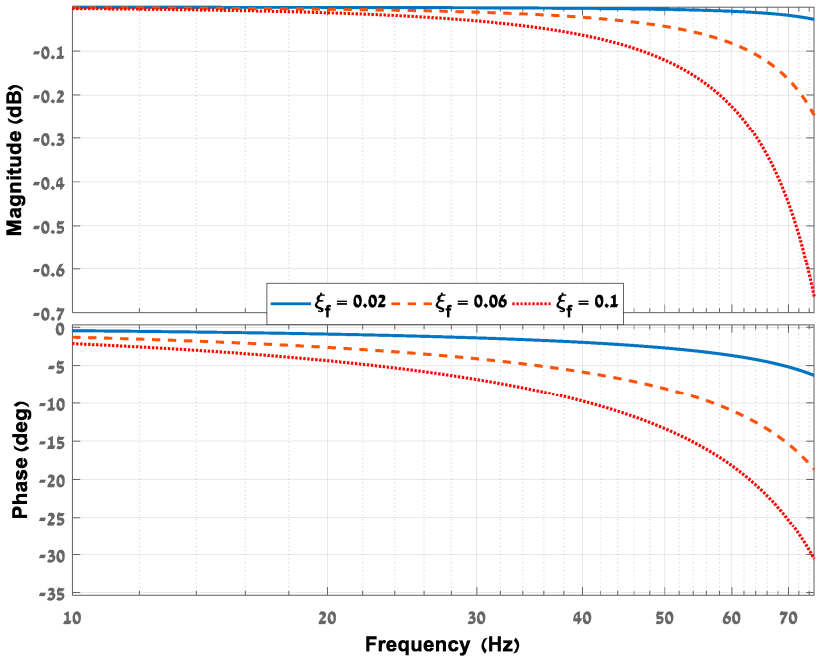

Figure 6. Bode diagram of dual-notch term $NF_1(s)\cdot NF_2(s)$ for different ξ_f values.

On the other hand, the phase contribution in (34) must be taken into account, imposing

$$\begin{aligned}&\arg\left(L(\omega_{CV})\right)=\\&tg^{-1}\left(2\xi_n\frac{\omega_{CV}}{\omega_n}\right)-\tan^{-1}\left(\frac{2\xi_f}{\frac{200\pi}{\omega_{CV}}-\frac{\omega_{CV}}{200\pi}}\right)-\tan^{-1}\left(\frac{2\xi_f}{\frac{240\pi}{\omega_{CV}}-\frac{\omega_{CV}}{240\pi}}\right)-\pi=-\pi+PM_V^*\end{aligned}\tag{37}$$

at the crossover frequency with PM_V^* indicating the desired voltage loop phase margin. Solving (37) with (36), there is

$$\xi_n=\left(\frac{\left(\frac{tg\left(PM_V^*+\beta\right)}{2\sqrt{2}}\right)^4}{2\left(\frac{tg\left(PM_V^*+\beta\right)}{2\sqrt{2}}\right)^2+\frac{1}{4}}\right)^{\frac{1}{4}},\quad \beta=\tan^{-1}\left(\frac{2\xi_f}{\frac{200\pi}{\omega_{CV}}-\frac{\omega_{CV}}{200\pi}}\right)+\tan^{-1}\left(\frac{2\xi_f}{\frac{240\pi}{\omega_{CV}}-\frac{\omega_{CV}}{240\pi}}\right).\tag{38}$$

Note that β in (38) may be approximated for simplicity (with some safety margin) as

$$\beta\cong 2\tan^{-1}\left(\frac{2\xi_f}{\frac{200\pi}{\omega_{CV}}-\frac{\omega_{CV}}{200\pi}}\right),\tag{39}$$

hence, in order to minimize it, ξ_f should satisfy

$$\xi_f<<\frac{1}{2}\left(\frac{200\pi}{\omega_{CV}}-\frac{\omega_{CV}}{200\pi}\right).\tag{40}$$

Setting ξ_f to

$$\xi_f=\frac{1}{2}\lambda\left(\frac{200\pi}{\omega_{CV}}-\frac{\omega_{CV}}{200\pi}\right),\tag{41}$$

and substituting into (39), there is

$$\beta\cong 2\tan^{-1}(\lambda)\approx 2\lambda,\quad \lambda<<1.\tag{42}$$

In order to bound β by $\beta_{\max}$ degrees, λ should be set to

$$\lambda = \frac{1}{2}\tan(\beta_{\max}) \tag{43}$$

and PM_V^* increased by $\beta_{\max}$ degrees to compensate for β. For the value of $\beta_{\max} = 5°$ recommended in [51], $\lambda = 0.0437$ should be selected. In case ξ_f is bounded according to (40), ξ_n and θ_n are presented graphically versus the typical range of the desired voltage loop phase margin values in Figures 7 and 8, respectively. It may be concluded that both parameters increase with the rise in PM_V^*. In addition, the crossover frequency ω_{CV} is always higher than ω_n for the practical values of the desired voltage loop phase margin.

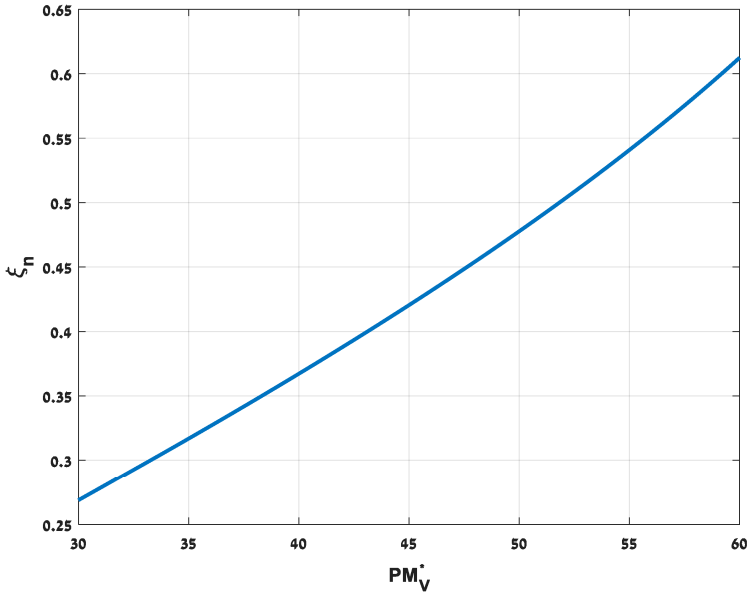

Figure 7. Graphical representation of ξ_n versus the desired voltage loop phase margin.

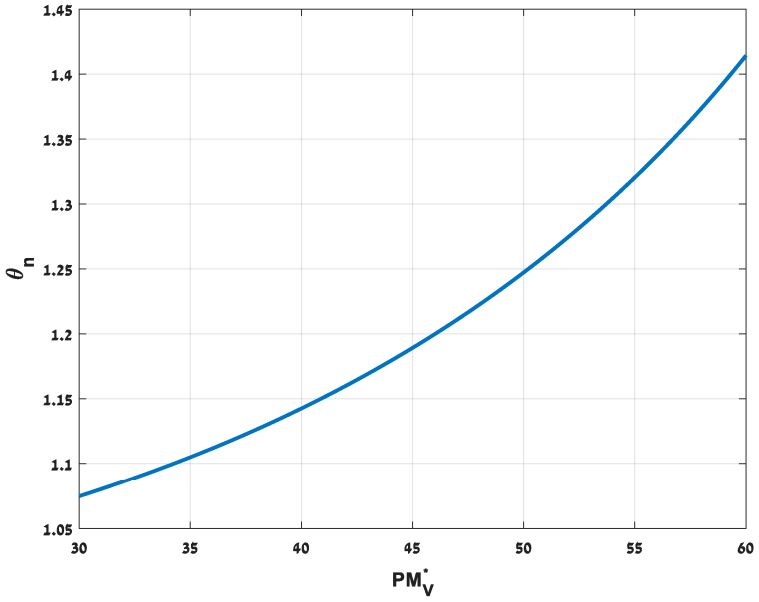

Figure 8. Graphical representation of θ_n versus the desired voltage loop phase margin.

In practice, the variations of grid voltage magnitude and frequency are slower with respect to the voltage loop time constant. Consequently, a critical transient response is the

one caused by load power variations. The corresponding transfer function of interest may be derived from Figure 5 (neglecting the influence of the dual notch term) as

$$\left.\frac{\widetilde{v}_{DC}(s)}{\widetilde{p}_L(s)}\right|_{p_2(t)=0} \approx -G_n \frac{s}{s^2+2\xi_n\omega_n s+\omega_n^2}, \quad G_n = \frac{1}{C_{DC}V_{DC}^*}. \tag{44}$$

Therefore, the load power step of ΔP_L imposes a DC link voltage perturbation expressed as

$$\widetilde{v}_{DC}(s)|_{p_2(s)=0} = -\frac{G_n\Delta P_L}{s^2+2\xi_n\omega_n s+\omega_n^2} \Rightarrow \widetilde{v}_{DC}(t)|_{p_2(t)=0} = -\frac{G_n\Delta P_L}{\omega_n\sqrt{1-\xi_n^2}}e^{-\xi_n\omega_n t}\sin\left(\omega_n\sqrt{1-\xi_n^2}t\right). \tag{45}$$

On the other hand, the contribution of $p_2(t)$ is given by $\Delta v_{DC}(t)$ in (13). Consequently, the total DC link voltage deviation may be approximated by

$$\begin{aligned}&\widetilde{v}_{DC}(t) = \widetilde{v}_{DC}(t)|_{p_2(t)=0} + \Delta v_{DC}(t) = \\ &-\frac{G_n\Delta P_L}{\omega_n\sqrt{1-\xi_n^2}}e^{-\xi_n\omega_n t}\sin\left(\omega_n\sqrt{1-\xi_n^2}t\right) - \frac{\Delta P_L}{2\omega_G V_{DC}^* C_{DC}}\sin(2\omega_G t),\end{aligned} \tag{46}$$

bounded by

$$\begin{aligned}&\widetilde{v}_{DC}(t) = v_{DC}(t) - V_{DC}^* \geq \\ &\max\left(\widetilde{v}_{DC}(t)|_{p_2(t)=0}\right) + \max(\Delta v_{DC}(t)) = -\frac{\Delta P_L}{V_{DC}^* C_{DC}}\left(\frac{1}{\omega_n}e^{-\frac{\xi_n\cos^{-1}\xi_n}{\sqrt{1-\xi_n^2}}} + \frac{1}{2\omega_G}\right).\end{aligned} \tag{47}$$

Since the value of ξ_n is dictated solely by $PM_V^* + \beta_{\max}$ (cf. (38)), the total DC link voltage deviation is reduced when ω_n is increased. Since ω_n is proportional to ω_{CV} (cf. (37)) for a given PM_V^*, increasing ω_n is equivalent to increasing the voltage loop bandwidth. Moreover, the right-hand side within the brackets of (46) implies that $\omega_G = \alpha_{\min}\cdot 100\pi$ would also be the worst case in terms of contribution to the DC link voltage deviation. It should be recalled that in an earlier work [51], the desired undershoot value rather than the minimal tolerable phase margin was used as a performance merit, yielding excessive stability at the expense of a larger DC link voltage overshoot. Here, a minimal tolerable phase margin is imposed, yielding an improved DC link voltage undershoot, as shown next.

5. Controller Parameters Selection

Combining (28) with (33) and solving while considering the worst-case grid frequency $\omega_G = \alpha_{\min}\cdot 100\pi$ yields

$$\omega_n = \sqrt{8}\xi_n\alpha_{\min}100\pi\sqrt{\sqrt{1+\frac{(THD^*)^2}{\xi_n^4 f^2(\alpha_{\min})}}-1}. \tag{48}$$

with

$$f(\alpha_{\min}) = \frac{1}{\sqrt{1+4\xi_f^2\frac{\alpha_{\min}^2}{\left(1-\alpha_{\min}^2\right)^2}}}\frac{1}{\sqrt{1+4\xi_f^2\frac{\left(\frac{5}{6}\alpha_{\min}\right)^2}{\left(1-\left(\frac{5}{6}\alpha_{\min}\right)^2\right)^2}}}. \tag{49}$$

As mentioned at the end of the preceding section, ω_n should be maximized in order to optimize the transient response (i.e., minimize the DC link voltage deviation). According to (43), this implies minimizing the value of $f(\alpha)$ since ξ_n is dictated solely by $PM_V^* + \beta_{\max}$. However, this conclusion contradicts the one drawn in Section 3, where the opposite was required in order to improve the steady-state performance. Consequently, the trade-off between steady-state and dynamic performances remains and the proposed methodology

aims to improve it but not eliminate it. According to (36) and (48), the crossover frequency is then given by

$$\omega_{CV} = \theta_n \sqrt{8} \xi_n \alpha_{\min} 100\pi \sqrt{\sqrt{1 + \frac{(THD^*)^2}{\xi_n^4 f^2(\alpha_{\min})}} - 1}. \tag{50}$$

Substituting (50) into (41) and rearranging, there is

$$\xi_f = \frac{1}{2}\lambda \left(\frac{1}{\theta_n \sqrt{2} \xi_n \alpha_{\min} \sqrt{\sqrt{1+\frac{(THD^*)^2}{\xi_n^4 f^2(\alpha_{\min})}} - 1}} - \theta_n \sqrt{2} \xi_n \alpha_{\min} \sqrt{\sqrt{1 + \frac{(THD^*)^2}{\xi_n^4 f^2(\alpha_{\min})}} - 1} \right). \tag{51}$$

Since θ_n and ξ_n are known from (36) and (38), solving (51) with (49) yields the value of ξ_f. Then, ω_n is obtained from (48) and the coefficients of the PI controller term in (17) are obtained as (cf. (33))

$$K = \frac{2C_{DC}V_{DC}^*}{V_M}\omega_n^2, \quad \tau = 2\frac{\xi_n}{\omega_n}. \tag{52}$$

The proposed process of controller coefficient tuning is then summarized as follows:

1. Initialize $\beta_{\max}$ and PM_V^*.
2. Obtain θ_n using (36), ξ_n using (38) and λ using (43).
3. Initialize THD^* and α_{min}.
4. Obtain ξ_f using (51) and ω_n using (48).
5. Initialize V_M, C_{DC} and V_{DC}^*.
6. Determine K and τ using (52).
7. Verify the design by Bode diagram.
8. Release requirement/s and iterate if necessary.

6. Example and Validation

Consider a bidirectional 500 W single-phase grid-connected converter shown in Figure 9 (the downstream DC-DC converter is represented by the power load element p_L [55]) operating at a switching frequency of 30 kHz with L = 3.5 mH. The value of the DC link capacitance was set to C_{DC} = 385 µF [22] and the DC link voltage set point was selected as V_{DC}^* = 400 V [51]. The desired performance merit pair was selected as THD^* = 0.05, PM_V^* = 40°. The grid frequency uncertainty was assumed to be 1%, i.e., $\alpha \in [\alpha_{\min} = 0.99, \alpha_{\max} = 1.01]$ were considered for both 50 Hz and 60 Hz mains and the corresponding magnitude was set to V_M = 325 V. According to the process of controller coefficient tuning proposed in the previous section:

1. β = 7.5° and PM_V^* = 40° + 7.5°.
2. θ_n = 1.2, ξ_n = 0.45 and λ = 0.066.
3. THD^* = 0.05 and α_{min} = 0.99.
4. ξ_f = 0.047 and ω_n = 2π·45 rad/s.
5. V_M = 325 V, C_{DC} = 385 µF and V_{DC}^* = 400 V.
6. K = 76 and τ = 0.0032.

The resulting Bode diagram of the DC link voltage loop gain (cf. (33)) is depicted in Figure 10, indicating a crossover frequency of ω_{CV} = 2π·52 rad/s and a phase margin of 39.2° in accurate agreement with PM_V^* = 40°.

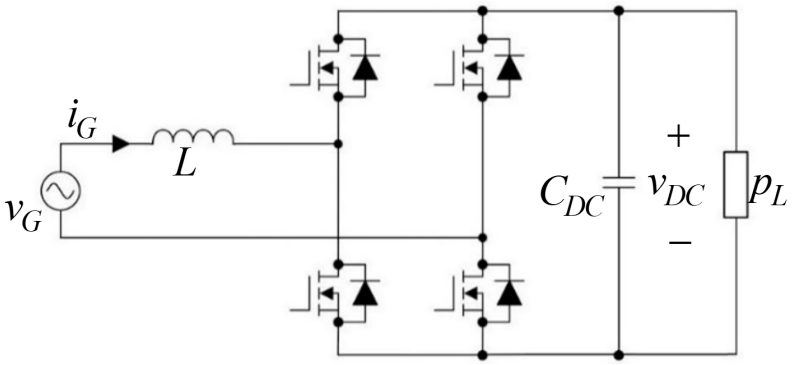

Figure 9. Grid-interfacing converter under study.

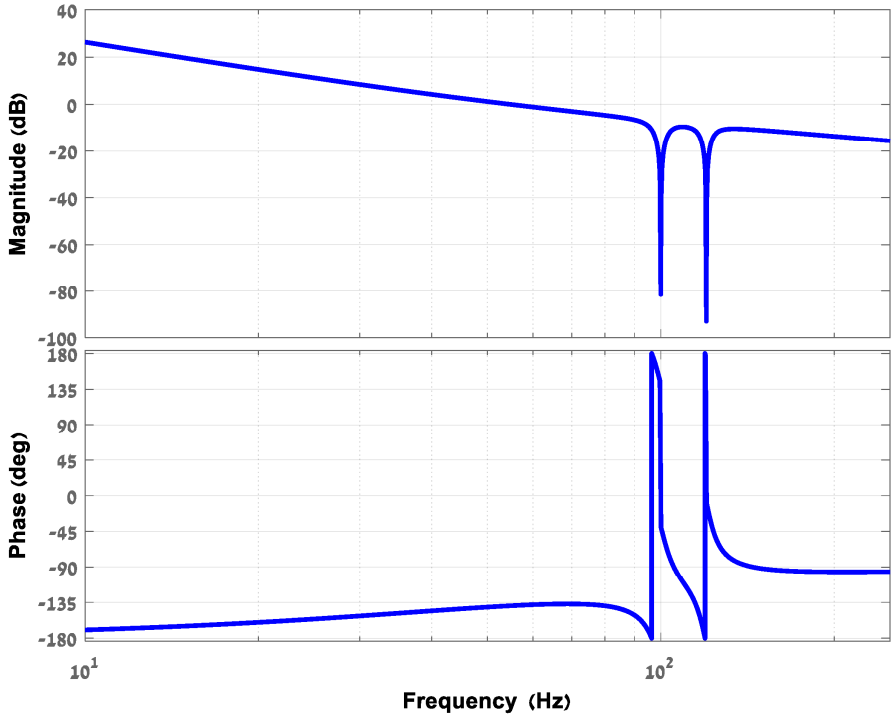

Figure 10. Bode diagram of the DC link voltage loop.

It is interesting to compare the expected performance to the one demonstrated in [51]. Here, voltage deviation of ~10 V is expected (cf. (47)) under a 40° phase margin. On the other hand, a DC link deviation of 20 V was attained in [51] under a 58° phase margin. It may be then concluded that imposing a minimal tolerable phase margin yields an optimized DC link voltage deviation, as stated at the end of Section 4.

6.1. Simulations

During simulations (PSIM 2022 software), the transient responses of the DC link voltage and grid-side current to a zero-to-rated power step-like load variation, and the corresponding steady-state performance under the proposed control methodology were evaluated. The results are depicted in Figures 11 and 12 for 50 Hz and 60 Hz mains, respectively.

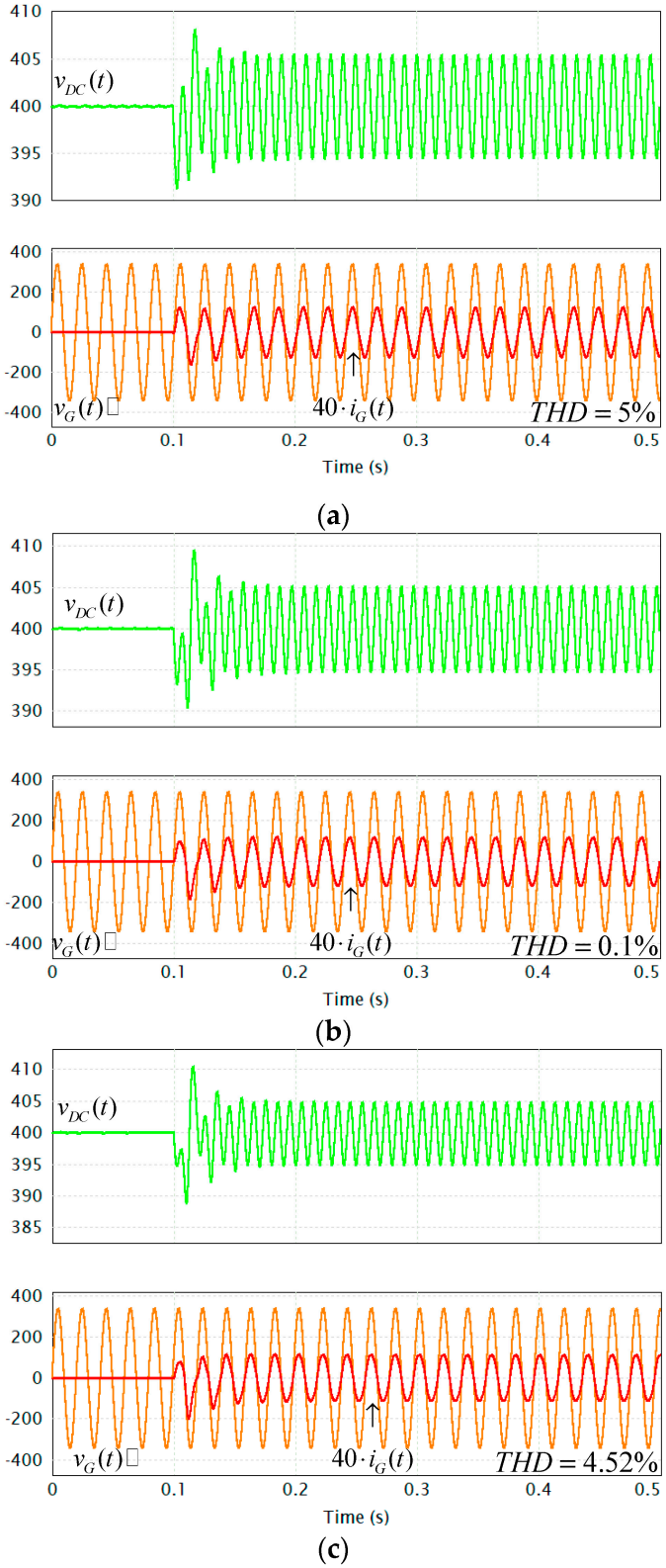

Figure 11. Simulation results, 50 Hz mains. DC link voltage and grid-side current response to 100% load increase at 50 ms for (**a**) $\omega_G = 2\pi \cdot 49.5$ rad/s; (**b**) $\omega_G = 2\pi \cdot 50$ rad/s; and (**c**) $\omega_G = 2\pi \cdot 50.5$ rad/s.

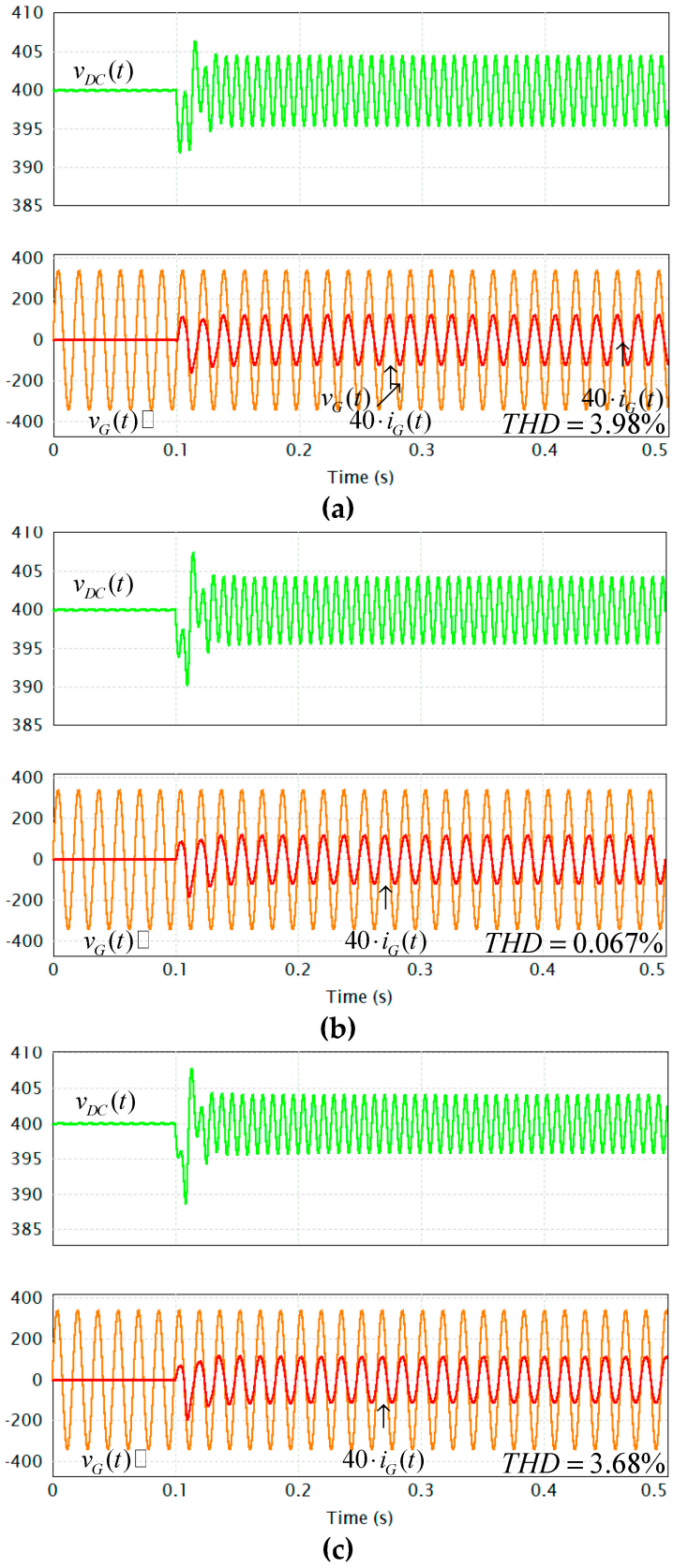

Figure 12. Simulation results, 60 Hz mains. DC link voltage response to load increase for (**a**) $\omega_G = 2\pi \cdot 59.4$ rad/s; (**b**) $\omega_G = 2\pi \cdot 60$ rad/s; and (**c**) $\omega_G = 2\pi \cdot 60.6$ rad/s.

It may be concluded that the system operates as expected under the proposed methodology in terms of dynamic response (a ~10 V DC link voltage deviation is evident irrespectively of mains frequency). As to the grid-side current quality, Table 1 summarizes the corresponding steady-state THD values. It is evident that the system designed according to the proposed approach complies well with THD^* at $\omega_G = \alpha_{\min} \cdot 100\pi$. Moreover, the THD attains near-zero values at the nominal values of the mains frequency, as predicted above.

Table 1. PSIM-measured THD in simulations.

$\omega_G/2\pi$	49.5 Hz	50 Hz	50.5 Hz	59.4 Hz	60 Hz	60.6 Hz
THD%	5	0.1	4.52	3.98	0.067	3.68

6.2. Experiments

In order to validate the proposed methodology experimentally, a modified Texas Instruments High Voltage Single Phase Inverter Kit [56] (Figure 13) was utilized.

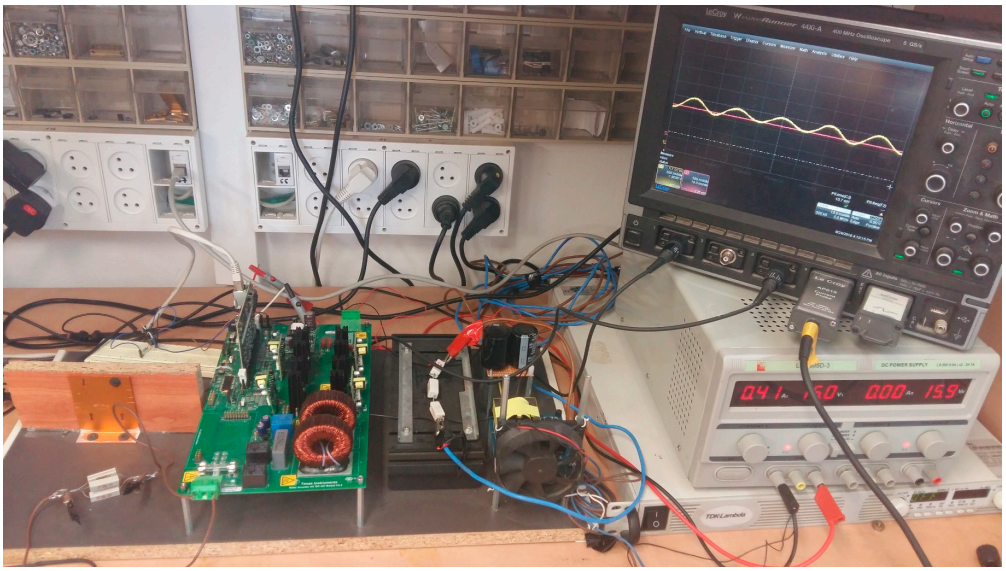

Figure 13. Texas Instruments High Voltage Single Phase Inverter Development Kit.

The control algorithm was realized adopting first-order hold digitization [57] by a TMS320F28335 DSP-based control card under an average-current-controlled inner loop. The utility was emulated by an APS-7100 Gw Instek programmable AC power source operating as 50 Hz/60 Hz ± 1%, 230V_{rms} sinusoidal voltage source. The M9715B Maynuo DC electronic load functioning in constant power mode was employed to emulate the power load p_L (cf. Figure 9).

During the simulation framework, it was shown that frequency variations have a negligible influence on the shape of transient responses; hence, the latter were recorded for nominal mains frequency values only. The corresponding results are depicted in Figure 14, matching well the corresponding simulation results demonstrating ~10 V DC link deviations upon a step-like load variation.

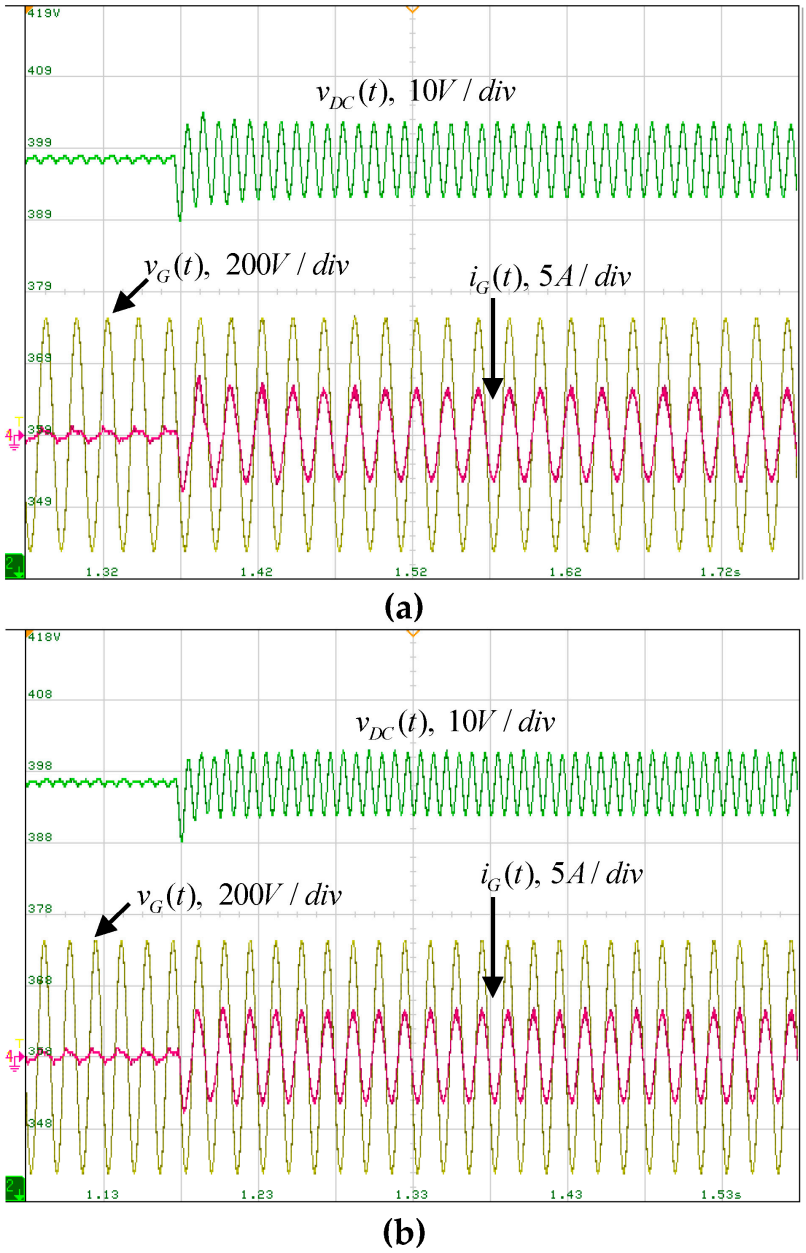

Figure 14. Experimental results. DC link voltage response to load increase for (**a**) $\omega_G = 2\pi \cdot 50$ rad/s, and (**b**) $\omega_G = 2\pi \cdot 60$ rad/s.

The steady-state performance under a rated load around 50 Hz and 60 Hz mains is demonstrated in Figures 15 and 16, respectively. Prior to the experimental framework, the AC power source voltage THD was measured and found to be 0.5%, as shown in Figure 9 in [22]. This value should be taken into account in order to correctly interpret the measured values of THD_i. Table 2 summarizes the corresponding steady-state THD values. It is evident that the system designed according to the proposed approach complies well with THD^*.

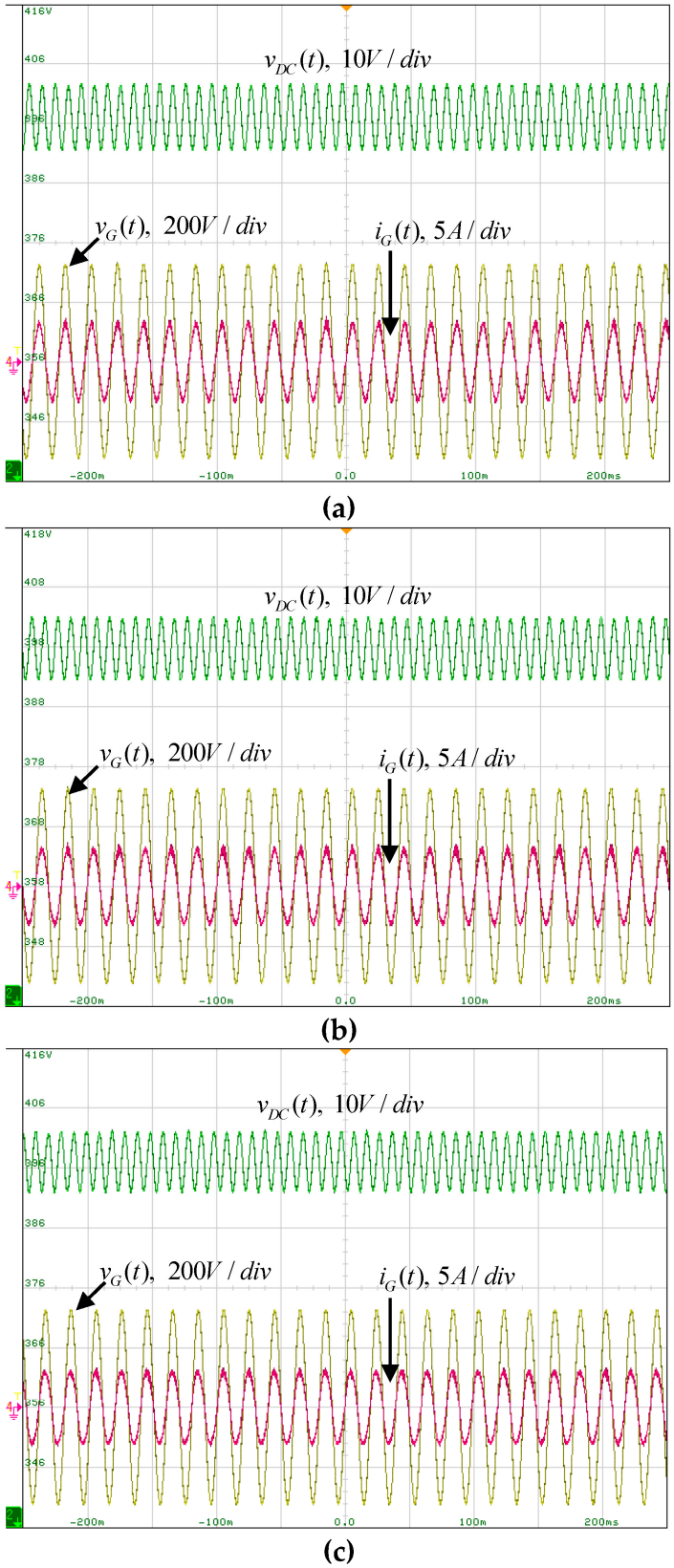

Figure 15. Experimental results, 50 Hz mains. Steady-state performance under (**a**) $\omega_G = 2\pi \cdot 49.5$ rad/s; (**b**) $\omega_G = 2\pi \cdot 50$ rad/s; and (**c**) $\omega_G = 2\pi \cdot 50.5$ rad/s.

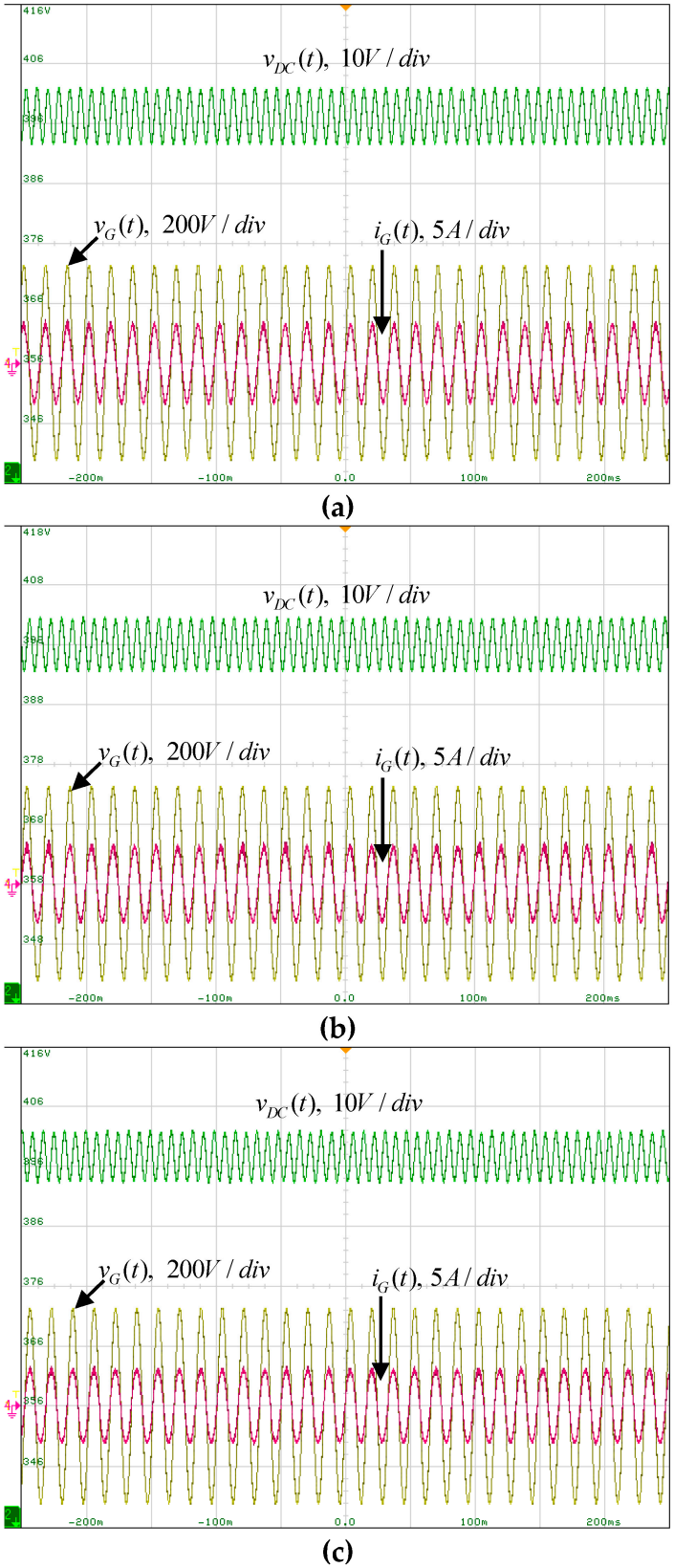

Figure 16. Experimental results, 60 Hz mains. Steady-state performance under (**a**) $\omega_G = 2\pi \cdot 59.4$ rad/s; (**b**) $\omega_G = 2\pi \cdot 60$ rad/s; and (**c**) $\omega_G = 2\pi \cdot 60.6$ rad/s.

Table 2. Scope-measured THD in experiments.

$\omega_G/2\pi$	49.5 Hz	50 Hz	50.5 Hz	59.4 Hz	60 Hz	60.6 Hz
THD	0.0535	0.0261	0.053	0.0528	0.0212	0.046

7. Conclusions

A method for deriving the coefficients of a proportional-integral and dual-notch controller employed for regulating the DC link voltage of single-phase converters interfacing either 50 Hz or 60 Hz mains was proposed in this work. The suggested approach allows for the optimization of the DC link voltage transient caused by step-like load changes while attaining the prescribed values of the grid-side current total harmonic distortion and the DC link voltage loop phase margin under a certain uncertainty range of mains frequency. An explicit process of controller coefficient tuning was established and successfully validated both by simulations and experimentally. It was shown that the 50 Hz and 60 Hz notch terms are nearly decoupled in frequency domain, allowing the proposed methodology to attain an approximate 5-fold increase in the DC link voltage loop crossover frequency compared to the classical PI control under a 5% grid-side current THD restriction, a 45° phase margin and a 1% grid frequency uncertainty. Future work on the subject will focus on distorted grid interfacing (calling for multi-dual-notch-based control structure) and examining the advantages of replacing the PI term of the controller with a type-II regulator. It is expected that the additional degree of freedom inherent in the type-II regulator may further improve the trade-off between steady-state and transient converter behavior. Moreover, multi-dual-notch-based control structures may give rise to stability issues which must be identified and appropriately resolved.

Author Contributions: Conceptualization, S.B. and A.K.; methodology, P.S. and A.K.; validation, S.B. and P.S.; formal analysis, A.K.; investigation, S.B. and P.S.; resources, A.K.; writing—original draft preparation, S.B.; writing—review and editing, A.K.; supervision, A.K.; project administration, A.K.; funding acquisition, A.K. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded in part by the Israel Science Foundation, grant number 2186/19, and by the Israel Innovation Authority.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this article.

Conflicts of Interest: The authors declare no conflict of interest.

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