applied sciences

MDPI

Supplementary Material:

Investigating the Device Performance Variation of a Buried Locally Gated Al/Al_2O_3 Graphene Field-Effect Transistor Process

Tzu-Jung Huang [1], Adheesh Ankolekar [2], Anibal Pacheco-Sanchez [3] and Ivan Puchades [2,*]

[1] Department of Microsystems Engineering, Rochester Institute of Technology, Rochester, NY 14623 USA; txh9958@rit.edu
[2] Department of Electrical and Microelectronic Engineering, Rochester Institute of Technology, Rochester, NY 14623 USA; ava9684@rit.edu
[3] Departament d'Enginyeria Electrònica, Escola d'Enginyeria, Universitat Autònoma de Barcelona, Bellaterra, Spain; anibaluriel.pacheco@uab.cat
* Correspondence: ivan.puchades@rit.edu; Tel.: +1-585-475-7294

Figure S1a shows the distriution of the measure VDirac. Figure S1b shows the hole mmobility as calculated using $\mu = gm/(W/L \times V_{ch} \times C_{ox})$, where gm is point of maximum trans-conductance of the I_{DS}-V_{GS} curves shown in **Error! Reference source not found.**b. *W* is the width of the transistor, *L* the length, and *Cox* is the capacitance per unit area of the gate dielectric. As a first approximation to characterize the entire batch of devices of this technology, the mobility was calculated with $V_{ch} = V_{DS}$, without taking into account the contact resistance. The average and standard deviation for the mobility are 457.97 cm^2/Vs and 110.35 cm^2/Vs, with a non-uniformity of 93%. Figure S1 shows that the values obtained are not normally distributed, as such it is justified to use the value of non-uniformity as a figure of merit to assess variability.

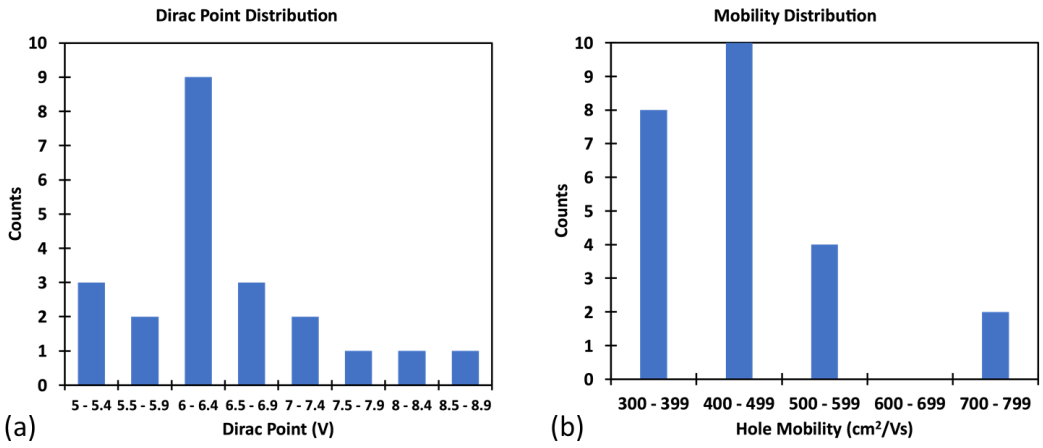

Figure S1. (a) Dirac point voltage and (**b**) mobility distribution of 24 identical devices.

Figure S2a shows the transfer curve of 3 identical dimension sampling devices for Raman spectrum and SEM imaging analysis. Gate voltage was swept one way from -10 V to 10 V and drain was biased constant at 1 V. Current level of the devices were characterized at

max current level at V_{GS} = -10 V. Figure S2b shows the Raman spectra measured on graphene on copper foil prior to transfer to make sure only a monolayer of graphene is present on the transfer host.

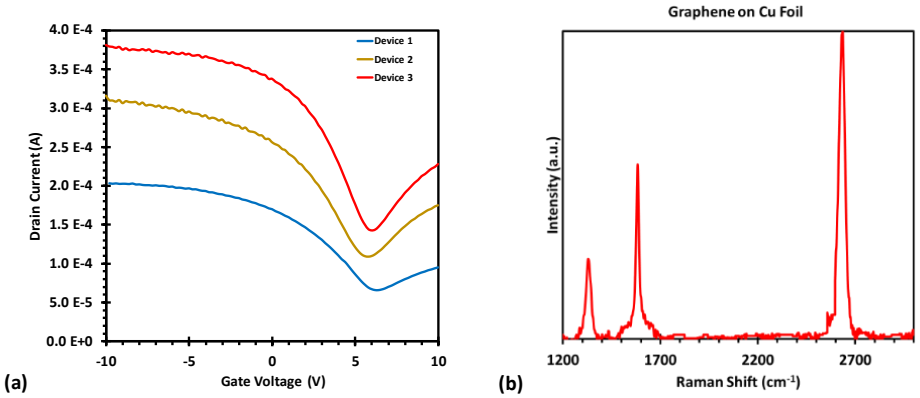

Figure S2. (**a**) Overlay of I_DV_G characteristics of Device 1(blue), Device 2(yellow), and Device 3 (red) representing low, medium, and high current sample devices (**b**) Raman spectra of graphene on 20 μm copper foil from Graphenea, Inc. prior to transfer.

Defect separation (L_D) was calculated from Eq. 1 for the area of graphene in interest. Laser energy (E_{633nm}) for a red 633 nm laser was calculated to be 1.96 eV, and can be used directly when calculating both defect density (n_D) as well as defect separation in Eq. 1 and 2 [70] by plugging in the maximum intensity for D ($Count_{D\_peak}$) and G ($Count_{G\_peak}$) peak. Constant values presented in Eq.1 and Eq.2 are model fit with the calculated laser energy, the value may be used for the defect density calculation illustrated below in Eq. 2 for the graphene on the gate electrode (Al_2O_3/Al stack), graphene at the edge of gate electrode and graphene on the Al_2O_3/SiO_2 interface. The I_D and I_G in Eq. 1 and Eq. 2 show the intensity peak of D and G of the Raman spectrum.

$$(L_D)^2 = \frac{[(4.3\pm1.3)\times10^3]}{(E_{633\ nm})^4}\left(\frac{Count_{D\_peak}}{Count_{G\_peak}}\right)^{-1} \quad \textbf{Eq. 1}$$

$$n_D = [(7.3 \pm 2.2) \times 10^9](E_{633\ nm})^4\left(\frac{Count_{D\_peak}}{Count_{G\_peak}}\right) \quad \textbf{Eq. 2}$$

The approximated number of transferred layers can be obtained by calculating the 2D-band to G-band intensity ratio. The approximation was used to determine whether the final transfer sample is a single layer graphene, bilayer, or multilayer (bulk) material. Raman spectroscopy analysis was also conducted on graphene on Cu supplied by Graphenea, Inc. Raman spectra suggests the baseline of the graphene material prior to transfer. 2D/G ratio of the spectra demonstrates a pristine monolayer graphene was indeed on the starting substrate. Identical 2D/G ratio can also be found in Trace C in **Error! Reference source not found.** (b), (d), and (f) that show a perfect and pristine single layer with respect to the supplied data. No D peak was observed in the starting sample because a first-order D peak cannot be visible in a pristine graphene due to its crystal symmetries [71].

Table S1. Average defect separation and density of each inspected sample.

Location	Parameter	Device 1		Device 2		Device 3	
		High	Low	High	Low	High	Low
On Gate	L_D (nm)	33.24	24.33	30.89	22.61	30.35	22.21
	n_D	2.4 E+10	1.3 E+10	5.6 E+10	3 E+10	5.78 E+10	3.1 E+10
Edge of Gate	L_D (nm)	37.10	27.16	44.95	32.90	23.65	17.31
	n_D	3.9 E+10	2.1 E+10	2.6 E+10	1.4 E+10	9.5 E+10	5.1 E+10
S/G Gap	L_D (nm)	61.18	44.78	55.93	40.93	54.55	39.93
	n_D	1.4 E+10	7.6 E+09	1.7 E+10	9.1 E+09	1.8 E+10	9.6 E+09

Defect density and average defect separation analysis were carried out based on the D/G peak ratio. Listed in Table S1 is the calculated defect density (n_D) and separation (L_D) based on Eq. 1 and Eq. 2 at three different regions on three separate dies. High and low in Table S1 displays the estimated range of the calculated defect density and defect separation. It can be observed that the defect distance for both Raman spectrum collected on the gate and edge of gate are significantly lower in comparison to the S/G Gap, or graphene on Al_2O_3/SiO_2; moreover, the defect density (n_D) is consistent across the board where a much higher defect density is obtained at areas that are not Al_2O_3/SiO_2. This again suggests the uneven Al gate surface may be a key hindering factor to the electrical results apart from contact resistance. All SEM images Figure 5 show a roughened Al gate surface which may lead to the electric field concentrating at certain points, as well as unwanted roughness at the graphene-substrate interface that may induce scattering effects which reduce mobility. Raman spectroscopy verifies the existence of graphene in all analyzed devices.

Tables S2, S3 and S4 show the results of the impact of traps on the variation and non-uniformity of the fabricated buried top gated graphene FETs, forward and backward V_{GS} sweeps with a staircase scheme and different bias stress conditions prior to the acquisition of the measurement data were performed. Analysis for a low, high and medium devices, are presented here while the analysis of an additional high current device is presented in Table 1.

Table S2. Extracted parameters of a low max I_{DS} (</=200 μA) sample device for contact resistance, mobility, and density of carriers at Dirac point for a device from this technology.

Measurement Condition	$R_{c,p}$ (kΩ)	$\mu_{0,p}$ (cm^2/Vs)	$R_{c,n}$ (kΩ)	$\mu_{0,n}$ (cm^2/Vs)	n_0 (cm^{-2})
No pulse (forward)	4.19	315	5.39	445	4.48 E12
No pulse (reverse)	4.29	525	4.65	605	3.38 E12
Pulse 0 V (forward)	4.21	380	5.38	525	3.49 E12
Pulse 0 V (reverse)	4.29	493	4.67	545	3.17 E12
Pulse -10 V (forward)	4.31	372	5.10	452	3.58 E12
Pulse -10 V (reverse)	4.31	372	5.10	462	3.58 E12

Table S3. Extracted parameters of a medium max I_{DS} (>275 μA) sample device for contact resistance, mobility, and density of carriers at Dirac point for a device from this technology.

Measurement Condition	$R_{c,p}$ (kΩ)	$\mu_{0,p}$ (cm^2/Vs)	$R_{c,n}$ (kΩ)	$\mu_{0,n}$ (cm^2/Vs)	n_0 (cm^{-2})
No pulse (forward)	4.58	209	7.68	519	5.29 E12
No pulse (reverse)	4.89	395	--	--	3.58 E12
Pulse 0 V (forward)	4.58	199	6.69	314	5.09 E12
Pulse 0 V (reverse)	4.79	249	4.80	288	5.01 E12
Pulse -10 V (forward)	4.58	203	6.68	333	5.08 E12
Pulse -10 V (reverse)	4.89	225	6.28	314	5.02 E12

Table S4. Extracted parameters of a high max I_{DS} (>350 μA) sample device for contact resistance, mobility, and density of carriers at Dirac point for a device from this technology.

Measurement Condition	$R_{c,p}$ (kΩ)	$\mu_{0,p}$ (cm^2/Vs)	$R_{c,n}$ (kΩ)	$\mu_{0,n}$ (cm^2/Vs)	n_0 (cm^{-2})
No pulse (forward)	2.18	283	5.08	633	3.79 E12
No pulse (reverse)	2.28	382	--	--	3.45 E12
Pulse 0 V (forward)	2.05	273	4.01	403	3.59 E12
Pulse 0 V (reverse)	2.19	353	2.39	357	3.58 E12
Pulse -10 V (forward)	2.25	313	4.18	463	3.19 E12
Pulse -10 V (reverse)	2.25	283	4.08	450	3.78 E12

Figure S3 shows the result of GFET without gate bias. A linear-like IV curve crossing through origin demonstrates a near ohmic contact between Ni/Au metal stack and graphene.

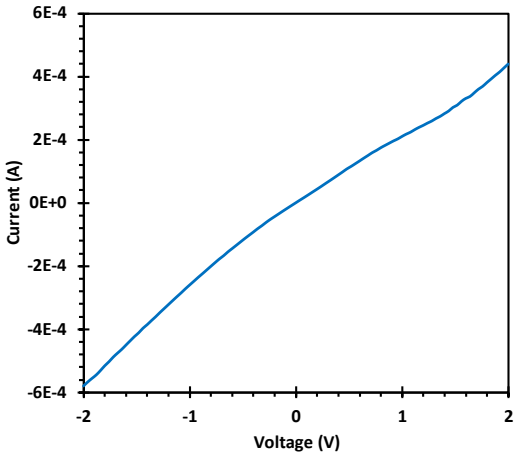

Figure S3. IV curve of fabricated GFET without gate bias for ohmic behavior observation.

Figure S4 (a) and (b) illustrate I_DV_G curve of back gated pristine graphene devices on thermally grown SiO_2 substrate. Devices with identical structure and dimension were investigated for commercially fabricated Graphenea GFET-S10 sample and RIT Nanofab fabricated shown in Figure S4 (a) and (b), respectively. Size of device tested here is significantly larger than the ones focused in this published work. These devices have a channel width of 100 µm and channel length of 80 µm. For commercially fabricated S-10 chip, measured hole and electron mobilities are 544.73 cm^2/Vs and 719.08 cm^2/Vs, respectively. RIT Nanofab fabricated devices shown in Figure S4 (b) obtained a hole and electron mobilities of 133.47 cm^2/Vs and 412.14 cm^2/Vs, respectively.

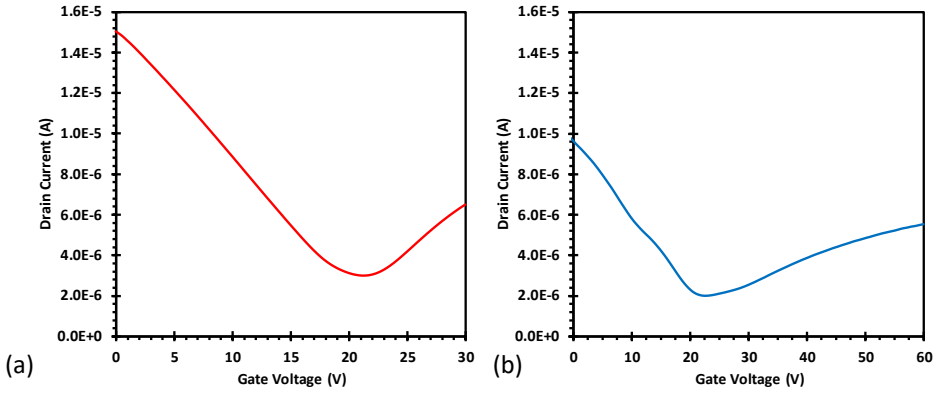

Figure S4. I_DV_G curve of (**a**) Graphenea GFET S-10 and (**b**) RIT Nanofab fabricated GFET with device dimensions of W/L = 100/80 µm