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A 200-MS/s 10-Bit SAR ADC Applied in WLAN Systems

Yu Zhang [1,2,*], Yilin Pu [1,3], Bin Wu [1,3], Taishan Mo [3] and Tianchun Ye [1,2]

[1] The Intelligent Manufacturing Electronics R&D Center, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing 100029, China
[2] School of Electronic, Electrical and Communication Engineering, University of Chinese Academy of Sciences, Beijing 100049, China
[3] Zhejiang CASEMIC Electronics Technology Co., Ltd., Hangzhou 310051, China
* Correspondence: zhangyu@ime.ac.cn

Abstract: This paper introduces a new high-performance successive approximation register (SAR) analog-to-digital converter (ADC) designed for high-speed and low-power wireless local area network (WLAN) applications using a SMIC 55 nm 1p8m CMOS process. The design employs several innovative techniques, including an improved bootstrap switch with high linearity, a 4-reference voltage method to minimize capacitive digital-to-analog converter (CDAC) mismatch, a kickback-canceling comparator to eliminate kick-back noise, and redundant design-assisted window-opening SAR logic to decrease conversion time. Experimental results reveal that the proposed ADC achieves an impressive signal-to-noise and distortion ratio (SNDR) of 55.3 dB and a spurious-free dynamic range (SFDR) of 66.6 dB at a sampling rate of 200 MHz with Nyquist frequency input while consuming a power of 2.8 mW at a 1.2 V power supply. This corresponds to a figure-of-merit (FoM) value of 29 fJ/conversion-step. Thanks to the incorporation of the 4-reference voltage method, the ADC demonstrates a significant area advantage compared to other designs with similar FOM values utilizing more advanced processes, occupying a mere 0.008 mm^2 of core area.

Keywords: SAR ADC; WLAN; kickback noise; mismatch

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1. Introduction

The proliferation of wireless communication technologies and the increasing demand for high-speed and high-precision wireless communication have created new opportunities and challenges for ADCs. As a critical component of wireless communication systems, ADCs play a vital role in converting analog signals into digital data for processing and transmission. In particular, WLAN technology has revolutionized the way people connect to the internet and communicate wirelessly, enabling users to access high-speed internet connections and use a variety of wireless devices.

Taking the receiver in WLAN as an example, as shown in Figure 1, various digital processing techniques, including modulation techniques, are implemented in the digital domain. However, the signals received by the antenna and the signals after down-conversion are in the RF and analog domains, respectively. Therefore, an analog-to-digital conversion interface is required to convert the analog signals into digital signals for signal processing and transmission. However, the increasing demand for high-speed, high-resolution, and low-power WLAN systems has placed a great burden on the design and implementation of ADCs.

With the improvement of CMOS technology, the application of large-scale digital logic and a fully dynamic structure make SAR ADCs more advantageous and attractive than other types of ADCs in the field of WLAN [1–4].

Despite these advancements, the design of SAR ADCs for WLANs still faces many challenges. One of the main challenges is the CDAC mismatch [5], KT/C noise [6], and

compartator input referred noise [7]. Another challenge is that the successive approximation serial structure limits the speed. These challenges require researchers to develop innovative design techniques to overcome them.

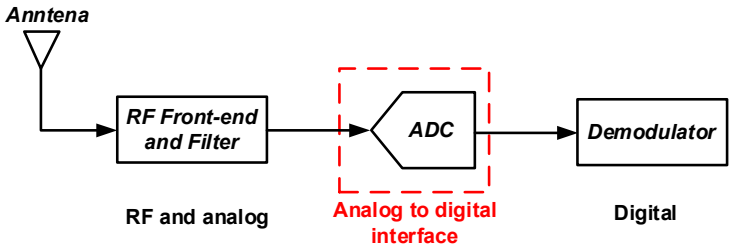

Figure 1. The role of ADC in the receiver.

The following Figure 2 illustrates the block diagram of a conventional SAR ADC, which mainly includes a sample and hold (S/H) block, a comparator, SAR logic, and a CDAC.

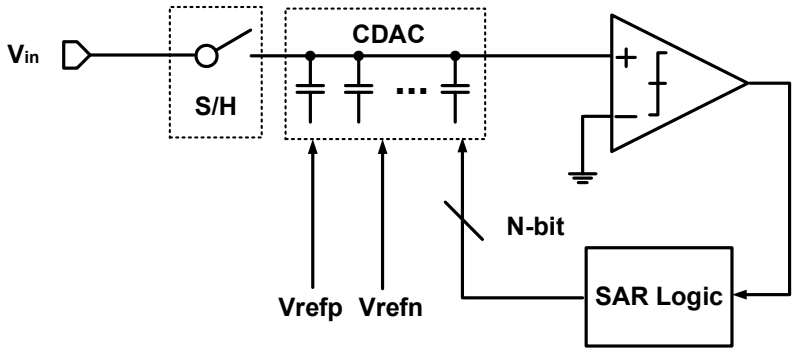

Figure 2. Architecture of a conventional SAR ADC.

This paper presents a novel SAR ADC designed for WLAN applications with a 200 MHz sampling rate and 10-bit resolution that consumes minimal power and occupies a small area. To achieve these goals, the design utilizes several innovative techniques, including an improved bootstrap switch with high linearity, a 4-reference voltage method to minimize CDAC mismatch, a kickback-canceling comparator to eliminate kickback noise, and redundant design-assisted window-opening SAR logic to decrease conversion time. The paper is structured as follows: Section 2 outlines the proposed SAR ADC architecture, which includes a high-linearity and high-speed design strategy. In Section 3, the individual building blocks are discussed in detail. Section 4 describes the test results. Finally, the discussion section compares the performance of the proposed ADC with other similar works, while the conclusion section summarizes the main contributions of this paper.

2. ADC Architecture and Considerations

The proposed SAR ADC architecture is depicted in Figure 3. During the sampling phase, the high-linearity bootstrap switch [8] is enabled to sample the input signal and store it in the CDAC. The design employs the top plate sampling technique, which means that the sampling signal Vin is directly connected to the input of the comparator. In the sampling phase, the bottom plate voltage of the CDAC is linked to VREF1, VREF2, VREF3, and VREF4 through an inverter and MUX, with VREF1 equaling 2 times VREF2, 4 times VREF3, and 8 times VREF4. After the sampling phase, the SAR ADC enters the successive approximation (SA) phase, during which the dynamic comparator begins to operate. The SAR logic adjusts the control signals SWP<i> and SWN<i> of the CDAC based on the comparator's output and generates the SAR ADC output result Dout. In the SA phase, the bottom plate of the CDAC is sequentially and monotonically switched to VREFN.

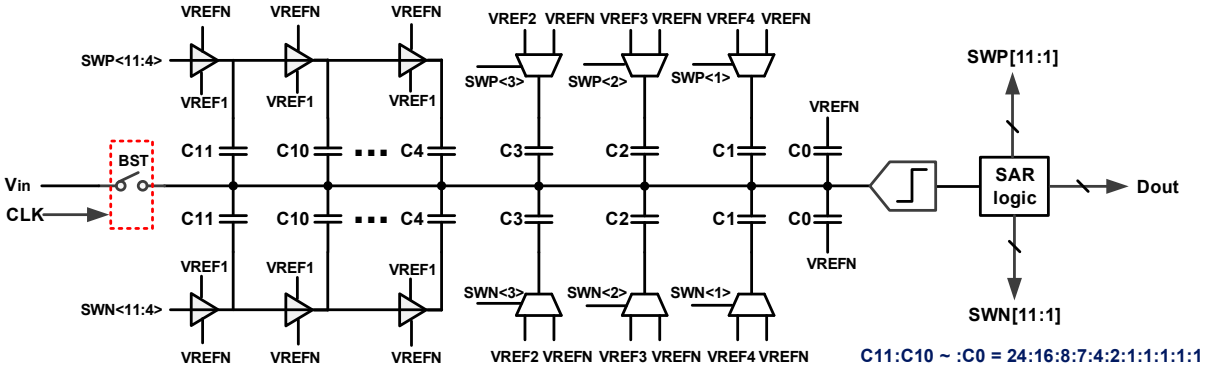

Figure 3. Architecture of the proposed SAR ADC.

The sampling clock signal CLK is generated by a clock generation circuit. The clock generation circuit utilizes a tunable delay unit and a series of digital logic to produce a variable duty cycle sampling clock signal.

2.1. In Terms of Linearity

The ADC's linearity is constrained by several factors. The first issue faced is the CDAC mismatch. According to capacitor mismatch theory, due to capacitor mismatch deterioration caused by size reduction, larger unit capacitors are needed to meet the linearity requirement [9,10]. However, the use of a large CDAC not only wastes power in the input and reference buffers but also imposes more stringent timing constraints. To reduce the total capacitance, the current mainstream solution is to reduce the size of the unit capacitor and then combine it with a digital calibration scheme [11]. However, whether based on self-calibration [12], LMS-based digital calibration [13–15], or capacitor mismatch shaping technology [16], these calibration schemes demand a significant amount of digital resources and lead to an increase in gain error. Therefore, these calibration solutions are more cost-effective for designs with 12 bits or more, but less so for the 10-bit design in this paper. The introduction of the dual-reference voltage technique [17] provides a new solution to reduce the total capacitance of the CDAC. Unlike the previous approach of reducing the size of the unit capacitor, the dual-reference voltage technique can directly reduce the total number of required capacitors in CDAC. The core theory of the multi-reference voltage scheme is charge conservation. In this paper, a 4-reference voltage technique is proposed based on this theory. Figure 4 shows the voltage jumping in the top plate of the CDAC during the switching process of the proposed 4-reference voltage technique. According to the law of charge conservation, it can be seen that the voltage change ratio ΔV1: ΔV4 satisfies 1:8 during the switching process of S1 and S4. However, to achieve a voltage jump ratio of 1:8 in a standard binary CDAC, the capacitance value of the corresponding bit position must satisfy an 8-fold relationship.

Following the switching scheme of the 4-reference voltage, the requirement for the number of capacitors in CDAC that meet the 10-bit requirement is reduced from 512 to 66. The unit capacitor is ultimately designed to be 6 fF. The capacitance value of a unit capacitor can better meet the requirements of linearity for mismatch consideration, and the total capacitance value of CDAC is about 410 fF, which can better balance the KT/C noise and the design pressure of the driving stage.

The second issue encountered by high-linearity ADCs is kickback noise. At sampling rates of hundreds of MHz [18,19], the comparator's speed is usually as high as several GHz. During the entire SA phase, comparator kickback noise will be injected into the CDAC through the C_{gs} and C_{gd} of the input differential pair. Due to the samping transistor being in the OFF state, the kickback noise on the top plate of the CDAC will affect the front-end driving structure through the C_{ds} of the switch transistor and will also be coupled to the output end of the RVB through the CDAC, as shown in Figure 5. Both situations will present a limiting factor for ADC resolution. This paper proposes a dynamic comparator

kickback noise cancellation technique that can effectively solve the degradation caused by the kickback noise on the CDAC top plate.

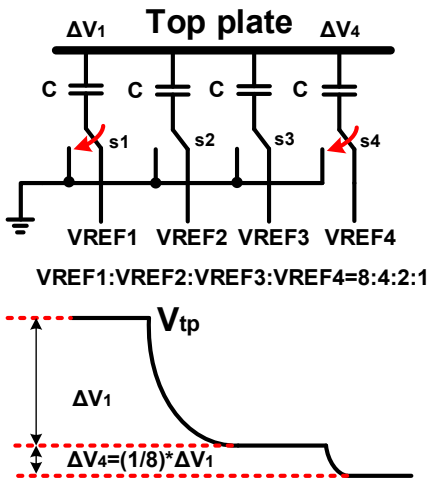

Figure 4. Voltage jumping during the 4-reference voltage scheme.

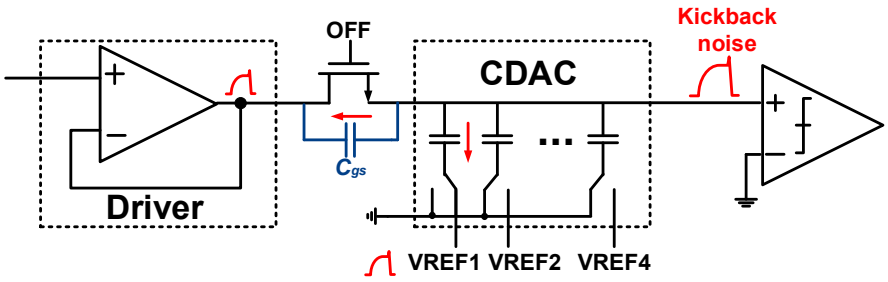

Figure 5. Kickback noise affects RVB and driving stages.

2.2. In Terms of Speed

In this design, the sampling time can be optimized at various sampling rates by adjusting the duty cycle through the clock generation circuit. This provides more time for the SA phase. During the SA phase, the speed limit of each bit conversion cycle is usually determined by the delay in the data path. The data paths in each bit conversion cycle, as shown in the red part of Figure 6, mainly include T_{comp}, $T_{sar,}$ and T_{set}.

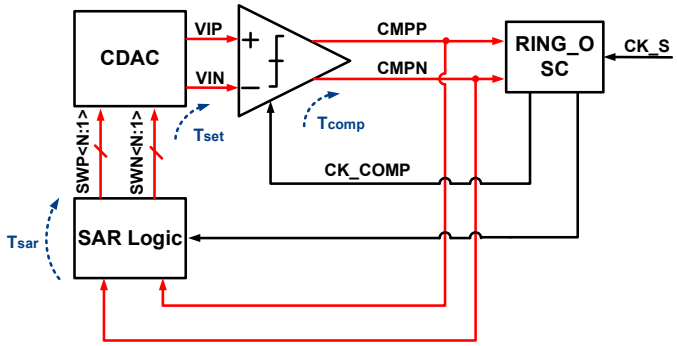

Figure 6. Data path during the SA phase.

T_{comp} represents the decision time of the comparator, T_{sar} represents the delay of the SAR logic, and T_{set} represents the time required for the VIP and VIN voltages at the comparator input to be established to the required accuracy. To shorten the corresponding delays, this design has been optimized for high-speed timing in several aspects.

Firstly, the optimization of T_{set} is crucial in the high-speed design. Reducing the settling time means enlarging the possibility of settling error, and the redundancy scheme [20] can be used to tolerate a certain range of settling error during bit-cycling. Additionally, redundancy techniques can also mitigate decision errors that may occur during the comparison process. This paper proposes a binary-scaled recombination redundancy scheme based on the 4-reference voltage scheme. Furthermore, to meet the requirements of fast response for the reference voltage, a high-speed on-chip RVB is proposed.

Additionally, in order to further reduce the delay in the data path, this design employs dynamic SAR logic based on a window-opening strategy. This approach allows the comparator results to be directly transmitted to the control signals of CDAC, greatly reducing the T_{sar} in the data path.

Moreover, to speed up the comparator, a monotonic switching procedure is adopted in this work. Specifically, the output common mode voltage of the CDAC decreases as the bit cycling progresses to the least significant bit (LSB), which increases the comparator's transconductance (gm) when using a p-type input pair.

3. Circuit Implementation

3.1. Bootstrap

Figure 7 shows a diagram of the conventional structure of the bootstrap. The cksb is the inverted signal of the sampling clock signal cks, and its working state mainly has two stages: charge storage and charge sharing. When the sampling clock cks is high, *C*3 is in the charge storage stage, and *C*3 is connected to VSS and *VDD* through M3 and M4 to complete the charging process. After charging is complete, cks jumps to a low voltage, and the *C*3 capacitor enters the charge sharing stage. At this step, the bottom plate of *C*3 is connected to IN/OUT through M9/M10, and the top plate of *C*3 is connected to the gate voltage signal sw_ctrl through M5. In the charge storage stage, the stored charge on *C*3 is $VDD^{*}\times C3$, and under the charge sharing stage, the V_{gs} of M10 is V_{boost} according to the law of charge conservation, which gives the expression:

$$V_{boost} \times (C3 + Cp) = VDD \times C3$$

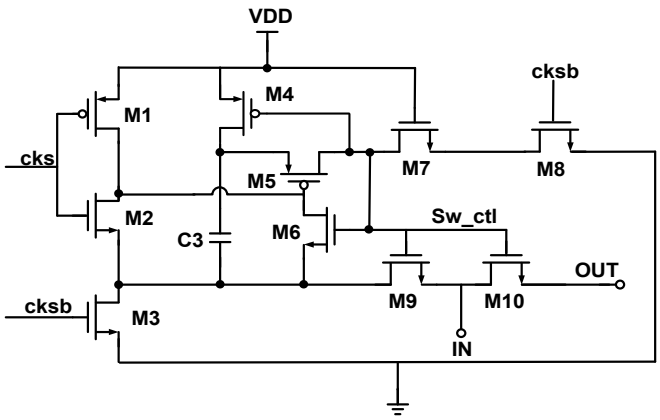

Figure 7. The conventional bootstrap.

C_p is the C_{gg} of M9, M10, M5, and M6, where C_{gg} contains variable capacitance that reduces linearity.

The proposed new structure of bootstrap is shown in Figure 8. It can be seen that in the charge sharing stage, the non-linear capacitance between sw_ctrl and IN terminals is only the switch transistors M9 and M10. In addition, the newly added M13 acts as a protective transistor, mainly to protect the V_{ds} of M7 from exceeding $2 \times VDD$ in the charge sharing stage, thereby improving the lifetime of the transistor. Furthermore, when in the charge sharing stage, M13 prevents the charge from leaking C3 into the drain of M8, further improving the linearity of the bootstrap.

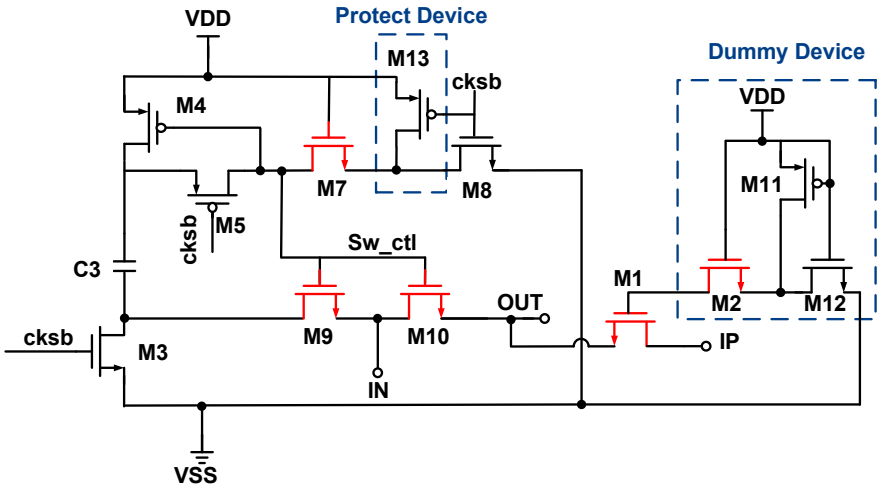

Figure 8. The proposed bootstrap.

During the SA phase, the M10 switch is closed, and the input signal (IN/IP) is coupled to the top plate of the CDAC through the C_{ds} of M10. This will directly lead to a degradation of the ADC's performance, which can be cancelled by cross-coupling [21]. A dummy capacitor scheme similar to that of ref [1] is also used to cancel the coupling effect. Nevertheless, in ref [1], the gate voltage of M1 is directly grounded, but in this design, the gate position of M1 is increased to include M2, M11, and M12, which are the same size as M7, M8, and M13. Their main function is to make the environment around M1 and M10 consistent in the layout to achieve better matching and, thus, better cancellation of the coupling effect. In the layout of this circuit, all the transistors in the red part of Figure 8 are placed in the deep n-well (DNW), which can better reduce the V_{bs} of M10 and make the on resistance (R_{on}) more stable. In fact, the adoption of DWN and dummy transistors not only improves linearity but also leads to an increase in layout area.

3.2. Comparator

The dynamic comparator with kickback noise cancellation mechanism proposed in this paper uses a conventional two-stage structure consisting of a preamplifier and a latch stage, as shown in Figures 9 and 10.

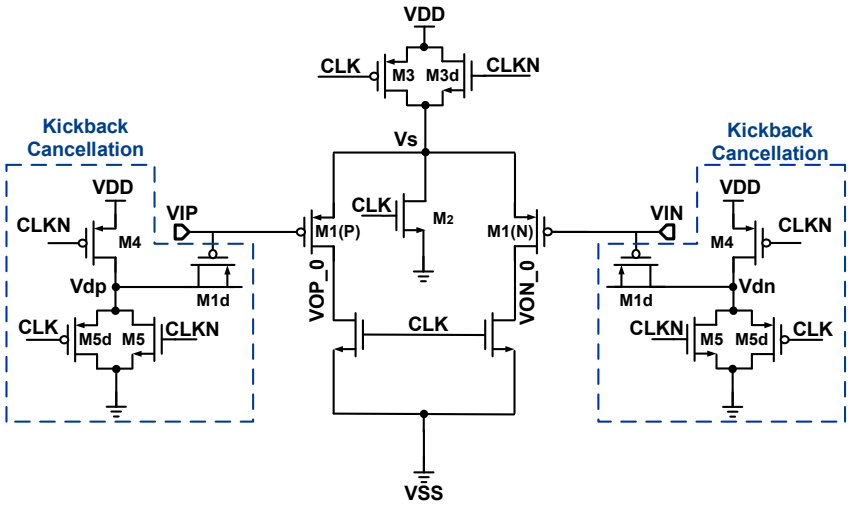

Figure 9. The preamplifier stage of the comparator.

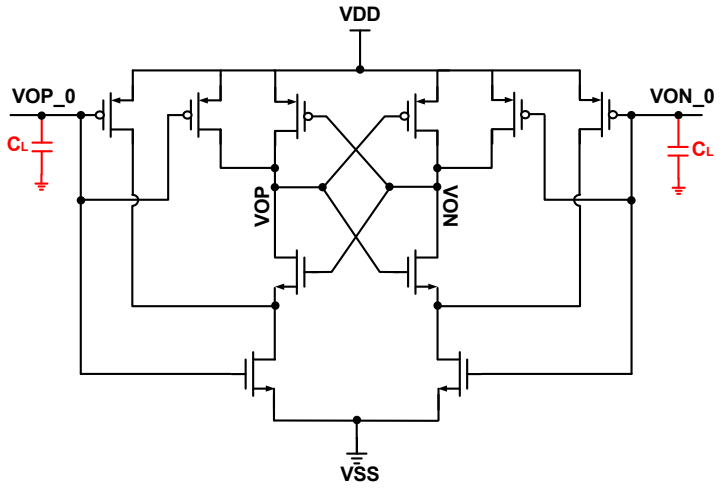

Figure 10. The latch stage of the comparator.

During the reset phase of the preamplifier, the clock signal CLK is maintained at a high level, resulting in the preamplifier output voltages VOP_0 and VON_0 being initialized to a ground voltage. Following this, during the subsequent comparison phase, the CLK signal transitions to a low level, enabling the charging process of the capacitor CL. The voltages VOP_0 and VON_0 exhibit varying charging rates, influenced by the input voltages VIP and VIN. This generates a differential voltage VO between VOP_0 and VON_0. When the differential voltage VO exceeds the threshold voltage of the second stage input transistor, the latch stage enters operating mode and finally produces a digital output at the points VOP and VON.

As described earlier, kickback noise is a common issue faced by all dynamic comparators, and its impact on the comparator is mainly manifested in the comparison phase. The kickback noise cancellation circuit proposed in this design is shown in Figure 9, where device M1d is a dummy transistor of M1, with its source/drain node discharged to ground during the reset phase of the preamplifier. When the comparator starts working, the comparator clock generates a falling edge, which causes the source terminal Vs of the input pair to start charging, producing an upward pulse that injects a charge amount ΔQ into the CDAC top plate, as shown in Figure 11. At the same time, the source-drain end of M1d produces a corresponding downward discharge pulse, which extracts a charge amount of ΔQ at the top plate of CDAC. In other words, all the charge injected by the input pair is taken away by the dummy transistor, effectively avoiding the impact of kickback noise. In addition, the purpose of the M4 and M2 transistor is to discharge Vs to ground and charge Vdp/Vdn to Vdd during the reset phase, so as to better ensure the consistency of charge and discharge at the CDAC top plate during the comparison phase.

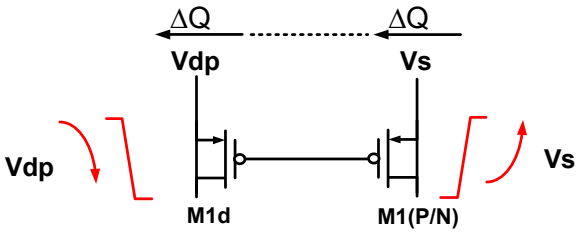

Figure 11. Kickback cancellation during the comparison phase.

Furthermore, due to the influence of the phase difference between CLK and CLKN, there may be a time deviation between the charge extraction of the dummy transistor and the charge injection of the comparator input pair, resulting in some residual charge. Therefore, in this design, the P/NMOS impedances of the transistors M3 and M3d, as well as M5 and M5d, need to be matched as much as possible.

The transient simulation of the comparator is conducted to demonstrate the effectiveness of the kickback cancellation circuit. Assume that the capacitor from the comparator input to ground is 410 fF and that the operating frequency of the comparator is 2 GHz. The transient simulation result of the comparator input voltage with and without the kickback cancellation circuit is shown in Figure 12, and it can be seen that the kickback cancellation mechanism plays a good suppression role for kickback noise in the comparison phase. In fact, the source-drain end of M1d needs to undergo charging and discharging operations in each comparison cycle, which increases the power consumption of the comparator. When the comparator operates normally at a frequency of 3 GHz, the approximate increase in dynamic current can be calculated using the CVF formula as 300 μA. Therefore, this structure trades off power consumption for the low kickback input characteristics of the comparator.

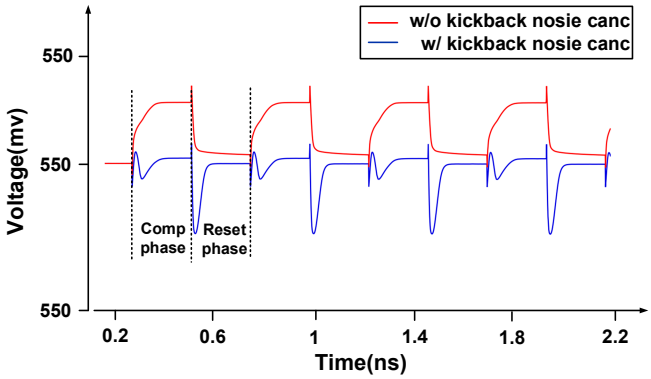

Figure 12. The comparator input voltage with/without a kickback cancellation circuit.

3.3. CDAC

In general, the CDAC occupies a significant portion of the ADC chip area. As described before, the 4-reference voltage switching strategy can significantly reduce the required number of unit capacitors in the CDAC, thereby greatly reducing the area of the CDAC. In addition, combining this approach with a binary-scaled recombination redundancy design can greatly relax the design requirements for the input buffer and RVB.

Based on the CDAC scheme shown in Figure 3, Table 1 lists the weight scheme and corresponding redundancy arrangement in this design.

Table 1. Redundancy arrangement in this design.

Bit-Cycling	Bit Weight	Reference (VREF)	Equivalent Weight	Redundancy (LSBs)
1	48	1	384	256
2	32	1	256	128
3	16	1	128	128
4	14	1	112	32
5	8	1	64	16
6	4	1	32	16
7	2	1	16	16
8	2	1	16	0
9	2	0.5	8	0
10	2	0.25	4	0
11	2	0.125	2	0
12	1	0.125	1	0

The equivalent weight is calculated based on the charge conservation principle, where the equivalent weight is equal to the product of bit weight and 8×Reference. The range of redundancy indicates the maximum tolerable error in the current bit.

Due to the fact that the MSB capacitor switching induces a large disturbance on the VREF, which is the main error source of incomplete settling in CDAC, most of the

redundancy range is arranged for the MSB decision steps. The unit capacitor is a high-density and highly matched MOM capacitor provided by the foundry. The total sampling capacitance is 410 fF, where the capacitance in the main DAC is about 340 fF and the parasitic capacitance is 70 fF.

3.4. SAR-Logic

According to the previous introduction, the delay T_{sar} on the SAR logic is a part of the data path in the bit conversion cycle. The traditional SAR logic consists of two stages of DFF, and the delay of the T_{sar} is shown as the red line in Figure 13a, which can be represented as: $T_{sar} = 2 \times T_{cq} + T_{OR}$, where T_{OR} is the delay of the OR gate and T_{DFF} is the delay of the shift register and the data register.

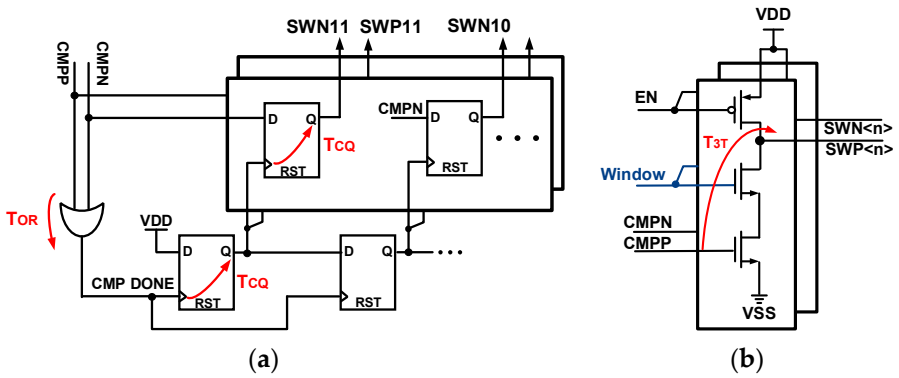

Figure 13. (**a**) Critical path of traditional SAR logic; (**b**) critical path of the 3-T cell.

To reduce the delay of T_{sar}, the proposed SAR logic uses a window-opening strategy to open the "window" signal in advance before each bit of data arrives and complete the "window" signal closing operation after data transmission. Figure 14 illustrates the scheme of the proposed SAR logic based on the window-opening strategy. The circuit of the tri-state gate is shown in Figure 15 (left), and the timing block of the window-opening is shown in Figure 15 (right). The bit cycling begins immediately after CLK_SAMPLE pulls down. The first DFF output EN1 of the opening window register level is high, opening the "Window" signal of the first tri-state gate. After the comparison process, the resultant signal is directly passed through the 3T structure. At this time, due to the high pulse generated by the CMP_DOWN signal, it will trigger the first DFF of the closing window register level to output a high level of LOCK1, thus locking the "window" signal. After the first reset phase of the comparator is completed, the second DFF output EN2 of the opening window register level is high, and the "window" signal of the second tri-state gate is opened to wait for the second comparator result. The remaining bit-cycling process is sequentially executed in this way until the last bit triggers the LOCK_RING signal to end the SA phase.

The T_{sar} of the proposed SAR logic is based on a window-opening strategy equivalent to a single 3-T cell delay, as shown in Figure 13b.

Compared with traditional SAR logic, the saved time during the conversion cycle can be expressed as:

$$T_{sar} = 12 \times (T_{CMP\_RDY} + 2 \times T_{DFF} - T_{3-T})$$

This time is approximately 1.5 ns in the SMIC55 process. By adopting this SAR logic, the conversion speed of the ADC can be greatly improved. However, the 3T cell is a tri-state gate, and during the SA phase, it exhibits a high-impedance state at its output. This necessitates additional risk considerations in circuit design.

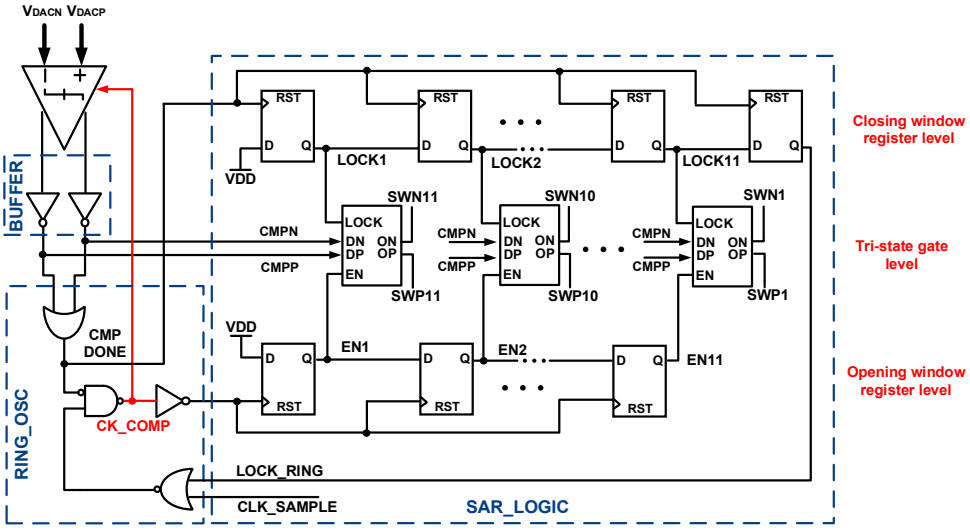

Figure 14. The proposed SAR Logic.

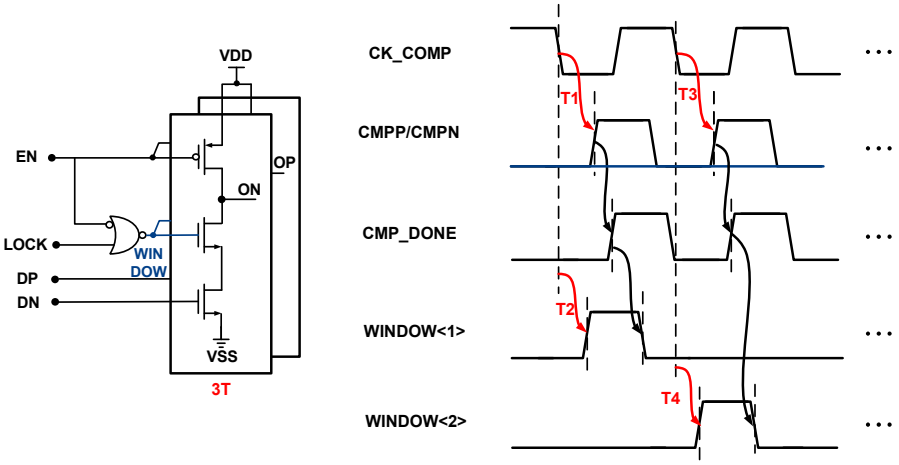

Figure 15. The proposed tri-state gate and corresponding timing diagram of the window-opening strategy.

3.5. RVB

The high-speed clock signal of the comparator, which can reach several GHz, imposes stringent requirements on the reference voltage settling time on the CDAC top plate. Typically, the settling process must be completed within a few hundred picoseconds. This requires the unity-gain frequency of the RVB to reach several GHz, which will consume a significant amount of current, even more than the ADC core circuit. To address this issue, this design uses an on-chip source follower [22,23] structure as the RVB for the four reference voltages.

The open-loop output stage structure provides a small output impedance, a wide bandwidth, low noise, and a small area. The following Figure 16 shows the proposed RVB. The output stage of the IQ channels replicates the second stage of the closed-loop operational amplifier, and the size of the output transistor M1R in both IQ channels is ten times that of M1. Moreover, in order to address the impact of power supply noise on the reference voltage, the output stage is implemented as a cascode structure, with VB providing the bias voltage for the stacked transistors, resulting in an improved power supply rejection ratio (PSRR). Additionally, RC filters have been incorporated into the design to minimize the effects of operational amplifier output noise.

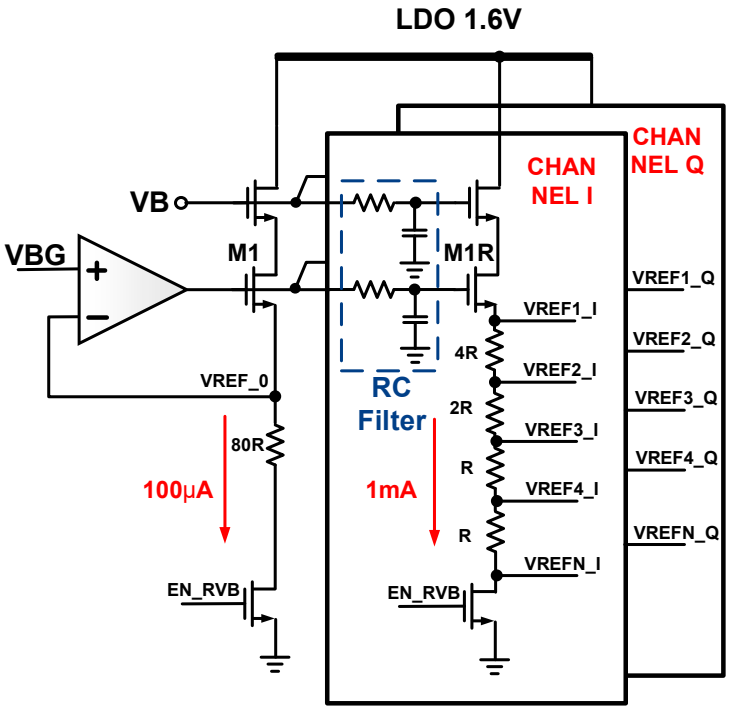

Figure 16. The proposed RVB.

With the help of redundancy technology, the output stage current is determined to be 1 mA. This design also uses a switch controlled by the signal EN_RVB to separate VREFN and VSS. Since there is only a single-point connection between VREFN and VSS on the layout and the wiring matching VREF1/2/3/4 with VREFN is in parallel, this can make the ratio between the four positive reference voltages VREF1/2/3/4 and the negative reference voltage VREFN more matched. In addition, since the mismatch between the resistors (4R, 2R, and R) at the output of RVB and the CDAC mismatch are equivalent in terms of their effects, it is necessary to ensure good matching by increasing the area of these resistors. Furthermore, dummy resistors are added around these resistors in the layout process to further improve the matching between the VREF1/2/3/4 and VREFN. The VBG, which is equal to 1.2 V and tracks the bandgap voltage, is insensitive to temperature and process variation. The output stage supply voltage of the RVB is 1.6 V.

Table 2 summarizes the detailed noise contribution of the proposed SAR ADC, assuming no CDAC mismatch. The thermal noise and quantization noise were obtained through calculation, while the comparator input referred noise and reference noise were obtained from post-layout noise simulation.

Table 2. Noise contribution of the proposed SAR ADC arrangement of this design.

Noise Source	Comparator Noise	Thermal Noise	Quantization Noise	Reference Noise
POWER (μV_{rms})	250	142	676	152
Ratio (%)	20.5	11.6	55.4	12.5

4. Test Results

The prototype ADC is fabricated in SMIC 55 nm 1p8m CMOS technology. Figure 17 shows the chip micrograph and the layout zoomed-in view of the ADC core, which only occupies 0.008 mm^2 (102 µm × 84 µm).

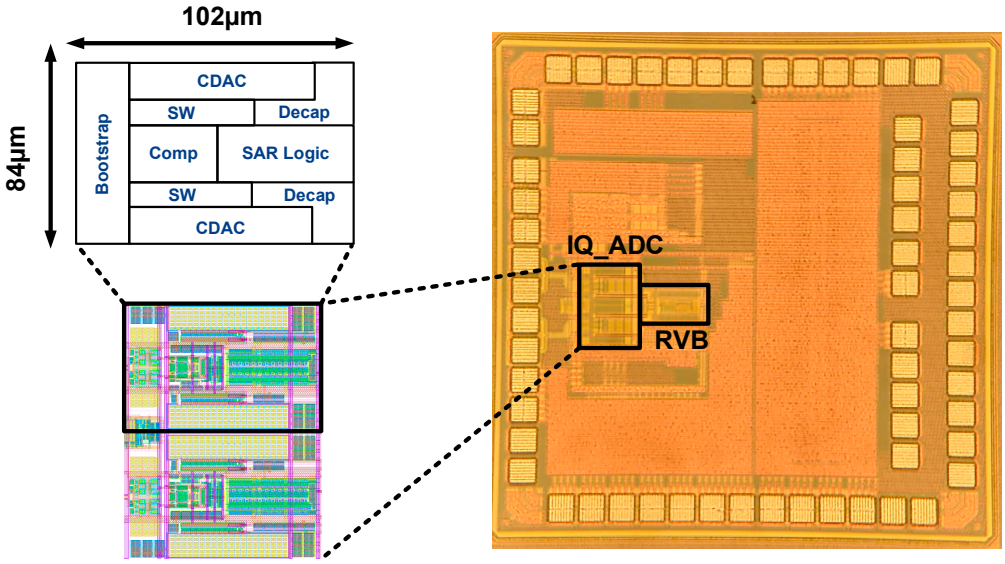

Figure 17. Chip micrograph and layout zoomed-in view of the SAR ADC core.

During the testing, the ADC operated with a reference voltage of 1.2 V. To achieve a full-swing output, the input VPP was increased to nearly 1.1 V. This indicates a gain error of approximately 9%. At a sampling rate of 200 MHz, the SA phase and sampling phase timings are adjusted using the clock duty cycle adjustment circuit inside the test chip to meet the requirements of sampling and conversion. All subsequent tests were conducted based on a sampling rate of 200 MHz.

Figures 18 and 19, respectively, depict the FFT plots under low-frequency input and Nyquist frequency input conditions. Under a low-frequency input of 6.2 MHz, the measured values for SNDR and SFDR are 56.3 dB and 59.3 dB, respectively, while under the Nyquist frequency input of 99 MHz, the measured values for SNDR and SFDR are 55.3 dB and 66.6 dB, respectively. Figure 20 shows the measured static performance using the code density method. The differential nonlinearity (DNL) is within −0.69/+0.62 LSB, and the integral nonlinearity (INL) is within −1.1/+1.2 LSB.

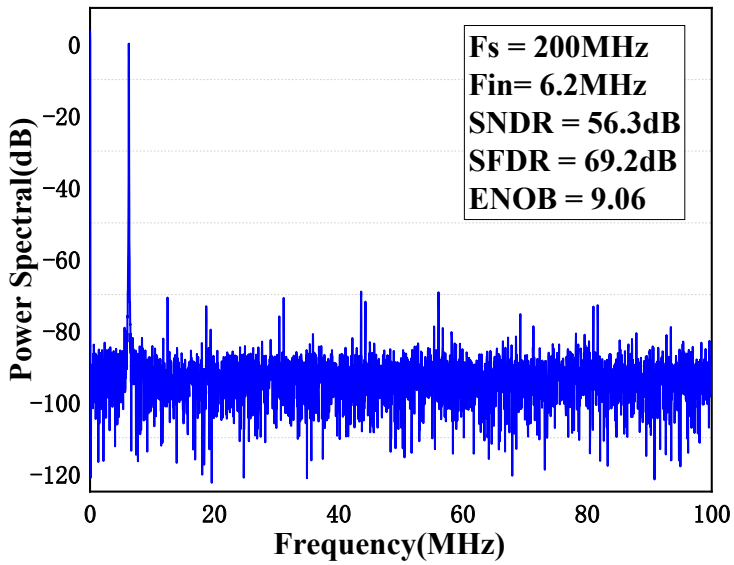

Figure 18. FFT plot with a 6 MHz input frequency at 200 MS/s.

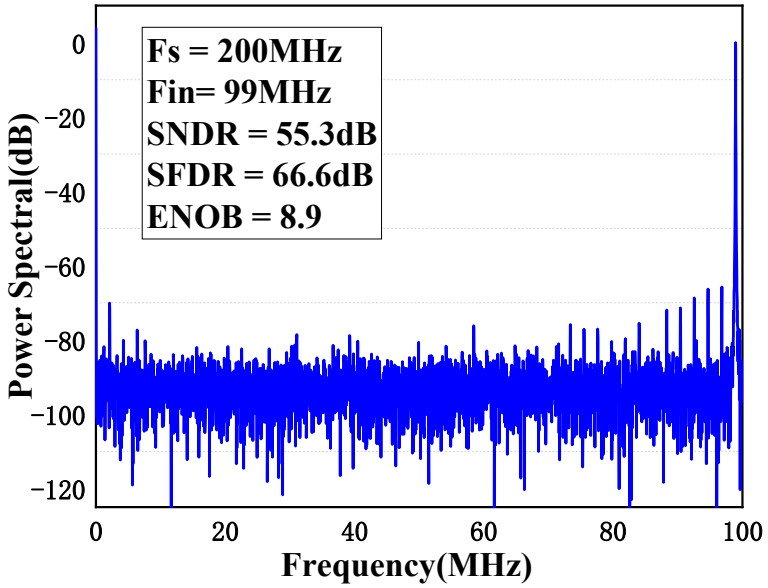

Figure 19. FFT plot with a 99 MHz input frequency at 200 MS/s.

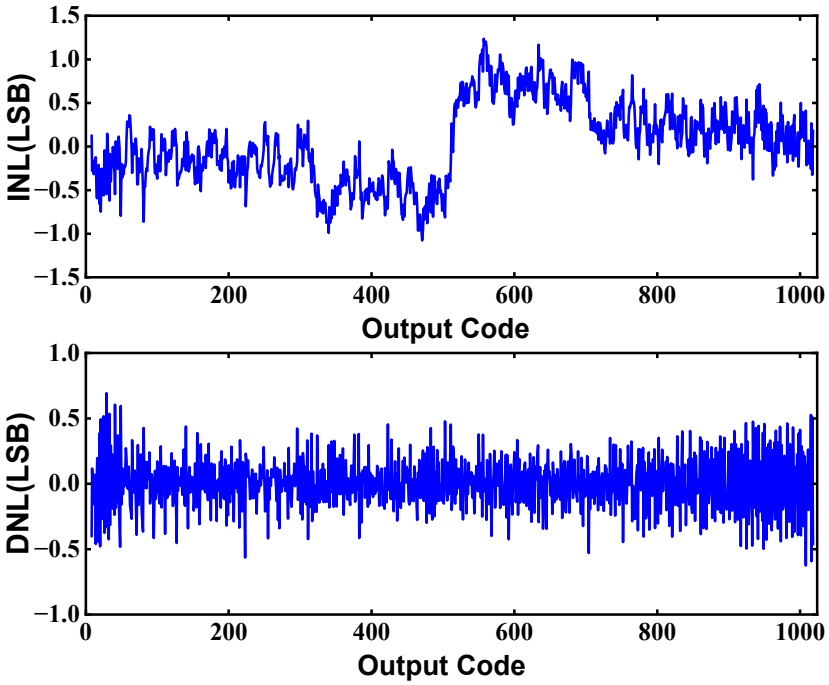

Figure 20. Measured DNL and INL.

Figure 21 plots the measured SNR and SNDR values versus the input power when the input frequency is 99 MHz. The total power consumption of the single ADC core is approximately 2.8 mW at a 1.2 V power supply with a sampling frequency of 200 MS/s. The proposed SAR ADC achieves a small area of 0.008 mm^2 and a FoM of 27 fJ/conversion-step at Nyquist rate.

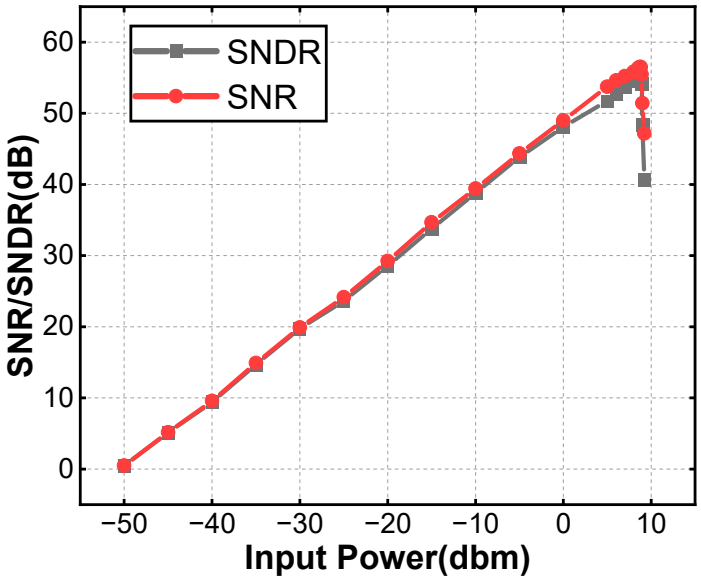

Figure 21. Measured performance versus input power.

5. Discussions

The performance of the proposed ADC at the Nyquist input frequency is compared to other state-of-the-art SAR ADCs with similar specifications in Table 3 based on the test results.

Table 3. Comparison with previous works.

Ref	[24]	[7]	[25]	[26]	[27]	This Work
Technology (nm)	40	65	28	90	22	55
Supply (V)	1.1/1.3	1.2	1.05	1	0.8	1.2
Sampling rate (MS/s)	100	160	250	100	200	200
Nyquist SNDR (dB)	56.3	55.6	52.4	55.4 *	48.7	55.3
Nyquist SFDR (dB)	76.3	69	68.3	68.1 *	62	66.3
ENOB (bit)	9.05	8.9	8.4	8.91 *	7.8	8.9
Power (mW)	1.4	2	3.23	1.25	4.3	2.8
INL(LSB)	−0.71/ +0.82	−0.97/ +0.93	−0.86/ +0.96	−1.02/ +1.8	-	−1.1/ +1.2
DNL(LSB)	−0.73/ +0.57	−0.75/ +0.47	−1.02/ +1.37	−0.93/ +1.72	-	−0.69/ +0.62
Nyquist FOM (fj/conv)	26.2	25.4	38.2	26 *	96.5	29
Core Area (mm^2)	0.027	0.023	0.068	0.0144	0.0168	0.008

* Due to a lack of testing data for the Nyquist input frequency, only low-frequency input data are available.

For SAR ADCs, the CDAC occupies the most significant area. The incorporation of the 4-reference voltage method provides a significant advantage in terms of area efficiency, surpassing other designs with similar FOM values that utilize more advanced processes. Remarkably, the proposed ADC occupies only 0.008 mm^2 of core area. The design of a high-linearity bootstrap, low-noise comparator, and low-mismatch CDAC enables the proposed ADC to achieve impressive SNDR and SFDR of 55.3 dB and 66.6 dB, respectively, at a sampling rate of 200 MHz and Nyquist input frequency. These results meet the system's requirements for ADC sampling rate and effective resolution. The measured SNR results also closely align with the SNR values calculated based on the noise budget in

Table 2, reflecting excellent design matching. In addition, in the subsequent large-scale testing (results not shown), the deviation of the SNDR was concentrated within 0.5 dB, further demonstrating that the proposed ADC can meet the requirements of large-scale production effectively.

6. Conclusions

This paper employs an improved high-linearity bootstrap to achieve high linearity sampling. The 4-reference voltage technique is used to increase the unit capacitance and reduce capacitor mismatch while maintaining the total capacitance. A comparator with a kickback cancellation mechanism is used to mitigate the impact of kickback noise. In terms of speed, a binary-scaled recombination redundancy design and an open-loop output stage RVB are used to accelerate the establishment of the reference voltage on the top plate of the CDAC. Additionally, a window-opening strategy is employed in the SAR logic to reduce the delay in the data path. The experimental results reveal that the proposed ADC achieves an impressive SNDR of 55.3 dB and a SFDR of 66.6 dB at a sampling rate of 200 MHz with Nyquist frequency input. It operates with a power consumption of 2.8 mW at a 1.2 V power supply, resulting in a remarkable FoM value of 29 fJ/conversion step. The core area of the proposed ADC is only 0.008 mm^2. With its impressive area efficiency and high-performance, low-power characteristics, the proposed ADC emerges as a promising solution for analog-to-digital conversion in WLAN applications.

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Conflicts of Interest: The authors declare no conflict of interest.

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