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Design Techniques for Low-Voltage RF/mm-Wave Circuits in Nanometer CMOS Technologies

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Abstract: This paper reviews state-of-the-art design approaches for low-voltage radio frequency (RF) and millimeter-wave (mm-wave) CMOS circuits. Effective design techniques at RF/mm-wave frequencies are described, including body biasing in fully depleted (FD) silicon-on-insulator (SOI) CMOS technologies and circuit topologies based on integrated reactive components (i.e., capacitors, inductors and transformers). The application of low-voltage design techniques is discussed for the main RF/mm-wave circuit blocks, i.e., low-noise amplifiers (LNAs), mixers and power amplifiers (PAs), highlighting the main design tradeoffs.

Keywords: body biasing; CMOS technology; integrated inductors; integrated transformers; low-noise amplifiers (LNAs); mixers; power combining; power amplifiers (PAs); reactive coupling

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1. Introduction

The success and pervasiveness of CMOS integrated circuits (ICs) have been mainly due to the continuous technology scaling that has improved transistor performance, even at RF and mm-wave operations, along with the lower production costs to comply with the mass market requirements. Thanks to this extreme scaling, advanced nanometer CMOS technologies are now suited to a wide range of applications up to 100 GHz (e.g., 5G, automotive radar, and imaging), with significant advantages over traditional compound semiconductor or heterojunction bipolar transistors (HBT), in terms of the level of integration, thus allowing complex system-on-chip (SoC) implementations [1]. Furthermore, CMOS scaling produces a continuous decrease in the supply voltage (well below 1 V), enabling new applications, such as wireless sensor networks (WSNs) and the Internet of Things (IoTs). Unfortunately, sub 1-V supply voltages involve the circuit design, especially at RF/mm-wave frequencies, thus requiring nonstandard circuit topologies and proper techniques to mitigate the voltage limitations. This work presents the most interesting approaches to comply with very low supply voltages for RF/mm-wave circuits, with a particular focus on nanometer CMOS technologies. A crucial role in RF/mm-wave, low-voltage operation is performed by the reactive components, especially inductive components (i.e., integrated inductors and transformers) that can be properly exploited to compensate for the limited voltage headroom. Another important contribution is also given by the body biasing approach, especially in fully depleted (FD) silicon-on-insulator (SOI) platforms [2], which further improves IC performance at low-voltage supply levels.

This paper is organized as follows: Section 2 reviews the main features, limitations, and design issues of inductive components (i.e., spiral inductors and transformers), with reference to the back-end-of-line (BEOL) in CMOS. Section 3 is dedicated to the body biasing approach in both traditional bulk and FD-SOI technologies. Low-voltage circuit topologies for RF/mm-wave operation are revised in Section 4, with special insights into low-noise amplifiers (LNAs), mixers and power amplifiers (PAs). Finally, Section 5 draws the main conclusions, highlighting future challenges for low-voltage RF/mm-wave ICs.

2. Integrated Inductive Components: Loss Phenomena and Main Design Guidelines

Inductive components are very important in RF/mm-wave integrated circuits (ICs). Indeed, they are exploited to implement irreplaceable functionality, such as simultaneous impedance/noise matching to the 50-ohm input source in LNAs, impedance matching and tuned resonant loads in amplifiers, LC tank in voltage-controlled oscillators, and integrated single-ended-to-differential conversion [3–7]. The Q -factor maximization at a given value of inductance, L , is the most common design issue. Other important figures of merit are the inductor ωQL product, the transformer characteristic resistance (TCR) and the insertion loss (IL) [8,9].

A scanning electron microscope (SEM) cross-section of a silicon-integrated spiral inductor is shown in Figure 1a. Geometrical parameters (i.e., layout parameters) can be properly tuned within the technology constraints, namely, the coil shape (i.e., circular, polygonal or squared), the number of turns, n , the inner diameter, d_{IN} , the metal width, w , and the metal spacing, s . The process parameters, such as the metal BEOL, the thickness and permittivity of the insulation layers, and the substrate conductivity, cannot be modified. Generally, the design of inductive devices is aimed at minimizing energy loss. The main energy dissipation phenomena of silicon-integrated inductive components are shown in Figure 1b. They occur in the metal layers that form the coil (series losses), as well as in the conductive layers below (parallel losses). The former is mainly due to the current crowding on the internal sides of the coil, due to skin and proximity effects. Current crowding rises with an increase in the operating frequency, thus increasing the equivalent resistance of the inductor. Thick conductive metals and multi-layer structures are common arrangements to lower the series losses, but their effectiveness degrades at RF/mm-wave frequencies. According to Faraday's law, current crowding is stronger in the inner turns. Therefore, the adoption of spirals with a low fill ratio, ρ , is a common rule [10].

Figure 1. (a) SEM cross-section of a silicon-integrated spiral inductor; (b) simplified representation of main loss phenomena in silicon-integrated inductive components. Reprinted with permission from Ref [9]. Copyright 2020, IEEE.

Figure 1b also depicts two different mechanisms taking place in the substrate layers, i.e., the (vertical) displacement currents and the (horizontal) magnetically induced currents. Both electrically and magnetically induced currents increase at RF/mm-wave frequencies and dominate the inductor losses. Substrate shielding can be implemented to reduce the effect of parallel losses for RF operation [11,12].

The design of an inductive component starts with its geometrical parameters, which set the low-frequency inductance, L_{DC} . The inductance maximum value reduces with an increase in the operating frequency, due to self-resonance. Actual inductors have a typical inductance range from a few hundred picohenrys to tens of picohenrys, moving from tens of gigahertz to 100 GHz and beyond. Since inductance is mainly dependent on n , the inner diameter, d_{IN} , is adjusted to trade off the silicon area with current crowding phenomena, by using a low fill ratio, ρ , while the metal width, w , is typically tuned to set the peak quality factor, Q_{MAX} , at the operating frequency. The metal spacing, s , must be set at the minimum value to maximize the coil auto-inductance. For the purpose of completeness, Table 1 summarizes the relationship between the electrical performance and the layout/process parameters of an integrated inductor.

Table 1. Layout/process parameters vs. electrical performance of an integrated inductor.

Inductor Parameters		Peak Q-Factor (Q_{MAX})	Low-Frequency Inductance (L_{DC})	Self-Resonance Frequency (SRF)
Number of turns, n	▲	▼	▲	▼
Metal width, w	▲	▲	▼	▼
Metal spacing, s	▲	▼	▼	▼
Fill ratio, ρ	▲	▲▼	▲▼	▼
Metal thickness, t	▲	▲	▼	▲
Oxide thickness t_{ox}	▲	▲	—	▲
Substrate resistivity, ρ_{SI}	▲	▲	▲	▲

▲ increase; ▼ decrease; ▲▼ optimum; — constant.

A special role in RF/mm-wave ICs is performed by transformers [13]. Figure 2 shows the main structures of integrated transformers. The traditional arrangements are the interleaved and stacked configurations. The interleaved configuration guarantees better winding Q -factors at the cost of a lower magnetic coupling factor, k , compared to the stacked configuration. However, interleaved transformers easily implement high transformer ratios, N , and achieve better SRFs. The interstacked configuration exploits mixed interleaved/stacked coils and guarantees higher k with respect to the stacked configuration, providing full winding symmetry [6,14,15]. Finally, when the operative frequency is excessively high with respect to the adopted BEOL, stacked folded configurations can be exploited [16]. Table 2 summarizes the pros and cons of the integrated transformer structures shown in Figure 2.

Table 2. Pros and cons of different integrated transformer configurations.

Performance Parameters	Transformer Structures			
	Interleaved	Stacked	Interstacked	Stacked Folded
Magnetic coupling factor, k	+	++	+++	++
Winding Q -factors	+++	+	++	+
Self-resonance frequency (SRF)	+++	+	+	++
Turn ratio, N	++	+	-	-

A final comment must be made about the BEOL of integration technologies. Bipolar and BiCMOS technologies benefit from optimized BEOL for RF/mm-wave applications with at least two thick copper top metals (i.e., thicker than 2 μm), along with thick intermetal oxide layers to reduce losses and capacitive parasitics. On the other hand, CMOS technologies usually adopt a standard BEOL with thin metals and intermetal oxides, leading to lower quality passive devices with limited SRF. Figure 3 shows a comparison between an optimized BiCMOS process [17] and a 28-nm CMOS technology with standard BEOL [2]. Although at mm-wave frequencies, an optimized BEOL technology produces small performance enhancements, due to increased fringing effects [18], it could have a significant

impact on inductive components operated at lower frequencies, where higher inductances and, hence, larger coils are used. Therefore, inductor design in standard CMOS is still a challenging issue.

Figure 2. Integrated transformer configurations for RF/mm-wave operation. Reprinted with permission from Ref [9]. Copyright 2020, IEEE.

Figure 3. BEOL comparison between (a) mm-wave-optimized BiCMOS technology [17] and (b) 28-nm CMOS technology with standard BEOL [2], Reprinted from Ref [18].

3. The Body Biasing Technique

The body biasing technique can be used to properly modify the threshold voltage, V_T , according to the well-known expression reported below for an n-MOS device:

$$V_T = V_{T0} + \gamma \left(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F} \right) \quad (1)$$

where V_{BS} is the voltage between the body and the source, V_{T0} is the threshold voltage for zero V_{BS} , ϕ_F is the bulk Fermi potential, and γ is the body effect coefficient. Changing V_{BS}

modifies V_T , and, thus, the transistor can be operated at a reduced bias voltage, with almost equivalent characteristics in terms of gain, linearity, and noise. Forward (reverse) biasing of n-MOS (p-MOS) transistors has been largely used at low frequencies, but it has also been proven to be effective for RF/mm-wave operations [19–24]. It is worth mentioning that for n-MOS (p-MOS) transistors, a forward (reverse) body bias turns on the source-to-body diode, and, thus, an exponential DC current flows across the junction. This produces additional power consumption and can also cause latch-up failure. A simple, but effective, solution to limit the junction current is to add a resistor to the body terminal.

The effectiveness of the body biasing technique is highly increased in the FD-SOI CMOS platform, thanks to a wider V_T variation with respect to bulk technologies and the lack of leakage currents. Figure 4a shows the simplified cross-section of a commercial FD-SOI CMOS technology [19–24]. Transistors are fabricated in a 7-nm layer of silicon sitting over a 25-nm buried oxide (BOX). An ultra-thin body (UTB) guarantees an isolated electrical conduction channel between the source and drain, since the channel is fully depleted. Figure 4a shows flipped-well low- V_T (LVT) transistors that use an n-well body and p-well body for n-MOS and p-MOS devices, respectively. In these transistors, the BOX layer works as a second gate oxide, and the body as a gate terminal (i.e., back gate terminal) that allows the tuning of V_T by means of the body voltage. The body gain factor (i.e., the sensitivity of V_T to the body voltage) is almost four times that of the traditional bulk technology (i.e., 90 mV/V). The lower V_T characteristics of flipped-well devices are well exploited in low-voltage ICs.

Figure 4. The 28-nm FD-SOI CMOS technology: (a) simplified cross-section of LVT flipped-well transistors, (b) V_T variation with respect to the body voltage for the LVT flipped-well devices. Reprinted with permission from Ref [25]. Copyright 2019, IEEE.

4. Circuit Topologies for Low-Voltage Operation of RF/mm-Wave Blocks

Geometrical scaling enabled RF/mm-wave applications for nanometer CMOS thanks to transition frequency, f_T , and maximum oscillation frequency, f_{MAX} , values close to, or even higher than, 200 GHz. Such performance improvements have been obtained at the cost of a considerable reduction in the transistor breakdown voltage (BV), and, consequently, of the maximum supply voltage in comparison with equivalent HBT BiCMOS technologies. This poses new challenges for the design of RF/mm-wave CMOS front ends that are still the very bottleneck for several applications (e.g., 5G, automotive radar, and imaging). The turning point is to properly adjust the well-established RF/mm-wave topologies to mitigate low-voltage operation drawbacks. To this aim, the following simple guidelines can be applied to the main circuit blocks, such as LNA, mixers, and PAs:

- Reduce the operative threshold voltage, V_T ;
- Increase the transconductance, g_m , by means of positive feedback;
- Use only one transistor between the supply voltage, V_{DD} , and ground;
- Adopt transformer-based power combining techniques.

A reduction in the V_T is strongly suggested to operate the transistor with a lower gate–source voltage, V_{GS} [26]. It can be achieved by exploiting the body biasing technique in standard CMOS, and more profitably in FD-SOI CMOS technologies, as discussed in Section 3. This approach is very effective, but often requires the implementation of additional circuitry, namely, body biasing generators [27,28]. Moreover, reducing V_T by means of body biasing could be in contrast with the exploitation of such a technique to compensate for the process–voltage–temperature (PVT) variations, which are typically quite large in nanometer CMOS, especially for automotive applications [29,30].

To further increase the gain performance of a transistor operated at low voltage, positive feedback configurations can be exploited, while trading off degradations of other performance parameters (e.g., noise or linearity) [20]. Several implementations of positive feedback in RF/mm-wave blocks adopt reactive coupling (i.e., inductive or capacitive) or an integrated transformer [31–33].

The more effective strategy for the low-voltage operation of RF/mm-wave circuits is to adjust standard topologies to have only one transistor between V_{DD} and the ground. In this perspective, the classical n-MOS cascode topology, largely adopted in high-frequency amplifiers (e.g., LNAs and PAs), thanks to its intrinsic advantages in terms of gain, stability and input–output isolation, cannot be used below a supply voltage of 1 V (i.e., $V_{DD} > 2V_{DS_SAT}$). Viable circuit alternatives could include the following:

- Neutralized common source (CS) topology;
- Folded cascode topology;
- Reactive resonant coupling: capacitive coupling;
- Reactive resonant coupling: transformer coupling.

Figure 5 depicts the low-voltage topologies for an RF/mm-wave LNA stage. It is worth noting that all the reported low-voltage topologies are fully compliant with the standard simultaneous noise/input impedance matching, based on gate, L_G , and source, L_S , inductance. Moreover, they can also be used to implement a PA stage. The choice of the most suitable solution depends on both the application (e.g., frequency band and current consumption/silicon area specs) and the adopted CMOS technology node.

Figure 5. (a) Cascode; (b) neutralized common source (CS); (c) folded cascode; (d) capacitive-coupled (CC) cascode; (e) transformer-coupled (TC) cascode.

The CS topology can be adopted for either LNAs [34] or PAs [35–37], provided that differential cross-coupled neutralization is used to compensate for the gate–drain capacitances, C_{gd} , thus improving the input/output isolation and guarantying frequency stability. Neutralization can be implemented with simple integrated capacitors, C_N , or by means of an additional pair of MOS transistors, to better track the process variation. Neutralized CS is a very effective solution for low-voltage operations (i.e., $V_{DD} > V_{DS_SAT}$), but it requires a very careful design to prevent oscillations in the amplifier.

The folded cascode topology takes advantage of the availability of complementary devices with good performance in CMOS technology, but it requires an additional inductor, L_d , with consequent extra silicon area consumption [38]. It is also possible to save silicon area and, at the same time, increase the voltage gain by replacing the inductor with the primary winding of a transformer, whose secondary coil is exploited as a load inductor, L_{D2} . In this way, positive feedback is easily implemented by means of transformer magnetic coupling [31].

Reactive resonant coupling enables the n-MOS cascode topology to also be used at a very low supply voltage, but at the cost of higher current consumption. It can be implemented by using a series resonant LC network (C_F , L_F), properly sized to exhibit low impedance at the operating frequency, as shown in Figure 5d. Indeed, both inductors, L_{D1} and L_{S2} , resonate with the capacitances at nodes A and B, respectively. The performance of a capacitive-coupled (CC) cascode amplifier is affected by the Q -factor of the LC network and, especially, of the inductor. Therefore, it can also be used a pure capacitive coupling through by-pass capacitors if the area consumption is tolerable [39].

The transformer-coupled (TC) cascode topology shown in Figure 5e takes advantage of an integrated transformer to couple the common-source and common-gate transistors of a cascode stage [40]. Coupling transformer losses (i.e., winding Q -factors and magnetic coupling factor, k) affect the performance of the TC cascode stage; therefore, resonant mode by means of shunt capacitors (not present in Figure 5e) is mandatory. Moreover, the choice of transformer configuration (i.e., interleaved, stacked or interstacked) is of utmost importance. Generally, the TC cascode topology is area saving in comparison with the CC cascode topology, since it requires a transformer instead of three inductors, excluding the load inductor.

Transformer coupling is also a highly convenient method to implement a low-voltage down- (up)-conversion mixer. Indeed, the traditional configuration of the mixer is based on the double-balanced Gilbert cell topology, shown in Figure 6a, which is not suited to low-voltage operations. It can be easily adjusted by using transformer coupling (TC) between the voltage-to-current (V/I) converter and the Gilbert cell, as shown in Figure 6b [41,42]. This solution also improves the linearity performance (i.e., 1-dB compression point), which is crucial in important applications, such as automotive radars [43]. A capacitive-coupled configuration can also be used as shown in Figure 6c.

CMOS low-voltage operations greatly affect the performance of PAs, especially at the output stage. Indeed, the delivered power is limited by the reduced voltage swing required for device reliability (i.e., drain–source break-down voltage, V_{DS_MAX}). A common solution is to adopt a classical cascode topology made up of a thin-oxide CS transistor and a thick-oxide CG transistor to allow for a higher supply voltage. More complex solutions exploit multistacked devices [44,45]. However, both cascode and multistacked topologies are not viable when the PA is integrated within a transceiver operated at low voltage. In this case, only low-voltage circuit topologies (as shown in Figure 5) can be adopted. However, the achieved output power is not sufficient for the application. Integrated transformers can further increase the output power of an RF/mm-wave PA by exploiting the power-combining technique at the output stage [46–56].

Figure 6. Double-balanced mixer topologies: (a) traditional Gilbert cell mixer; (b) TC Gilbert cell mixer; (c) CC Gilbert cell mixer.

Transformer-based PAs have the following benefits, especially when differential topologies are mandatory:

- Implement single-ended-to-differential and differential-to-single-ended conversions, providing inherent virtual ground for differential operations;
- Transform impedance for impedance matching and output power matching;
- Provide simple DC biasing of power devices via the center tap, avoiding the use of RF chokes and DC blocks.

Moreover, transformers can easily combine the output power of two devices, thus nearly doubling the overall power (if the losses of the combining network are negligible). Power combining can be obtained by using voltage-combining transformers (VCTs) or current-combining transformers (CCTS), which are also known as series or parallel combining, respectively.

Figure 7 depicts a two-way implementation for voltage- and current-combining techniques, by using integrated transformers with a 1:N turn ratio. The voltage-combining technique is aimed at summing the voltage produced by each PA unit by exploiting stacked secondary windings, in order to increase the output voltage and, thus, the delivered power of low-voltage CMOS PAs. On the other hand, the current-combining technique is aimed at gathering the current of each PA unit by exploiting the parallel-coupled secondary winding to increase the overall current, thus boosting the output power.

By extending these techniques to M PA units, the output power can be theoretically boosted up to M time, either by using series or parallel combining.

Physical implementations of power combining are greatly influenced by the specific application and adopted integration technology. An important limitation is caused by the integrated transformers, whose losses have to be properly minimized to preserve the power-combining advantage with reasonable silicon area consumption. Figure 8 depicts the simplified layout of an example of a series-combining transformer for the voltage-combining topology in Figure 7a. The transformer exploits only two metal layers (i.e., the upper and thicker metal layers) for both windings, which are coupled by means of an interleaved configuration.

Figure 7. Power-combining techniques (a): voltage-combining (SCT), (b) current-combining (PCT).

Figure 8. Example of an SCT for PA voltage combining.

Unfortunately, both series- and parallel-combining techniques have practical design limitations on the maximum number of PA units that can be profitably combined. Specifically, in the voltage-combining technique, the number of PA units is limited by the optimal impedance of each power device, R_{OPT} , and is equal to the following:

$$R_{OPT} = \frac{R_{LOAD}}{2 \cdot M_S \cdot N^2} \quad (2)$$

where R_{LOAD} , M_S , and N are the load resistance, the number of PA units and the transformer turn ratio, respectively. Indeed, according to Equation (2), when M_S increases, R_{OPT} reduces, thus requiring larger power transistors with lower maximum available gain, due to the RLC parasitics. Therefore, voltage combining is not used for an M_S higher than four.

On the other hand, in the current-combining technique, R_{OPT} is equal to the following:

$$R_{OPT} = \frac{M_P}{2 \cdot N^2} R_{LOAD} \quad (3)$$

where R_{LOAD} , M_P , and N are the load resistance, the number of PA units and the transformer turn ratio, respectively. From Equation (3), it is evident that the current-combining technique is more flexible in the selection of the optimum resistance, since the turn ratio, N , can be properly used to tune the optimum impedance, R_{OPT} . In particular, a larger turn ratio is required to lower the R_{OPT} when a higher M_P is used. Unfortunately, increasing N often produces lossy and area-consuming integrated transformers. Moreover, only integer number turn ratios can be practically implemented.

These drawbacks can be overcome by using a hybrid-combining technique, based on both series and parallel transformers. Figure 9 shows two types of hybrid-combining topologies, namely, voltage–current combining (SPCT) and current–voltage combining (PSCT), both implemented for $M_S = M_P = 2$. Generally, the output powers of $M_S \times M_P$ PA units can be increased up to $M_S \times M_P$ times. This hybrid approach gives more freedom to designers, with respect to pure voltage or current technique, since the optimum resistance is given by the following:

$$R_{\text{OPT}} = \frac{M_P \cdot M_S}{2 \cdot N^2} R_{\text{LOAD}} \quad (4)$$

Figure 9. Power-combining techniques (a): voltage–current combining (SPCT); (b) current–voltage combining (PSCT).

Figure 10 depicts an example of a series–parallel-combining transformer for the circuit topology in Figure 9a. The transformer combines four PA units by means of interleaved coupling, thus requiring only two metal layers. Moreover, the structure maximizes the use of the top metal layer (i.e., the thicker layer of a standard CMOS BEOL), while reducing the need for the second metal layer, which is exclusively used for the underpass connections. It is worth noting that stacked coupling could be used to increase the magnetic coupling and save silicon area, but stacked transformers require at least two thick metal layers to have an advantage [18].

Figure 10. Example of a series-parallel-combining transformer (SPCT) for 4 PA voltage-current combining.

5. Conclusions

This paper has provided the reader with an overview of state-of-the-art low-voltage design techniques for RF/mm-wave ICs, from body biasing for low- V_T operations of nanometer CMOS transistors to reactive resonant coupling for sub 1-V circuits. A special insight was dedicated to transformer-based power-combining approaches to boost the PA output power, especially at mm-wave frequencies. Thanks to proper combinations of the described techniques, several high-frequency applications can be addressed by using sub 1-V CMOS ICs. This process started with RF wireless communications and now involves mm-wave applications, such as W-band automotive radar and beyond. Nanometer FD-SOI CMOS technologies are the natural candidates for future low-voltage RF/mm-wave ICs, especially with thick BEOL for better passive components.

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