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Understanding the Light Detection in an Integrated Novel Electrophotonic Wavesensor Photodetector

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Abstract: This work presents a novel integrable silicon photodetector which can only be conceived as part of a monolithic electrophotonic basic structure formed of a silicon light emitter, waveguide and light detector. That is, it cannot operate as a single electronic or photonic device. The detector presents current gain, and photons reach the depletion region straightforward, allowing the detection of low power light produced by silicon light sources currently in use, which is difficult for existing photodetectors. The waveguide core is made of silicon nitride, and it is simultaneously the insulator in a MOS-like device. The light detection unit is intended for novel seamless electrophotonic platforms, and it is called wavesensor. In spite that the device is a MOS-like structure, it is not a MOSFET neither a lateral bipolar transistor, and one of the main differences with the former is that this is a bulk device working in Punch-Through regime. Being a MOS-like structure, it is fully compatible with standard microelectronics technology. A development of the mathematics involved in its operation is carried out in order to understand the physics of the detector, showing a gain factor in the photocurrent. Computer simulations of the fabrication process and photoelectric response of the device confirmed photocurrent values higher than the expected for a photodiode with efficiency = 1, thus demonstrating a new integrable photodetector with gain, capable of detecting light in the range of nW for electrophotonic applications.

Keywords: photodetectors; detectors; silicon; integrated optoelectronics

Citation: Hernández-Betanzos, J.; Aceves-Mijares, M.; González-Fernández, A.A. Understanding the Light Detection in an Integrated Novel Electrophotonic Wavesensor Photodetector. *Appl. Sci.* **2022**, *12*, 1264. <https://doi.org/10.3390/app12031264>

Academic Editor: Young Tea Chun

Received: 14 December 2021

Accepted: 18 January 2022

Published: 25 January 2022

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1. Introduction

Seamless silicon integrated electrophotonics is the combination of electronic and photonic devices to produce a monolithic circuit which simultaneously controls and manipulates both optical and electronic signals. There are three basic elements considered the bare minimum to obtain an electrophotonic circuit: light emitters in silicon, waveguides compatible with silicon technology, and silicon photodetectors [1,2].

In the past few years, the development of silicon light sources has advanced significantly, and integration of such devices into electrophotonic circuits has been demonstrated [3–8]. However, one of the major challenges to tackle remains the improvement of their relatively low light emission powers [9–11]. One of the most promising silicon compatible light sources reported is the Light Emitting Capacitor (LEC), which uses Silicon Rich Oxide (SRO) as an active light emission layer [12–15]. The light emission of the SRO-based MOS-like structures ranges from the visible to the near infrared, and they are completely integrable with existing photonic elements based on silicon nitride (Si₃N₄). Most importantly, their fabrication is fully compatible with MOS processes. Due to its broad spectrum within the visible range, this kind of light sources can be suitable for chemical or biological sensors. However, they present the disadvantage of the mentioned low emission power as compared to other external light sources, such as externally coupled lasers. Despite

this, SRO-based LECs have been successfully used in electrophotonic chips, and the light has been transmitted across the nitride waveguide and detected by an integrated silicon photodiode in the same silicon chip [5]. Other technologies, such as silicon on insulator use lasers and sensors made of Si-Ge, InGaAs, III/V and other materials that do not have such light power limitations, but they are not compatible with MOS technologies, and consequently, it is not possible to monolithically integrate in silicon electronics [9,16,17].

On the matter of light transmission, photonic devices are currently available in different foundries, including waveguides and other photonic devices [18–20]. A particularly interesting material for light guiding is Si_3N_4 , as it is fully compatible with CMOS processes, it presents good transmission for visible and NIR light, and its refractive index in such range has enough contrast with air and silicon dioxide to obtain adequate confinement [21–23]. In addition, Si_3N_4 has been successfully coupled to LECs, and it has even been coupled to photodetectors to obtain complex integrated sensors [5,24].

Regarding photodetectors, up to now silicon photodiodes have been the main choice for seamless electrophotonic integrated circuits [4,8,16]. The monolithic integration of LECs, nitride waveguides, and silicon planar photodetectors is possible in CMOS technology, and all the elements are auto-coupled to each other, which is an unprecedented advantage. However, distributed electrophotonic functions along the chip will require better light detection capabilities, due to the mentioned relatively low light intensity emitted by LECs, which is in the range of nanowatts [11]. For example, developing integrated systems as lab-on-a-chip will require the simultaneous interaction between light and both chemical and biological elements, a difficult task for such low powers. Then, as an alternative to higher power light sources, which present lower compatibility for integration, we propose the development of more adequate electrophotonic sensors to counteract this limitation by the emitter, as the presently existing photodetectors are not developed within the intimate integration philosophy that electrophotonics offer [25].

The use of the traditional architecture of silicon photodiodes presents some disadvantages in this respect, such as the light passing across a heavily doped layer before photons can reach the active depleted zone. In [19] a variety of integrated photodetector architectures within the frame of electrophotonics are proposed. The photosensors are directly integrated with the waveguide and cannot be used separately as discrete photonic or electronic sensors. The light is directly transmitted to the depletion layer, resulting in lower electron-hole recombination and a higher contribution to photocurrent by the photons in the range of the LEC emission. In addition, the novel approach of seamless relation between guide and detector enables new advantages, such as the possibility of increased photoresponse due to current gain, in which lower light intensities result in higher photocurrents.

In this work, the concept and analysis of a novel waveguide-detector binomial, called wavesensor (WS) for application in electrophotonic integrated circuits is proposed. The photodetector is designed to be integrated with an SRO LEC and with a silicon nitride waveguide. It does not function as a discrete photonic or electronic sensor, but only makes sense as part of an electrophotonic system, in which electrons and photons are intimately interrelated. The light transmitted by the waveguide is injected directly to the active depletion layer. The core of the waveguide is seamlessly integrated as the gate dielectric to a MOS-like structure. The WS biased in the Punch-Through regime allows for light detection in the visible range in the bulk of the device. Amplification of the detected photocurrent is observed in the drain current. The analyses of the physics and simulation results show electric gain for the detected photocurrent in the substrate, meaning the device is not controlled by surface phenomena as regular MOS transistors are. The results show the viability of a unique monolithically integrated capable of detecting powers in the range of nanowatts, meaning a step forward in the integration of SRO light emitters for development of electrophotonics.

2. Materials and Methods

The simulation of the wavesensor fabrication process was carried out with the software SILVACO-Athena, based on the parameters used in the integrated emitter-waveguide-photodiode presented in [5], except for the substrate type and resistivity. The electro-optical response was simulated using SILVACO-Atlas. Different voltage values in drain, gate, source and bulk were fixed and swept to the terminals, and the arriving light was modeled as a uniform beam, with different power and wavelengths.

3. Device Description

A descriptive schematic of the proposed integrated circuit is presented in Figure 1. This shows the LEC, the waveguide, and the photodetector. As can be seen, the wavesensor is a MIS-like structure, with the insulator being simultaneously an integrated silicon nitride (Si_3N_4) planar waveguide core, extended into below the gate contact metal.

Figure 1. Representation of the integrated circuit with the waveguide from the LEC up to the MIS-like WS (a). 2D schematic of the wavesensor, that is a MIS-like photodetector with the waveguide core being monolithically integrated under the gate terminal (b).

In the scheme of Figure 1, the light is produced by an SRO LEC and injected into the silicon nitride waveguide core. The waveguide ends on the WS, and the gate metal is on the top of the nitride core. With this configuration, the light is absorbed directly by the photodetecting region as follows: since the buried SiO₂ lower cladding ends exactly at the edge of the WS, the radiation is transmitted with low losses until it reaches the gate area, and when the SiO₂ cladding reaches the edge of the Si substrate part of the WS, the change

in refractive index allows the transmission of the light from the waveguide to the silicon, right below the gate. The photons transfer energy to the WS to produce electron-hole pairs, which causes drain current variations. Note that this is not a regular photonic or electronic device, as no external light input-output ports exist, and the only way to inject light is through the waveguide core.

To estimate the viability of the concept and its detection characteristics, the phenomena taking place in the device were studied, in order to propose optimal fabrication parameters. Computational simulations were then carried out to confirm the viability and expected behavior of the WS.

Following the process reported in [5], the substrate was a p-doped Silicon with acceptor concentration N_A of $1 \times 10^{14} \text{ cm}^{-3}$. The distance between source and drain L , and the width of the transistor W , were, respectively, $5 \mu\text{m}$ and $1 \mu\text{m}$. Drain and source regions were obtained through phosphor implantation prior to a thermal rediffusion at 1100°C for 180 min. The nitride waveguide/gate insulator was obtained by chemical vapor deposition, and the thickness of the film was 140 nm. The metal used for the contacts was aluminum with thickness of $1 \mu\text{m}$. After the fabrication, electrical and optical simulations were performed. Substrate and source contacts were biased to 0 V, and the gate voltage was -5 V . The drain voltage was varied from 0 V to 5 V. The light source was modeled using a uniform beam with wavelength (λ) of 600 nm and light power (P_{in}) varied from 0 nW to 50 nW, as reported for SRO-based light sources [12]. Figure 2 shows the 2D schematic of the WS.

Figure 2. Schematic of the wavesensor (WS). The red arrows represent the lighting from the nitride waveguide directly into the depletion layer.

4. Electrical Behavior and Photodetection

4.1. Electrical Current

In Figure 3a, the applied voltages on the drain, source, and substrate are 0 V ($V_B = V_S = V_D = 0 \text{ V}$). The gate is biased in accumulation regime and its effect is just to avoid surface currents. The light is detected through the variation of the source to drain current produced by the absorption of the light directly into the depletion layer, below the extended waveguide core. The proposed device operates in Punch-Through regime. The lateral depletion zones of the source and drain overlap when the drain-source voltage V_{DS} reaches the Punch-Through voltage V_{PT} , as illustrated in Figure 3c. An electric current from source to drain is established under this bias condition. As an approximation, the analysis

of the physics will be carried out in a substrate depth corresponding to the middle of source and drain. This reduces the analysis to two PN junctions separated by the depleted substrate below the gate area, as illustrated in Figure 3.

Figure 3. Idealized scheme of the WS showing the charge, electric field and voltage profiles for the WS under thermal equilibrium (a), biased with $V_{DS} < V_{PT}$ (b), biased with $V_{DS} \geq V_{PT}$ (Punch-Through) (c).

Figure 3a shows the charge (Q), electric field (E), and voltage (V) profiles obtained under equilibrium conditions using the depletion approximation [26–28]. Donor and acceptor profiles are assumed to be constant in the N and P zones. The p-n junctions (drain-substrate and source-substrate) are considered abrupt. Under these assumptions, the charges on the depleted zones are as shown in Figure 3, and comply with charge neutrality condition (1):

$$qN_A x_p = qN_D x_n \quad (1)$$

where x_n is the depletion width on the n-regions (drain and source) and x_p the depletion width on the substrate region. As drain and source are heavily doped, the depletion width has a larger extension inside the substrate. The junctions produce a built-in voltage V_{bi} , as shown in Figure 3a. Since the electric charge is constant in the depletion zone, the electric field presents a linear profile with a maximum in the metallurgical junction. Calculating the integral of the electric field, a parabolic voltage profile can be obtained.

Figure 3b shows the profiles when drain is biased. When drain-substrate junction is reversely biased, the depletion width is increased. The depletion width under reverse bias can be calculated using (2) [27,29]:

$$W_D = x_n + x_p \approx \sqrt{\frac{2\epsilon_S(V_{bi} + V_{DS})}{qN_A}} \quad (2)$$

When $V_{DS} = 0V$, the depletion width has an initial value called x_{j0} , also showed in Figure 3. As V_{DS} increases, the depletion regions grow wider, to the point where Punch-Through is reached at $V_{DS} = V_{PT}$. That is, both depletion regions overlap. The Punch-Through voltage (V_{PT}) can be calculated using (3).

$$V_{PT} = \frac{qN_A L^2}{2\epsilon_S} - V_{bi} \quad (3)$$

Figure 3c shows the profiles when $V_{DS} > V_{PT}$ and Punch-Through is assured. The substrate region under the gate is fully depleted. If V_{DS} continues increasing beyond V_{PT} , the electric field increases enough to act on the source-substrate junction. The drain voltage induces a reduction of the potential barrier between source and substrate, as depicted in the bottom of Figure 3c. This can be interpreted as an induced forward voltage on this junction. The barrier reduction and the high drain voltage promotes a current flow towards the drain

on Punch-Through regime. The current density in the depletion region j_{SCR} is space charge limited, and has been proposed as a main current mechanism in devices working in this regime, as expressed in (4) [30–34]:

$$j_{SCR} = \frac{9\epsilon_S\mu}{8L^3}(V_{DS} - V_{PT})^2 \quad (4)$$

where ϵ_S is the silicon permittivity, μ is the electron mobility, and L is the distance between the source and drain. The current j_{SCR} has a quadratic dependence on the drain voltage. As the device is kept in the Punch-Through regime, variation of V_{PT} will produce variation in the j_{SCR} .

An additional current arises as a result of the effect of drain voltage (V_{DS}) on the source. This is represented as an equivalent forward voltage, $V_F(V_{DS})$. For low injection from the source to the depleted region at low electric fields, this current can be expressed as (5) [35–38]:

$$j_n = \frac{qD_n n_i^2}{2\sqrt{\pi}L_D N_A} \exp\left(\frac{qV_F}{kT}\right) \quad (5)$$

where D_n is the diffusion constant for electrons, L_D is the Debye Length, k The Boltzmann Constant, T the temperature, n_i the intrinsic concentration, and V_F is the induced forward voltage caused by the drain voltage, which triggers a potential barrier reduction. Additional carrier generation in the substrate, such as optical or thermal, could also modify the effective V_F , affecting j_n . This perturbation stimulates an excess of current, which can be reflected in the total drain current.

It is also expected an influence of the gate voltage on the substrate surface, affecting its conductivity. However, these phenomena are to be addressed in a future work. For the present study, it was assumed a gate bias point corresponding to flat band or accumulation, making the superficial drain-source current negligible.

4.2. Energy Band Behavior on Dark Condition

Figure 4 illustrates the energy levels of the conduction band (E_C), valence band (E_V) and the Fermi level (E_F) along source, bulk and drain for a WS with p-type substrate. The evaluation is at a middle depth in the n+ wells, where surface effects are negligible.

At this initial condition, drain current is not established due to the potential barriers. When the WS is biased with $V_{DS} > 0$ V, band bending is produced and probability of carrier injection is increased. The drain voltage produces a drain-substrate junction reverse biased, increasing the width of depletion. As the drain voltage increments, the depleted zone in the drain increases, until both drain and source depletion regions overlap. This is known as Punch-Through condition, at $V_{DS} = V_{PT}$. The value of V_{PT} is proportional to the separation L between source and drain. At Punch-Through, the voltage barrier reduces, as shown in Figure 5. Then, an electric current can be established due to the higher carrier injection probability.

4.3. Energy Bands under Illumination Condition

If the drain-source junction is biased beyond Punch-Through condition, and light with an optical power P_{in} is absorbed by the silicon below the gate area, electron-hole pairs are produced in the space charge region between drain and source. This mechanism is depicted in Figure 6.

Figure 4. Energy band diagrams at thermal equilibrium for a WS.

Figure 5. Energy band diagrams for a WS on Punch-Through condition.

Figure 6. Energy diagram for WS on Punch-Through under stimulation of light with absorbed photons with energy E_{ph} . Red dots represent the electrons and blue dots the holes.

Absorbed photons with energy E_{ph} greater than the band gap E_g produce electron-hole pairs, the electric field inside the depletion region separates the pair, and a current I_{ph} is established. If it is assumed that each absorbed photon generates one electron-hole pair, then the current corresponding to photons I_{ph} under ideal conditions can be calculated with (6).

$$I_{ph} = \frac{qP_{in}\lambda}{hc} \quad (6)$$

where h , is the Planck constant, c the speed of light in vacuum, λ the wavelength, and P_{in} the incident optical power. This is the maximum current that can be generated by the absorbed light in a photodiode or any photodetector. However, the transduction of light in silicon present losses due to recombination processes, and only a portion of the generated electron-hole pairs end up contributing to the detectable current I_{opt} , which always is lower than I_{ph} , depending on the quantum efficiency η as indicated in (7):

$$I_{opt} = \eta I_{ph} = \eta \frac{qP_{in}\lambda}{hc} \quad (7)$$

In addition, a Fermi quasi-level variation is produced by the optical carrier excess, and then the potential barrier is additionally reduced, promoting the injection of extra carriers from source to drain. Then, a current of electrons from the source j_n is added to the photogenerated current. Assuming the WS is biased at low voltage, and a low injection regime, j_n current is expressed as (8):

$$j_n = \frac{qD_n n_i^2}{2\sqrt{\pi}L_D N_A} \exp\left(\frac{qV_{Feff}}{kT}\right) \quad (8)$$

Here, V_{Eff} is known as the effective induced source voltage, and is composed by a potential V_F induced by the drain-source bias, plus the optical potential induced by photogenerated carrier excess ϕ_{opt} .

$$V_{Eff} = V_F + \phi_{opt}, \quad (V_{DS} > V_{PT}) \quad (9)$$

The total electron drain current density j_{dtotal} can be expressed as (10):

$$j_{dtotal} = j_n + j_{opt} = \frac{qD_n n_i^2}{2\sqrt{\pi}L_D N_A} \exp\left(\frac{qV_{Eff}}{kT}\right) + j_{opt} \quad (10)$$

Using (7), we can obtain j_{opt} , which is the photocurrent density generated in the substrate within the space charge region. This current can be simplified into (11):

$$j_{opt} = \frac{I_{opt}}{A} = \eta \frac{qP_{in}\lambda}{Ahc} \quad (11)$$

where A , is the cross-section area of the space charge region. In the presented configuration of the device, an optical current of holes is established through the substrate junction. This can be computed using (12) [39,40]:

$$j_p = \frac{qD_p p_{n0}}{L_p} \exp\left(\frac{q\phi_{opt}}{kT} - 1\right) \quad (12)$$

Using this current, and considering that hole and electron currents are of the same magnitude, it is possible to estimate the optical potential as:

$$\phi_{opt} = \frac{kT}{q} \left(1 + \frac{L_p j_{opt}}{qD_p p_{n0}}\right) \quad (13)$$

Combining (9), (10) and (13), the total equivalent drain current density can be expressed as:

$$j_{dtotal} = \frac{qD_n n_i^2}{2\sqrt{\pi}L_D N_A} \exp\left(\frac{qV_F}{kT}\right) + \frac{D_n n_i^2}{2\sqrt{\pi}L_D N_A} \left(\frac{L_p j_{opt}}{D_p p_{n0}}\right) \exp\left(\frac{qV_F}{kT}\right) + j_{opt} \quad (14)$$

in which the second and third terms account for to the presence of light. If the dark current is subtracted, the optical contribution to current j_{dopt} can be identified:

$$j_{dopt} = \frac{D_n n_i^2}{2\sqrt{\pi}L_D N_A} \left(\frac{L_p j_{opt}}{D_p p_{n0}}\right) \exp\left(\frac{qV_F}{kT}\right) + j_{opt} \quad (15)$$

Remember j_{opt} represents the photocurrent density, taking into account quantum efficiency. Then, the ratio of j_{dopt} to j_{opt} delivers a value which, in case of being larger than 1, indicates an optical gain. This is β expressed in (16):

$$\beta = \frac{j_{dopt}}{j_{opt}} = \frac{D_n n_i^2}{2\sqrt{\pi}L_D N_A} \left(\frac{L_p}{D_p p_{n0}}\right) \exp\left(\frac{qV_F}{kT}\right) + 1 \quad (16)$$

This is the gain of the WS.

4.4. General Summary of the Principles of Operation

The WS integrates a light emitter, waveguide, and a photodetector. In spite that it is a MOS-like structure, its operation is significantly different from the usual electrical amplification mechanisms. First, the proposed sensor is a bulk device, not a surface one. The metal gate has the only purpose of controlling the surface to avoid superficial current flow. The waveguide is also the dielectric under gate, making these devices electrophotonic

and not electronic nor photonic. The device works in Punch-Through condition, extending as much as possible the sensing region length, increasing the photon conversion. In addition, the light is directly absorbed in the depleted region, without passing through highly doped or non-fully transparent materials. In Punch-Through condition, the high electric field moves the carriers towards the drain terminal. Drain current consists of two components: one produced by the carriers generated by light, and another made by electrons injected from Source. In the presence of light, the latter is increased due to a reduction of the barrier in the source-substrate interface, adding extra carriers to those directly photogenerated. This results in a gain on the photocurrent.

5. Results

Figure 7 depicts a cross-section of the device in the Punch-Through regime as obtained by fabrication process simulation using SILVACO-Athena.

Figure 7. WS obtained in Athena-Silvaco. Red lines show the edge of the depletion width when the drain is biased on Punch-Through.

The drain and source diffusions are heavily doped and have a depth junction of around 4 μm . This is due to the thermal treatment necessary in SRO-based light emitters, which is 1100 $^{\circ}\text{C}$ for 180 min [5]. As mentioned, the fabrication process was simulated using these thermal treatment conditions because the device is intended to work with an embedded SRO emitter, for full and monolithic integration.

To simulate its photoelectric behavior, the gate was biased at $V_{GS} = -5$ V, in order to promote hole accumulation in the surface. This way, the drain current can be exclusively controlled by the drain-source voltage, and current effects due to surface phenomena are avoided. The drain-source voltage applied was $V_{DS} = 5$ V, causing the overlap of the depletion zones around drain and source (Punch-Through condition). For the wavelengths of interest, the absorption depth in silicon is located inside the depletion region, approximately from 0.1 μm to 10 μm for respective wavelength limits of 400 nm and 800 nm [27,41]. Figure 8 shows the electric field profile for the WS under the mentioned bias conditions.

Figure 8. Electric Field inside the simulated WS. The direction is showed with arrows and the magnitude is represented in logarithmic scale with color levels. V_{DS} was 5 V, V_{BS} was 0 V and V_{GS} was -5 V.

The strongest electric field is located close to the drain zone, caused by the V_{DS} voltage. If electron-hole pairs are produced in the space charge region, the electric field transports the electrons into the drain terminal, and the holes are separated towards the substrate. Note the accumulated region in the surface, indicating no surface current can go through. Figure 9 shows the drain current as a function of drain voltage, considering both dark and light stimulation conditions.

As mentioned, a negative value of V_{GS} prevents carrier transport through the surface, and the current is dominated by carrier generated in the substrate. The drain current-voltage behavior under this condition fits a quadratic curve. This is consistent to the mechanism of space charge limited current. If drain current in dark condition I_{Ddark} is subtracted from the total observed current when there is light I_D , it can be obtained the contribution of light to the drain current I_{Dopt} . If the ratio of this value to the ideal photocurrent (I_{ph}) is larger than one, it can be concluded that the device exhibits an optical gain β_{opt} , as predicted by the previous analysis. This is presented in (17):

$$\beta_{opt} = \frac{I_D - I_{Ddark}}{I_{ph}} \quad (17)$$

Figure 10 shows such photocurrent ratios for different optical powers and drain voltage.

Figure 9. Drain current as function of drain voltage under illumination for different optical powers.

Figure 10. Photocurrent ratio, β_{opt} , for different optical power as a function of drain voltage.

β_{opt} is approximately 100 for $V_{DS} = 2$ V when light power is 10 nW. It reaches 400 when $V_{DS} = 5$ V. Note that, although the gain increases with the drain voltage, the dark current is

also incremented. Then, there is a compromise between photocurrent gain and keeping the dark current low. It can be seen that the obtained gain is reduced when the optical power is increased. In spite more research is needed to better understand this phenomenon, this can be related to the variation of the Fermi quasi-level produced by the photo generated carrier excess. That is, the higher the input light power, the more influential the effect of photogeneration on the source barrier. The variation of the potential height as obtained by the simulations can be observed in the Figure 11.

Figure 11. Potential profile for different drain bias and light stimulation. Light produces a reduction of the potential height in the source-substrate edge. The caption shows a zoom view of the specified range.

When voltage is applied to the drain, the drain-substrate junction is reversely biased, causing a reduction of potential height in the source-substrate junction as compared to equilibrium position. Incident optical power produces further potential reduction, promoting an additional injection of electrons from the source to the drain, thus obtaining a flow of carriers larger than the produced by electron-hole generation only, given place to the gain current in the WS. This indicates that the observed electro-optical gain phenomenon is due to a light-induced reduction of the potential barrier in the drain-substrate junction, as predicted from the analysis presented in the previous section.

6. Conclusions

In this paper, we propose a new electrophotonic sensor named wavesensor, conceived to be integrated with a silicon light source and a waveguide. The physics and mathematics involved in its operation have been developed, and a technological process parameters were suggested. The compatibility of the device with CMOS standard process has been demonstrated through computational simulation. It was mathematically demonstrated that light in the visible range is detected in the bulk and not in the surface, so the WS is a bulk device. The surface should be in accumulation regime to avoid parasitic currents. Light in the visible range, with powers in the order of nanowatts produces a photocurrent that is amplified by the WS. The silicon nitride waveguide core assures direct coupling with both the low optical power light source and the WS, in such a way that photons are injected directly to the depleted region without passing through a highly doped region. The photocurrent gain has a dependence on drain voltage. Computational simulations corroborated the mathematical model developed.

Author Contributions: Conceptualization, J.H.-B., A.A.G.-F. and M.A.-M.; methodology, J.H.-B., A.A.G.-F. and M.A.-M.; formal analysis, J.H.-B.; investigation, J.H.-B. and M.A.-M.; data curation, A.A.G.-F.; writing—original draft preparation, J.H.-B. and A.A.G.-F.; writing—review and editing, A.A.G.-F. and M.A.-M.; visualization, J.H.-B.; supervision, A.A.G.-F. and M.A.-M. All authors have read and agreed to the published version of the manuscript.

Funding: This project has received funding from the European Union’s Horizon 2020 research and innovation program under the Marie Skłodowska-Curie grant agreement No 801342 (Tecniospring INDUSTRY).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The simulation data that support the findings of this study are available in INAOE institutional repository [42].

Acknowledgments: The authors acknowledge the support from CONACyT of Mexico.

Conflicts of Interest: The authors declare no conflict of interest.

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