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Characteristics of a Novel FinFET with Multi-Enhanced Operation Gates (MEOG FinFET)

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Abstract: This study illustrates a type of novel device. Integrating fin field-effect transistors (FinFETs) with current silicon-on-insulator (SOI) wafers provides an excellent platform to fabricate advanced specific devices. An SOI FinFET device consists of three independent gates. By connecting the various gates, multiple working modes are obtained. Compared with traditional FinFETs, the multi-enhanced operation gate fin field-effect transistor in this study combines independent gates by connecting the selection modes; thus, a possible operation can be performed to attain a FinFET with five equivalent working states in only one device. This novel function can enable the device to work with multiple specific voltages and currents by connecting the corresponding gate combinations, augmenting the integrated degrees and shifting the working modes, thereby meeting the different needs of high-speed, low-power, and other potential applications. Further, the potential applications are highlighted.

Keywords: multi-enhanced operation gate fin field-effect transistor (MEOG FinFET); silicon-on-insulator (SOI); operation in various states; independent gates

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Citation: Wan, H.; Liu, X.; Su, X.; Ren, X.; Luo, S.; Zhou, Q. Characteristics of a Novel FinFET with Multi-Enhanced Operation Gates (MEOG FinFET). *Appl. Sci.* **2022**, *12*, 11279. https://doi.org/10.3390/app122111279

Received: 22 October 2022
Accepted: 4 November 2022
Published: 7 November 2022

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1. Introduction

With the rapid development of science and technology, significant changes have occurred since the emergence of the MOSFET some decades ago. The novel technologies, materials, structures, and other related exploration factors make the development of semiconductor devices immeasurable. The level at which semiconductor devices have developed cannot be underestimated and various research studies have emerged in succession, from the original MOSFET to current devices such as silicon-on-insulator (SOI) fin field-effect transistors (FinFETs). After continuous exploration, a variety of novel devices have been fabricated to replace the previous ones. The practical applications of these devices are also constantly developing and expanding. They are used in various scenarios, such as for low power consumption or high performance. Among them, FinFETs, which are novel devices, have significant research prospects. They can be used to resolve a series of problems during device miniaturization. They are valuable novel semiconductor devices that can be used in future technical processes. The continuous sizes reductions for traditional MOSFET devices and their gate control ability have led to a severe short-channel effect (SCE) and a series of problems, such as severe threshold voltage roll-off, sub-threshold swing weakening, and increased leakage currents. Thus, the FinFET has become a mainstream device used to overcome SCE [1–3]. It has further contributed to the development of other devices. With the large-scale application of transistor-integrated circuits showing a blowout geometric or even exponential growth and the progressive introduction of relevant integrated circuit control methods in all professions and trades, their application scenarios have increased from simple to complex, from conventional to adverse environments, and from commercial to industrial applications. Semiconductor-based IC chips are used everywhere and play a significant role in all aspects and walks of life. With the large-scale application of semiconductors, the proper arrangement of the appropriate devices for specific scenarios to adapt to the corresponding work requirements is of great

significance. The application spectrum of semiconductors is wide. Thus, choosing the appropriate types of devices based on various aspects for a specific application is also important. Complex and specialized applications also require the optimal selection of devices. In the traditional transistor structure, the gate that controls the flow of the current can only control the ON and OFF states of the circuit on one side of the gate, which belongs to a planar structure. As a 3D architecture, a FinFET can also control the connection and disconnection of the circuit on both sides of the gate. The gate surrounds the channel from three sides and the three-dimensional structure is used to replace the planar device to enhance the control ability of the gate. However, owing to the quasi-planar structure, the width of the FinFET can only be increased in line with the quanta of the fin height [4]. The width quantization results in numerous issues in FinFET-based circuit design, especially in terms of the static random access memory, which has self-conflicting design requirements and requires appropriate transistor sizing for cell stability [5]. SOI FinFETs are multi-gate structures that can reduce the leakage current and improve the control of the device [6]. Combined with the SOI process already applied in the traditional two-dimensional planar MOSFET, a novel and improved FinFET called SOI FinFET is fabricated. As the technology enters the nano-node generation, seeking a better device structure compatible with the Si-based process flow is a good way to promote the drive current and product competition [7]. By adopting various novel FinFET-based technologies, some problems can be properly resolved. This device combines the advantages of the two devices, leading to effective integration. The unique structure of SOI devices has many advantages: (1) as an insulating layer with an insulation function, the oxide layer can reduce the parasitic capacitance of the source and drain, meaning it has a lower delay and dynamic power consumption than bulk silicon devices; (2) owing to the existence of the insulation layer, an additional back gate bias can be exerted, and this structure also has little influence on the threshold voltage, meaning SOI devices are more suitable for low-power applications; (3) SOI devices also have better subthreshold characteristics than other devices and the leakage current is also smaller; (4) SOI devices do not have the latch-up problem, which can be effectively resolved.

2. Device Fabrication

For the device explained in this study, based on the combination of SOI and FinFET technologies, the SOI FinFET devices are produced based on other existing bulk silicon devices. Thus, one novel device structure is shown in Figure 1.

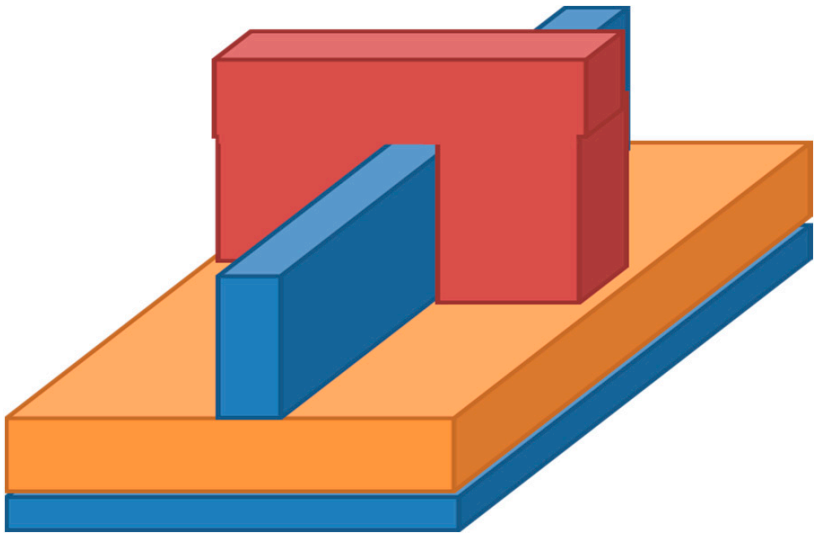


Figure 1. Device diagram.

This structure shown in Figure 2 is basically an SOI FinFET device with three independent gates, composed of gate1 on one side of the channel side wall, gate2 on the top of the middle of the fin channel, and gate3 on the other side of the channel side wall. Gate1 and gate3 have similar structures. Generally, the three gates are isolated from each other by an isolation dielectric layer. The FinFET device has multiple independent gate structures. In terms of the process, the SOI substrate should first be prepared, followed by the main structure (FinFET), by following the general process. Subsequently, the dielectric inter-gate isolation layer is gradually adopted in the subsequent processes to form three independent gates.

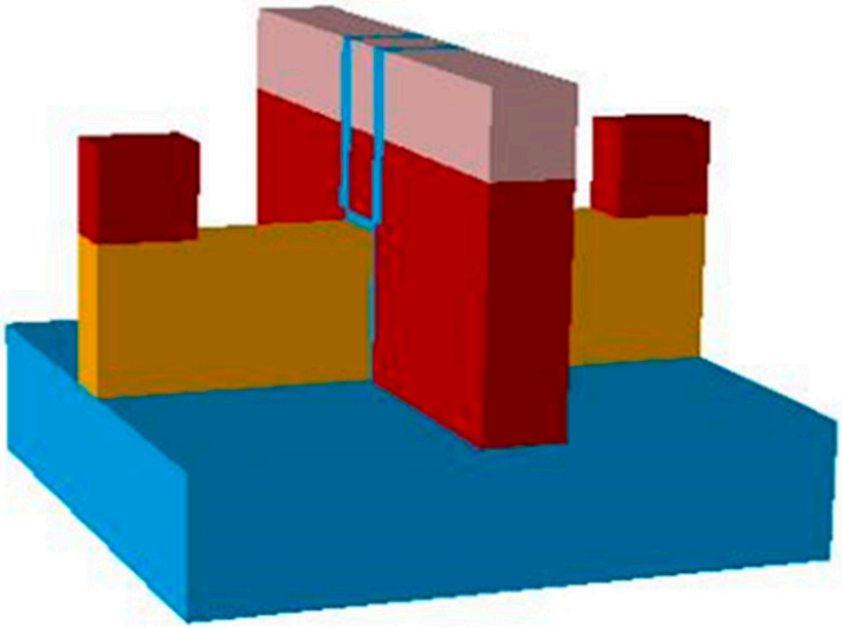


Figure 2. Device structure diagram.

The specific steps are shown in Figure 3. As can be seen, this structure can reduce the process loss and complexity. The basic dimensions are listed: H_{fin} = 30 nm, W_{fin} = 10 nm, Lg = 12 nm. By directly introducing the relevant inter-gate isolation process steps in the gate oxide layer stage, the self-aligned isolation can be effectively completed, possible interference between different adjacent steps can be avoided, the isolation quality can be guaranteed, and the process can be completed in one composition. Moreover, the device composition process is based on the existing process, avoiding complexity and reducing the process cost. Thus, it is more suitable for the current mainstream FinFET process. As shown in Figure 3:

(1) The SOI substrate is first prepared as the basis for the next steps;
(2) The p-well is formed by doping p-type impurities, and boron is used for the p-type impurities here. In this step, the process is similar to the conventional process;
(3) The fin structure is fabricated using repeated photolithography and step-wise etching;
(4) Subsequently, the gate oxide layer deposition stage follows. Following the deposition of the relevant gate oxide, the chemical mechanical polishing step is used to flatten the surface and facilitate the development of the subsequent steps;
(5) The relevant masking layer is deposited to prepare for the next photolithography etching step. Photoresists are used as the masking layer in the process;
(6) The gate oxide layer at the specified scale is formed through another photolithography and etching;
(7) The implantation masking layer is deposited again to pre-treat the subsequent source-drain doping;

(8) The ion implantation doping stage dopes the n-type impurities, and phosphorus is used for the n-type impurities. Consequently, the impurity ion implantation at the source-drain end is completed;
(9) Thus, the structure of the total gate is constructed and the preliminary structure of the gate is completed through the relevant deposition and photolithography steps;
(10) Next, the masking layer of the photoresist deposition step is performed again to prepare for the subsequent lithography and etching;
(11) Photolithography and etching are again performed to construct a self-aligned position hole for the subsequent gate isolation dielectric layer;
(12) The deposition of the relevant isolation dielectric finally forms the multi-gate isolation structure with an independent gate;
(13) The electrode contact of the back channel is formed.

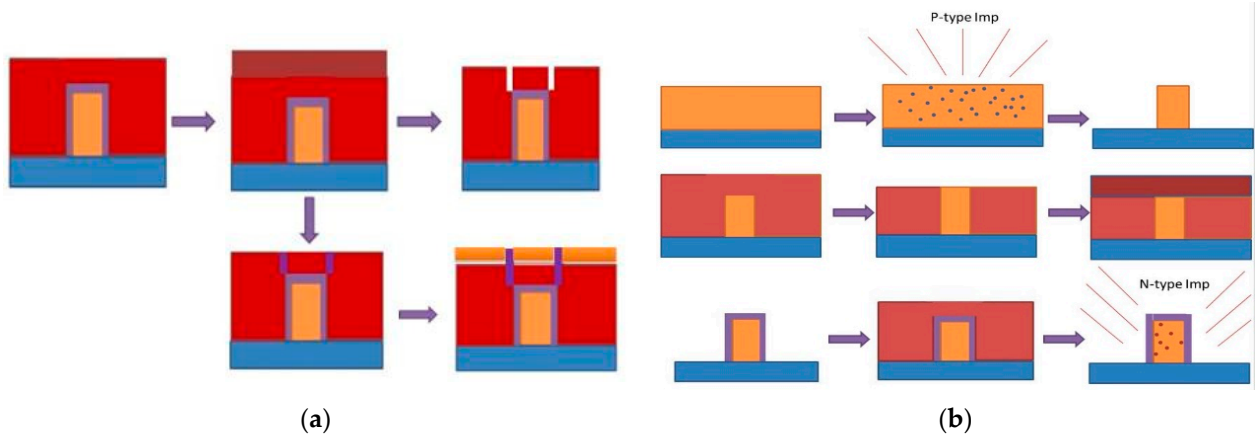


Figure 3. Device construction procedures: (**a**) procedure I (**b**) procedure II.

Through the aforementioned detailed introduction of the construction process, the construction of the target device in this study is completed based on the mainstream process, which can reflect the universal and effective application of the process, simplify the relevant steps, and facilitate the implementation for large-scale industrialization and rapid production and application.

3. Results and Discussion

Based on the constructed device, the relevant TCAD software is used to simulate some characteristics of the relevant devices, and the various simulation results are displayed and analyzed to explore the functionality of the device. Moreover, differing from the traditional FinFET, the SOI FinFET in this study has three main independent gates: gate1, gate2, and gate3. The multi-gate-independent structure provides several optional combined control methods, which can be seen in Figure 4. Because the device is based on a more symmetrical gate structure, it has the following open states: (1) only gate1 or gate3 is open, which is the MODEL1 state; (2) only gate2 is open, which is the MODEL2 state.;(3) when gate1 or gate3 and gate2 are open, this is the MODEL3 state; (4) only gate1 and gate2 are open, which is the MODEL4 state; (5) when gate1, gate2, and gate3 are all open, this is the MODEL5 state.

Before providing a further explanation for the relevant results, some comparisons with the traditional model are made; that is, transfer characteristic and output characteristic are presented in Figure 5, respectively. MODEL5 is taken as an example to present the performance of the novel device.

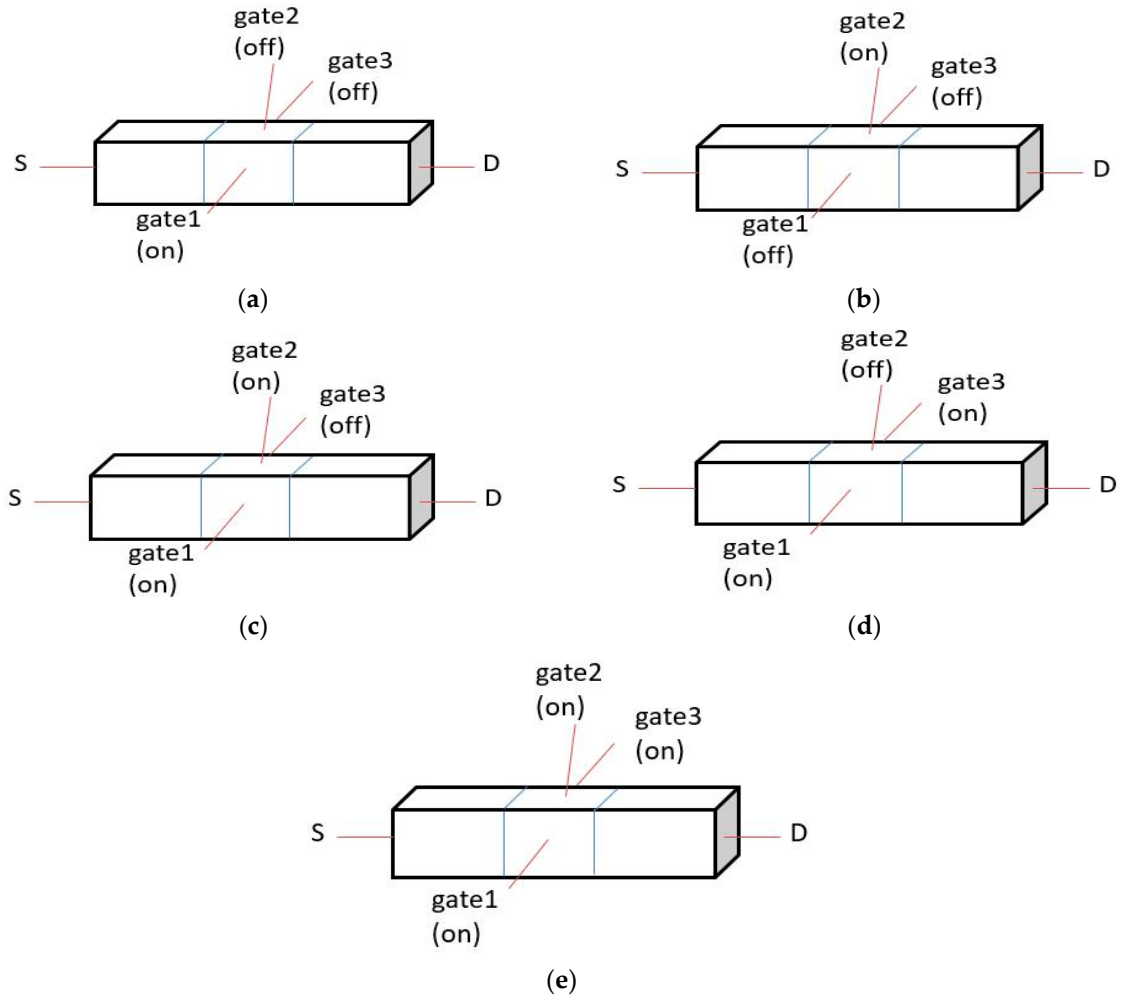


Figure 4. Working mode diagram: (**a**) MODEL1 mode state; (**b**) MODEL2 mode state; (**c**) MODEL3 mode state; (**d**) MODEL4 mode state; (**e**) MODEL5 mode state.

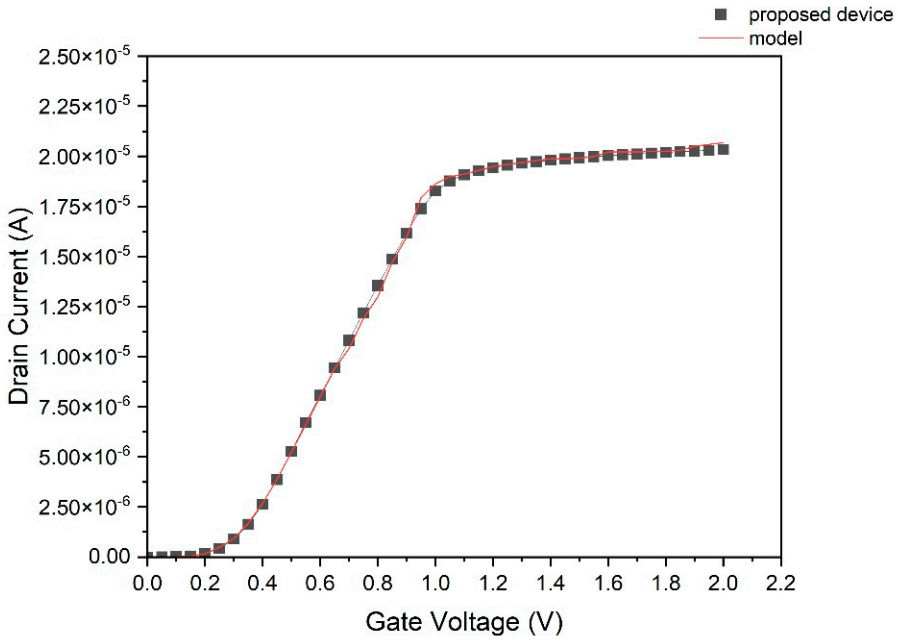


Figure 5. Transfer characteristic curves: TCAD simulation of the device used in this study and the traditional device model.

Obviously, the results demonstrate that this kind of device has emerging applications. In Figure 5, the transfer characteristic curve of the device used in this study is in a balanced state, but the traditional device model is in a non-stable state. Under the same conditions, it needs more time to be in a working state. In Figure 6, the output characteristic curve of the device in this study is still in a balanced state compared with the traditional device model curve within an accepted spectrum. Then, this novel device can be applied in specific scenes.

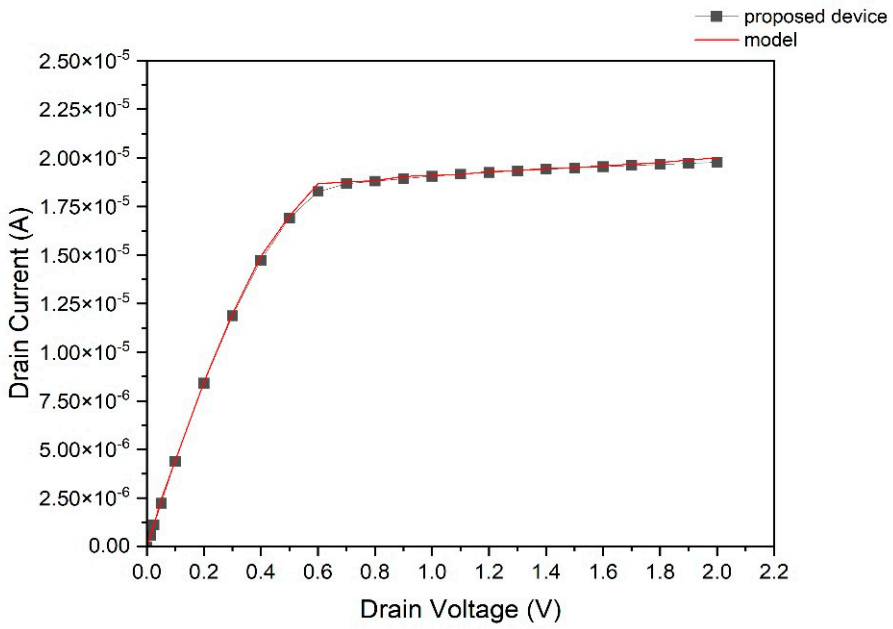


Figure 6. Output characteristic curves: TCAD simulation of the device used in this study and the traditional device model.

In each selected access mode, the specific state and relevant electrical characteristic curves are shown in Figure 7, according to which the transfer characteristic curve (Id-Vgs) of the independently controlled SOI FinFET device proposed in this study under different modes of operation is reflected. As seen, the ON state current of the FinFET device is significantly influenced by the different modes of operation. In Figure 7, one state is the case in which a single gate is on; that is, MODEL1 state mode. This is the side gate ON state. For this transfer curve, gate1 or gate3 is on and the other gates are off; approximately one state in Figure 7 is also the case in which a single gate is open, i.e., the top gate is open, which is the MODEL2 state. Here, gate2 is open and the other gates are closed. At this time, the relevant transfer characteristic curve in this state is presented; thus, the MODEL3 state in Figure 7 is a dual-gate control method that differs from the previous single-gate control method, whereby the top gate is open (gate2 is open) and a side gate is open (gate1 or gate3 is open), enabling gate1 or gate3 and gate2 to be open simultaneously. The corresponding transfer curve appears in this state. In Figure 7, one state is also the double-gate open state. At this time, a similar situation occurs and the top gate is closed (gate2 is in the closed state), whereas the side gates are in the open state (gate1 and gate3 are opened simultaneously), which can result in the MODEL4 working state mode, in which gate2 is closed and both gate1 and gate3 are open. For the final state in Figure 7, all gates are in the open state; that is, the top gate and the side gates on both sides are in the open state, which is similar to the general multi-gate FinFET device. Here, gate1, gate2, and gate3 are in the open state, which corresponds to the working state mode of MODEL5. Here, the corresponding transfer characteristic curve surfaces. The specific comparison of these multiple operating modes is shown in Figure 3. In each mode, the transfer characteristic curve (Id-Vgs) is shown under the same coordinates to allow an obvious and intuitive mutual comparison. Under this comparison, the unique curves under each working state

can also be obtained comprehensively, which can be used as a relevant reference for the appropriate matching of the working environment in practice and as a reference manual. As seen in Figure 7, in the case of MODEL5 (where all gates are open), which is equivalent to the traditional FinFET, the ON current Id is maximal. The minimum current appears in MODEL2. Owing to the quantum constraint effect, the peak current occurs near the fin center. Therefore, all gates in the FinFET significantly influence the current and the three gates are strongly coupled. Therefore, MODEL5 has a significant coupling effect and a large current is obtained. When gate2 is closed (MODEL4), the coupling between the top and side gates will be interrupted. In addition to reducing the control ability of the gate, the additional electric field from the top gate also has a significant impact on the reverse charge layer formed by the side gate [5]. Therefore, MODEL4 has a lower current than MODEL5. In addition, in MODEL3, the coupling between gate2 and gate1 or gate3 is eliminated; thus, the current in MODEL3 is less than that in MODEL5. Comparing the current in MODEL4 with that in MODEL3, as seen in the structure, because the fin height is much larger than the fin width in our proposed FinFET, the side gate (gate1 or gate3) can induce more reverse-charged layers than the top gate (gate2); thus, the current in MODEL3 will be smaller than that in MODEL4. Similarly, this also explains why the current in MODEL2 is much smaller than that in MODEL1. Compared with MODEL3, because the top gate (gate2) is closed in MODEL1, the gate control ability is reduced, resulting in a lower current in MODEL1 [1]. The semiconductor industry has been studying the famous "Moore's law" for more than half a century [8]. By constructing such a novel structure, the five working states of MODEL1, MODEL2, MODEL3, MODEL4, and MODEL5 enable the adoption of this valuable device in different fields.

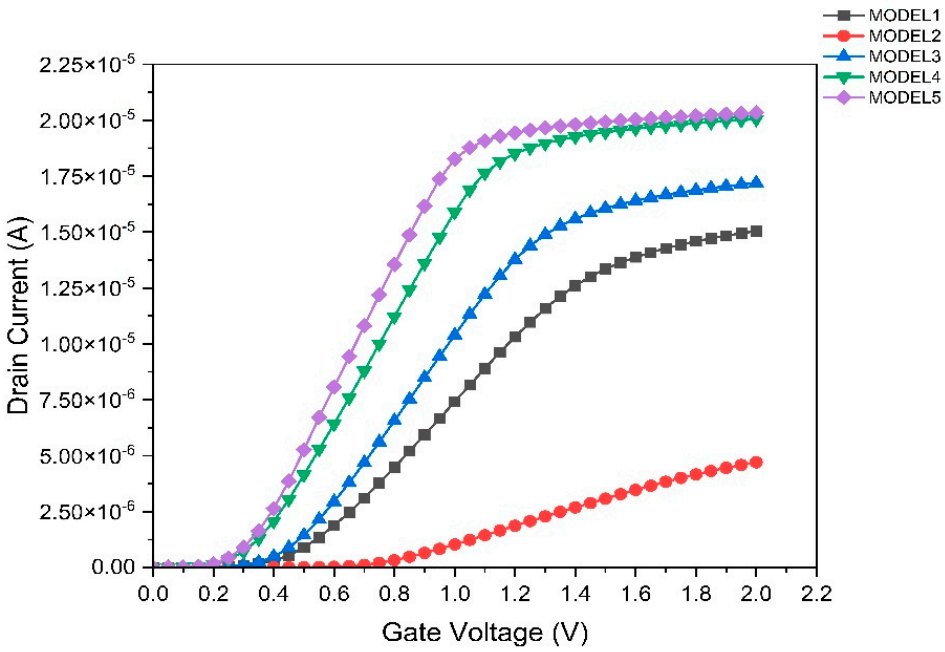


Figure 7. Transfer characteristic curves for five independently controlled SOI FinFET devices under different modes of operation.

Some key electrical parameters also vary in different operation modes; that is, these parameters can be flexibly controlled in different states, reflecting the adaptive performance of the device under multi-mode operation. These are listed in Table 1 together with the specific data. For example, the characteristic parameters such as the threshold voltage (Vth), saturation current (Isat), off-state leakage current (Ioff), subthreshold swing (SS), and drain-induced barrier reduction (DIBL) achieved using our proposed methods are listed and compared with the existing traditional devices. When all gates are open, the proposed FinFET will be equivalent to the traditional single-fin FinFET; thus, the characteristics of

MODEL5 in the FinFET are similar to the traditional FinFET. However, compared with the traditional FinFET, our proposed FinFET shows significant Vth controllability, which can provide five Vth levels according to different modes of operation, can improve the flexibility of the circuit design, and can provide methods to adapt to different working conditions. For example, MODEL1 and MODEL2 can be adopted in low-power applications, whereas MODEL4 and MODEL5 can function in high-speed applications. Moreover, compared with the previously proposed FinFET, when the device is used as an access transistor in the memory, the delay and noise are reduced. Owing to having the same channel electrostatic field environment, the leakage current (Ioff) values of our proposed FinFET are almost the same as the traditional FinFET under five different working modes [1]. For the five working states, because the gate control capacity levels differ, the Vth, SS, and DIBL values also differ, as shown in Table 1. These parameters are critical to the performance of the devices; thus, extensive knowledge of these parameters is essential. Among the various FinFETs, the SOI FinFET shows a suppressed leakage current and superior SCEs [9]. It limits the depletion region of the source-drain region, which can improve the leakage current, SCE, and sub-threshold characteristics of the device [10]. Tremendous progress has been made recently regarding the extremely thin SOI material technology [11], as well as other advances; thus, their significance is apparent.

Table 1. A comparison of the electrical parameters in the different models.

MODEL	Vth (mV)	Idsat (10^{-5}A)	Ioff (10^{-9}A)	SS (mV/dec)	DIBL (mV/V)
MODEL1	501.6	1.50	5.39	166.5	74.2
MODEL2	757.9	0.471	6.54	167.1	86.2
MODEL3	459.6	1.72	3.08	153.8	66.0
MODEL4	338.2	2.00	1.55	96.9	55.2
MODEL5	319	2.03	1.55	91.8	52.4
PROTOTYPE	319	2.03	1.55	91.8	52.4

For our proposed structural device, the output characteristic curve, i.e., the Id-Vd curve, is also presented, as shown in Figure 8, which represents the curves under different working conditions. One state in Figure 8 shows the situation in which a single gate is turned on (MODEL1). Here, the side gate is turned on, which is the curve mode of MODEL1. For MODEL2 in Figure 8, the top gate (gate2) is open and the other gates are closed. This is a novel control mode with different states. The relevant output characteristic Id-Vd curve in this state is presented. In Figure 8, MODEL3 shows the double-gate control. In this state, the top gate (gate2) is open and one of the side gates (gate1 or gate3) is open. The Id-Vd curve under MODEL4 is also shown in Figure 8. This state is still in the double-gate control; however, the top gate (gate2) is closed, whereas the side gates are in the same open state. At this time, gate1 and gate3 are simultaneously opened, which results in MODEL4, with gate2 being closed and gate1 and gate3 being open. Finally, Figure 8 also shows a state in which gate1, gate2, and gate3 are on, and this corresponds to the working-state mode of MODEL5. In this mode, the corresponding transfer characteristic curve is presented. A specific comparison of these multiple modes of operation is also shown in Figure 8.

The different output characteristic curves under the five working states are similar based on the aforementioned analysis process when describing the transfer characteristic curve. However, the curves vary owing to the different couplings under the multiple-gate control structure. This also shows the good adaptability of the device in multiple working states from the statistical data used for the characteristic curve.

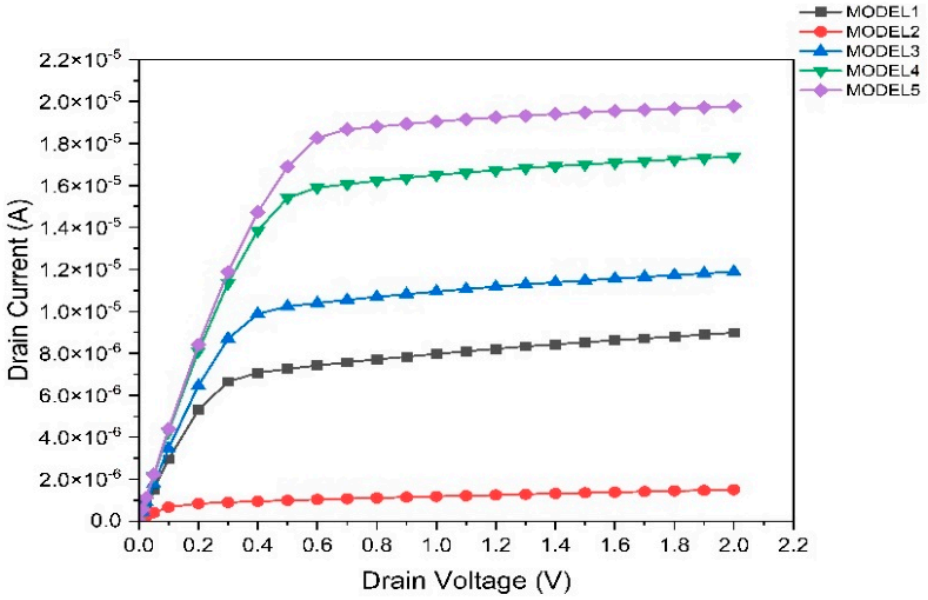


Figure 8. Output characteristic curves for five independently controlled SOI FinFET devices under different modes of operation.

4. Conclusions

This study proposed a novel multi-independent gate-controlled FinFET technology. This device has quantitative strengths. As the device's critical dimensions are scaled down to the nanometer-scale, this FinFET with high speed, a high density, lower power, and high scalability can allow better control channel carrier transport [12]. This multi-gate device has good application prospects. The FinFET can obtain an improved ON state driving current (Ion); thus, it can increase the speed of the circuit [13]. Compared with traditional FinFETs, our proposed FinFET not only has the inherent advantages of the SOI FinFET but also provides a variety of different modes to meet the different needs of high-speed, low-power, and other potential applications; that is, by combining independent gates connecting selection modes, a single FinFET with 5 working states can be attained. This novel feature enables the device to function using multiple specific voltages and currents by connecting the corresponding gate combinations, augmenting the integrated degrees, and shifting the working modes. In addition, parameters such as the threshold voltage can be effectively controlled with a reduced delay. A tradeoff between high speed and stability can also be obtained in memory and other applications, which will increase its development potential and prospects in various fields.

Author Contributions: Conceptualization, H.W.; methodology, H.W.; software, H.W.; validation, H.W.; formal analysis, H.W.; investigation, H.W.; resources, H.W., X.L., X.S., X.R., S.L. and Q.Z.; data curation, H.W.; writing—original draft preparation, H.W.; writing—review and editing, H.W.; visualization, H.W.; supervision, H.W. and X.L.; project administration, X.L.; funding acquisition, X.L. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the National Natural Science Foundation of China (No. 41875026).

Conflicts of Interest: The authors declare no conflict of interest.

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