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Design of 2–16 GHz Non-Uniform Distributed GaN HEMT MMIC Power Amplifier with Harmonic Suppression Network

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Abstract: In this paper, an ultra-wideband (UWB) power amplifier (PA) on a 0.25 μm gallium-nitride (GaN) on silicon carbide (SiC) high-electron-mobility transistor (HEMT) process, operating in Ku-band, is presented. The broadband PA design is based on the four-stage non-uniform distributed amplifier structure. In order to improve the efficiency of the PA, a harmonic suppression network is added at the output of the drain artificial transmission line. At the same time, a capacitor is connected in series at the input of the gate, which is used to compensate for the phase offset of the gate and increase the cut-off frequency of the PA. The final gate width of the first stage is 0.56 μm, and the other three-stage gate widths are all 0.32 μm. Over the frequency range of 2–16 GHz, the simulated results of this NDPA exhibit a power-added efficiency (PAE) of 16.6–27%, a saturated continuous wave (CW) output power of 35–37 dBm, a small signal gain of 9.1–11.6 dB, and output return losses of 5–15 dB.

Keywords: GaN-On-SiC HEMT; non-uniform distributed; power amplifier; ultra-wideband; harmonic suppression

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1. Introduction

Modern electronic systems play an important role in various military and civil contexts, and there are also increasing demands on the capabilities of electronic systems [1]. The power amplifier (PA) in the transmitter is one of the important components of an electronic system [2–4], which has a high demand on its wide bandwidth, high power, and high efficiency [5,6]. At present, the distributed amplifier (DA) has been analyzed and developed to improve bandwidth [7], in which the artificial transmission lines (ATLs) can absorb the input and output parasitic capacitances of field effect transistors (FETs).

For a DA, in order to improve the bandwidth, some scholars have connected the capacitor in series at the input of the gate to reduce the equivalent capacitance. The authors of [8] suggest that the gain of a DA depends on transistor size, as higher gains require multiple cascade structures. Since the drain current flows in both the source and load directions, which is one of the reasons for the inefficiency of the DA, typical DA topologies have an absorption resistance in series with the drain and gate terminals [9–12]. In order to replace the absorption resistance, some scholars use a non-uniform distributed amplifier (NDPA) structure [13–15]. By adjusting the characteristic impedance of drain ATLs, the drain current can be stacked step by step. The output power of the DA is determined by V_d^2/R_L, wherein V_d is the power supply voltage and R_L is the load impedance that the amplifier is driving. As the supply voltage is limited by the transistor technology, some scholars reduce the load impedance to improve the output power [9].

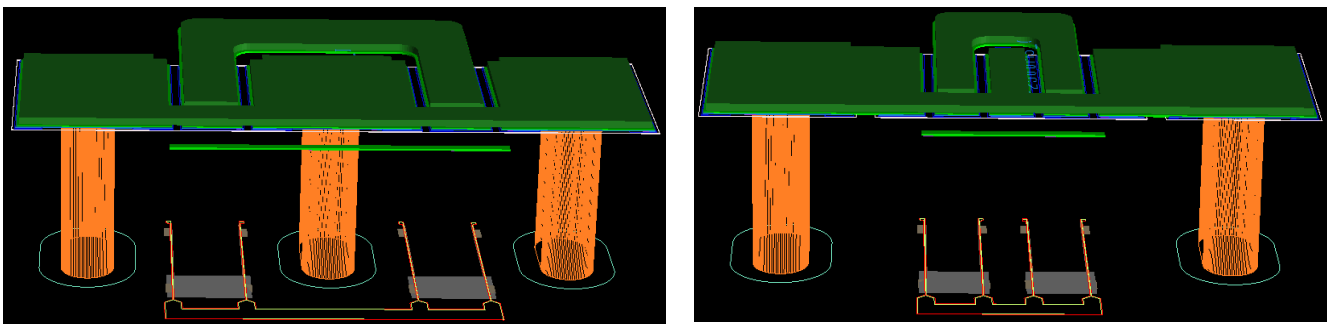
As more and more industrial and academic researchers focus on radio frequency (RF) ultra-wideband (UWB) amplifiers [16–20], in recent years, UWB amplifiers with

excellent performance and a novel structure have been published [17,21–26]. A new biasing technique was proposed to prevent bandwidth degradation caused by cascading multiple amplifiers [8]. This design comes with a power added efficiency (PAE) of 18.4–36.5% and a large signal gain of 15.8–17.5 dB in the 2–20 GHz frequency range. A novel trifilar transformer and space-saving architecture was proposed using the WIN NP15 process [2]. In the 4–16 GHz frequency range, the highest PAE is up to 34%, the large signal gain is 8.7–14.6 dB, and the output power is 37.8–40.2 dBm. The authors of [3] designed a 6–18 GHz NPDA using a 0.25 um gallium-nitride (GaN) high-electron mobility transistor (HEMT). In order to increase the output power, it halves the characteristic impedance by doubling the phase of the drain line. The PAE is 13.6–33.8%, the large signal gain is 8–13 dB, and the output power is 6.8–14.5 W. A harmonic suppression method was proposed by [27]. This design, with the presence of the balun, achieved high-power-level even-order harmonic suppression properties. Moreover, the simulated results show a minimum linear gain of 10.8 dB, with the saturated output power of 44.6 dBm in the 2–6 GHz band. The author of [9] states that for NDPA to achieve a higher efficiency, the load impedance must be reduced and the total FET periphery must be increased. However, the current technology cannot maintain bandwidth and improve efficiency at the same time.

In this work, the factors affecting the efficiency of the NDPA are analyzed in detail, and a harmonic suppression network at the output of the drain ATLs is proposed. Section 2 introduces device models used in the design of circuits. Section 3 starts from the transmission line theory, explains the basic principle of the DA, as well as the design method and the final design schematic diagram. Section 4 shows the simulation results in detail and the conclusion is in Section 5.

2. GaN on SiC HEMTs

Gallium arsenide (GaAs) and GaN materials are used for NDPA design. The GaN HEMT, with higher breakdown voltage and higher output power, is more suitable for making UWB and high-power amplifiers [28]. The 0.25 μm GaN/SiC HEMT process on 4-inch wafers with 100 μm SiC substrates was used for this design. In order to provide a reliable operating breakdown voltage at high-drain bias conditions, the process utilizes a source-coupled field plate design. Additionally, this process offers two interconnected metal layers, high-reliability metal–insulator–metal (MIM) capacitors and precision TaN resistors for full monolithic microwave integrated circuit (MMIC) designs. The process employs through-substrate vias for ground connections and provides an optional transistor layout with low-inductance via connections under each source pad. Figure 1 shows two versions of the process; one is ISV (transistor with individual back-via) and the other is OSV (transistor with outside back-via). Since the DA needs a larger ground area for heat dissipation, the ISV structure is chosen for the design, but at the same time, the size of the FET is also increased.



(**a**) (**b**)

Figure 1. Transistor model: (**a**) ISV model, (**b**) OSV model.

According to the work manual [29], when the gate width is 0.25 μm, the saturation output power at 10 GHz is 5 W/mm with V_d = 28 V and I_d = 100 mA/mm. When the drain bias voltage is at 28 V, the cut-off frequency is 25 GHz, the maximum oscillation frequency is 75 GHz, and the maximum stable gain at 10 GHz is 19.5 dB. A typical transfer curve is shown in Figure 2a with the device exhibiting transconductance with a peak of approximately 180 mS/mm at V_d = 28 V and the gate width at 4 × 100 μm. When the drain bias voltage is 28 V and the gate width is 4 × 50 μm, the transconductance is more than doubled to 75 mS/mm. Under the same drain bias voltage, it can be seen that the current of 0.4 μm gate width is twice as large as that of 0.2 μm gate width, and it increases with the increase in gate bias voltage. The full I-V curve with 0.4 μm FETs for the technique is shown in Figure 2b. Figure 2b exhibits well-behaved characteristics and a maximum current density over 325 mA/mm (at V_g = 0 V, V_d = 28 V). It can be seen that, under the same drain bias voltage, changing the gate voltage greatly changes the output current. The different gate and drain bias voltages of the transistor represent different working states of the power amplifier. When the drain bias voltage is at −1.5 V, it means that the power amplifier is working in a class AB working state. Compared with the gate bias voltage at −0.2 V, the efficiency is increased, but the linearity is reduced.

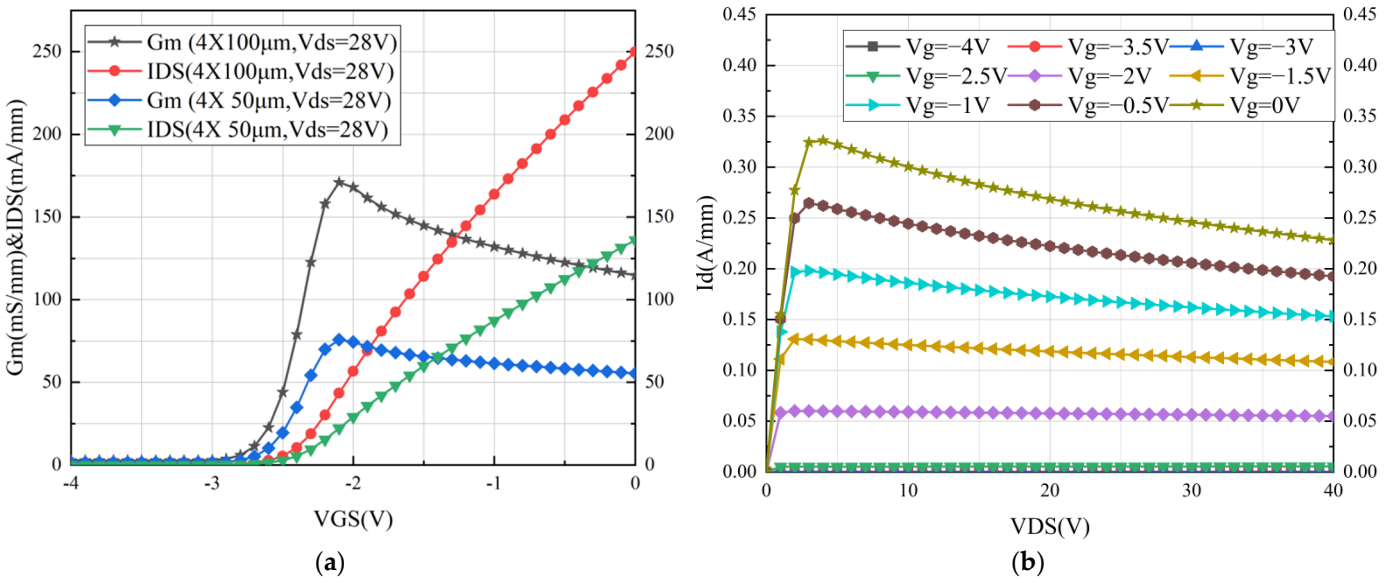


Figure 2. The characteristics of 0.25 μm GaN HEMT: (**a**) Transfer curve of 0.25 μm GaN HEMT, (**b**) I-V curve of 0.25 μm GaN HEMT.

It is known that the maximum cut-off frequency of this process is 24.5 GHz. In order to obtain the best matching transistor performance, the large signal parameters of the transistor are obtained. The saturated output power density of the transistor is 5 W/mm, the PAE is 65%, and power gain is 14.1 dB. When the input power of GaN devices is 27 dBm at 10 GHz, the transistor's PAE reaches its maximum, but the gain is severely compressed at this time.

The small-signal equivalent circuit of the GaN HEMT device is shown in Figure 3. R_s, R_d, and R_g represent the source, drain, and gate parasitic resistances, respectively. C_{gs}, C_{gd}, and C_{ds} represent the capacitance between gate–source, gate–drain, and drain–source, respectively. L_g, L_s, and L_d, respectively, represent the parasitic inductance of leads between gate–source, gate–drain, and drain–source. Through the frequency response characteristics of a single GaN transistor, we can intuitively identify the factors that affect the bandwidth of the amplifier. At low frequencies, parasitic capacitance is generally considered to have no effect on the gain amplitude of the amplifier, but as the frequency increases, the parasitic capacitance will cause the gain amplitude of the amplifier to roll down. Therefore, in order

to increase the cutoff frequency, a slightly smaller-sized transistor should be selected, and a trade-off should be made with the gain.

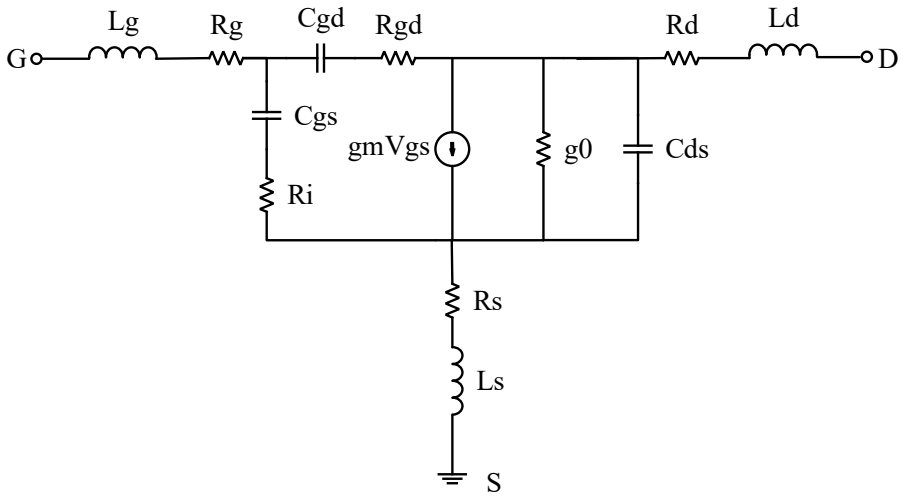


Figure 3. GaN HEMTs equivalent small-signal model for transistors.

3. Circuit Design

3.1. Principle of Distributed Amplifier

According to the analysis of the transistor small-signal model in the previous section, the parasitic capacitance of the transistor has an adverse impact on the gain and bandwidth of the amplifier. The basic principle of the DA is to connect the gate and drain parasitic capacitors of a certain number of transistors side-by-side with inductive devices, so that the gate and drain ATLs are constructed to overcome the gain roll-down caused by transistor parasitic capacitance. Therefore, on one hand, the parasitic capacitance of the transistor is absorbed by the inductive element, which effectively inhibits the high frequency gain drop caused by the parasitic capacitance of the amplifier. On the other hand, the parasitic capacitance and the inductive element form a T-type matching network greatly expand the working frequency band of the amplifier [12]. As shown in Figure 4, the DA is composed of a gate ATL and a drain ATL, and the characteristic impedance of the transmission line is Z_0. The gate input and drain output ATLs are coupled through the transconductance of the transistors.

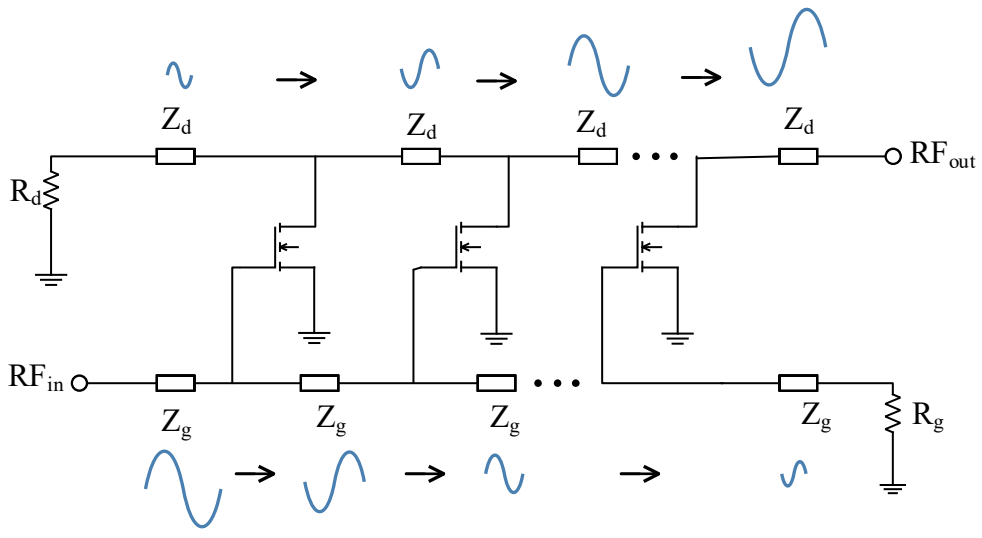


Figure 4. Topology of a typical DPA.

As described above, the DA is based on the transmission line theory. Take a double transmission line with length ΔZ; as long as ΔZ tends to be infinitesimal, the equivalent lumped parameter circuit of this transmission line can be considered to have infinitesimal resistance, conductivity, inductance, and capacitance. The equivalent model circuit is shown in Figure 5.

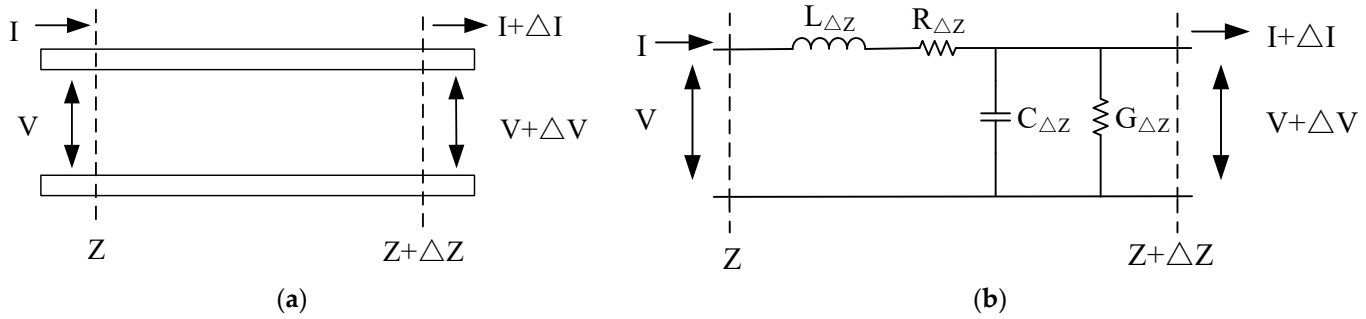


Figure 5. Model of double transmission line: (**a**) Double transmission line, (**b**) Equivalent model.

For the limited transmission lines, it can be considered as a distributed parameter circuit cascaded by several ΔZ-length transmission lines. Using Kirchhoff's law of voltage and current for the circuit shown in Figure 5b, we can obtain Formulas (1) and (2). The specific meaning of the variables involved in the formula will not be repeated. Formulas (3) and (4) are finally obtained by solving simultaneous equations, where γ is the complex propagation constant, which is a function of frequency, and its expression is Formula (5). α is the attenuation constant and β is the phase shift constant, as is explained in detail in [12].

$$v(z) - R\Delta z \cdot i(z) - jwL\Delta z \cdot i(z) - v(z + \Delta z) = 0 \tag{1}$$

$$i(z) - G\Delta z \cdot v(z + \Delta z) - jwC\Delta z \cdot v(z + \Delta z) - i(z + \Delta z) = 0 \tag{2}$$

$$v(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{3}$$

$$i(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z} \tag{4}$$

$$\gamma = \alpha + j\beta = \sqrt{(R + jwL)(G + jwC)} \tag{5}$$

Formula (6) denotes the characteristic impedance Z_0 of the transmission lines. At this point, the voltage and current on the transmission line are correlated by characteristic impedance, that is, $Z_0 = \frac{V_0^+}{I_0^+} = -\frac{V_0^-}{I_0^-}$.

$$Z_{0,n} = \frac{R + jwL}{\gamma} = \sqrt{\frac{R + jwL}{G + jwC}} \tag{6}$$

According to the transmission line theory, the propagation constants of the gate and drain ATLs of the DA can be written as $\gamma_g = \alpha_g + j\beta_g$ and $\gamma_d = \alpha_d + j\beta_d$. In the case of the lossless transmission line $\alpha_g = \alpha_d = 0$, then $\gamma_g = j\beta_g$ $\gamma_d = j\beta_d$. Figures 6 and 7 show the equivalent circuit model of the gate and drain ATLs. As shown in Figure 6, after the RF signal is transconducted to the drain transmission line, the signal can be transmitted from the left and right directions, so the gain of the DA is divided into forward gain and reverse gain. The forward gain is the gain from the signal input port to the signal output port, by adjusting the propagation constant and impedance of each transmission line to make the phase velocity of the signal propagation on the input and output transmission lines equal, as the forward traveling wave amplified by each stage of transistor can be added in phase at the drain transmission line port. The reverse gain is the gain from the signal input port

to the terminal impedance of the drain transmission line [13]. The existence of reverse gain is one of the factors of low efficiency.

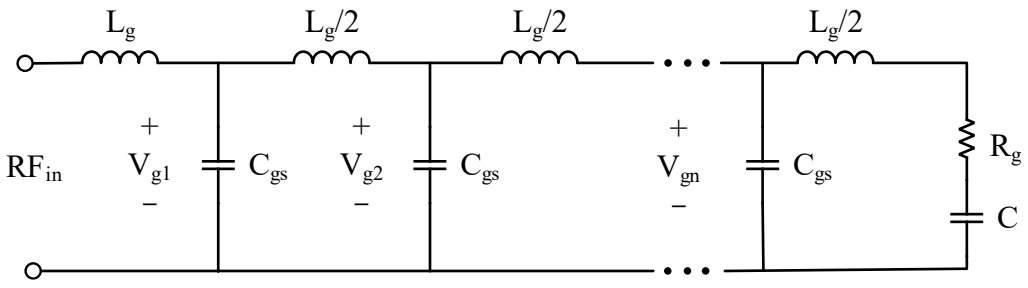


Figure 6. Equivalent circuit of gate ATL.

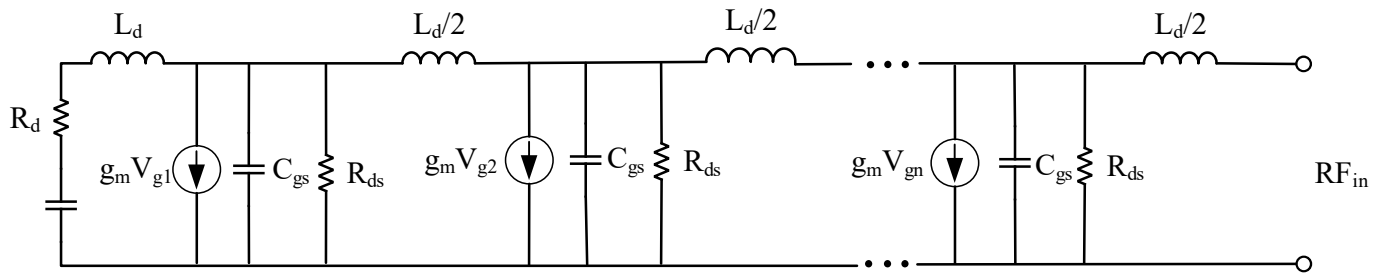


Figure 7. Equivalent circuit of drain ATL.

The authors of [7] show that the circuit can be matched to the best load by adjusting the size of different transistors. The current flow diagram of any two adjacent transistors in an inhomogeneous structure can be seen in Figure 8. According to the principle of the microwave, the positive and negative currents in Figure 8 can be expressed as Formulas (7) and (8). When the characteristic impedance of each drain transmission line in the non-uniform structure satisfies Formula (9), the reverse current offsets almost all the current flows to the load, which improves the efficiency of the distributed amplifier.

$$i_n^- = \frac{1-k}{1+k} n i_d, i_n^+ = n i_d - n i_n^- = \frac{2}{1+k} n i_d \tag{7}$$

$$i_{n+1}^- = \frac{k}{1+k} i_d, i_{n+1}^+ = i_d - i_{n+1}^- = \frac{1}{1+k} i_d \tag{8}$$

$$k = \frac{n}{1+n} \tag{9}$$

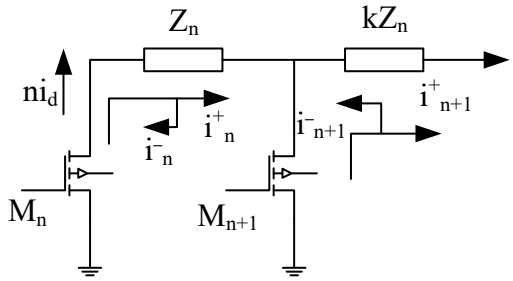


Figure 8. Current flow diagram of adjacent transistors in non-uniform structure.

As shown in Figure 9, in order to better absorb the reverse current of the drain transmission line, some scholars replace the absorption impedance with a nonuniform

drain transmission line, by changing the characteristic impedance $Z_{0,n}$ of each transmission line. On account of the parasitic capacitance, the transistor can affect the cut-off frequency of the amplifier and the C_{ds} is much smaller than the C_{gs}, so the gate ATL cutoff frequency is the most important factor limiting NDPA bandwidth. In order to improve the cutoff frequency, most scholars connect small capacitors in series at the gate to reduce the value of the equivalent capacitance $C_{g,n}$. Additionally, the series resistor $R_{g,n}$ supplies power to the gate bias voltage, and the RC structure can also improve the stability of the entire circuit.

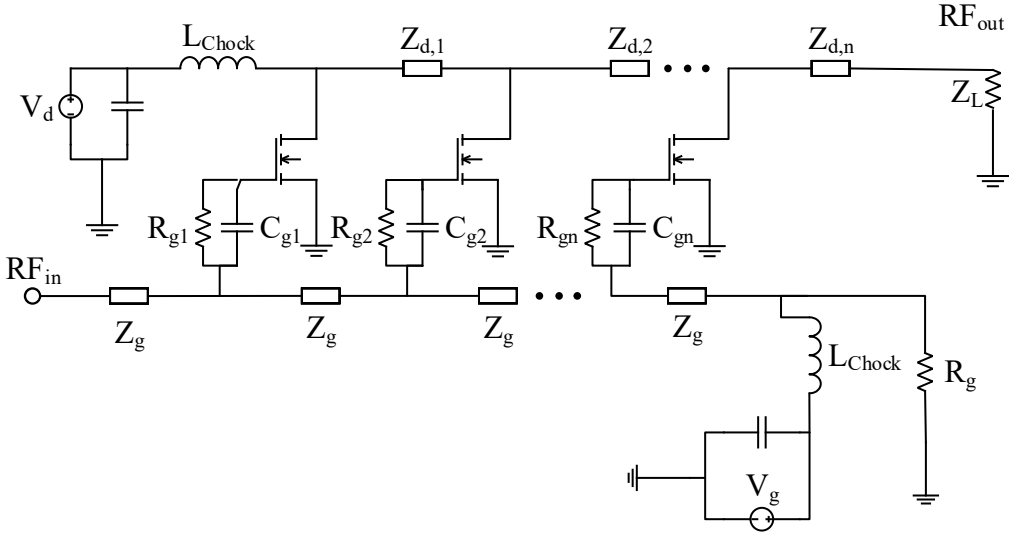


Figure 9. A typical NDPA topology for improving cutoff frequency.

Due to a large resistor, R_g is connected in parallel to provide a bias path. If the NDPA adopts the method of ATLs to absorb C, the device can be simply equivalent to pure resistance characteristics. Therefore, the nTH power-saving circuit can be simply equivalent as shown in Figure 10 [9,10].

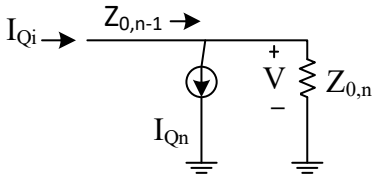


Figure 10. Equivalent circuit diagram of the nTH core.

It is assumed that if all devices in the NDPA have the same bias conditions and excitation levels, to ensure the best match of the NTH tube, then

$$R_{ds,n} = \frac{V}{-I_{Q_n}} = Z_{0,n}\left(1 + \frac{\sum_{i=1}^{n-1} I_Q}{I_{Q_n}}\right) = Z_{0,n}\left(\frac{\sum_{i=1}^{n} W_Q}{W_Q}\right) \tag{10}$$

Which defines the output impedance per millimeter of the device,

$$R_{ds}(\Omega\text{mm}) = R_{ds,n} W_{Q_n} = Z_{0,n} \sum_{i=1}^{n} W_{Q_i} \tag{11}$$

$$Z_{0,n} = \frac{R_{ds}(\Omega\text{mm})}{\sum_{i=1}^{n} W_{Q_i}} \tag{12}$$

In order to ensure maximum power transmission to the load, so

$$\frac{R_{ds}(\Omega\text{mm})}{R_L} = \sum_{i=1}^{n} W_{Q_i} \tag{13}$$

It can be seen from Figure 10 that the total gate width of the NDPA is determined by the output impedance of each millimeter wave of the device and the terminal impedance of the circuit, and the output power is determined by the total gate width of the device. The output impedance per mm is determined by the material and process. Through the simulation of the DC characteristics of the model, when the drain bias is 28 V, the gate width is 0.5 mm and the point of the current is 146 mA. At this time, the impedance per millimeter of the 0.25 μm GaN HEMT is calculated to be 94 Ohm·mm, and only this result is used for approximate calculation. The total gate width of the device was calculated and determined as 1.88 mm according to Equation (13). In order to trade-off chip size and gain, a four-section topology is adopted.

Figure 11 shows the simulation values of each device in the actual simulation schematic. Since the DA sacrifices efficiency to expand bandwidth, the efficiency of the DA is generally low. In order to improve efficiency, a harmonic suppression network is added to the drain output port in the actual design.

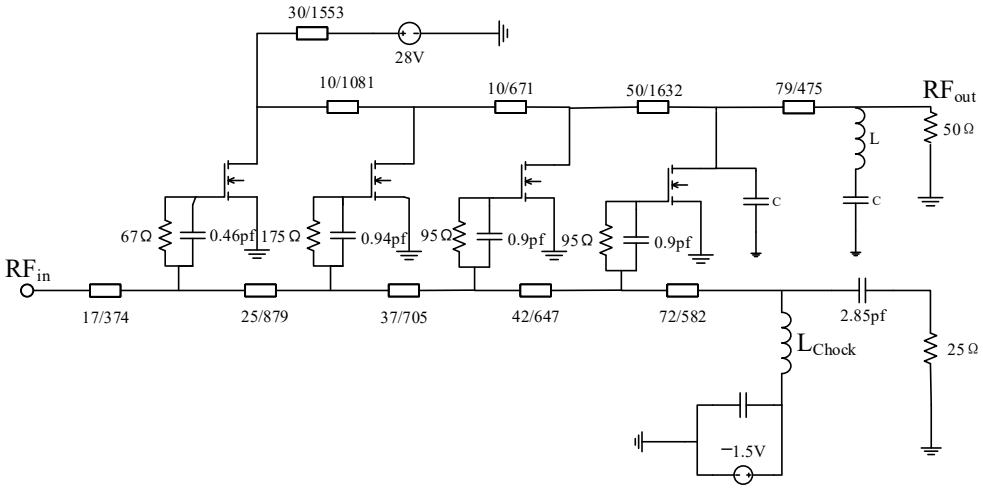


Figure 11. Actual schematic of a four-stage NDPA.

3.2. Simulation Analysis

The principle of the NDPA is to add the current on the drain ATLs step-by-step, but the offset of the current phase will bring about inefficiency. Figure 12a shows the variation of the output current of each stage of the drain. It can be seen that both the amplitude and phase of the current have changed, and the ideal situation is that the currents at all levels are superimposed in phase. Figure 12b shows the change of current at the drain output under different frequencies. It can be seen that the amplitude and phase of the output current are inconsistent at different frequencies. In the frequency range of 3 GHz–9 GHz, the amplitude difference of the current is small, but the phase difference is up to 90°. When the frequency is 16 GHz, the current amplitude reaches the maximum, but the phase difference between the other frequency points can reach nearly 180°. In the simulation process, adjusting the length and width of the microstrip line can greatly affect the phase, but at the same time change the impedance value calculated in Table 1.

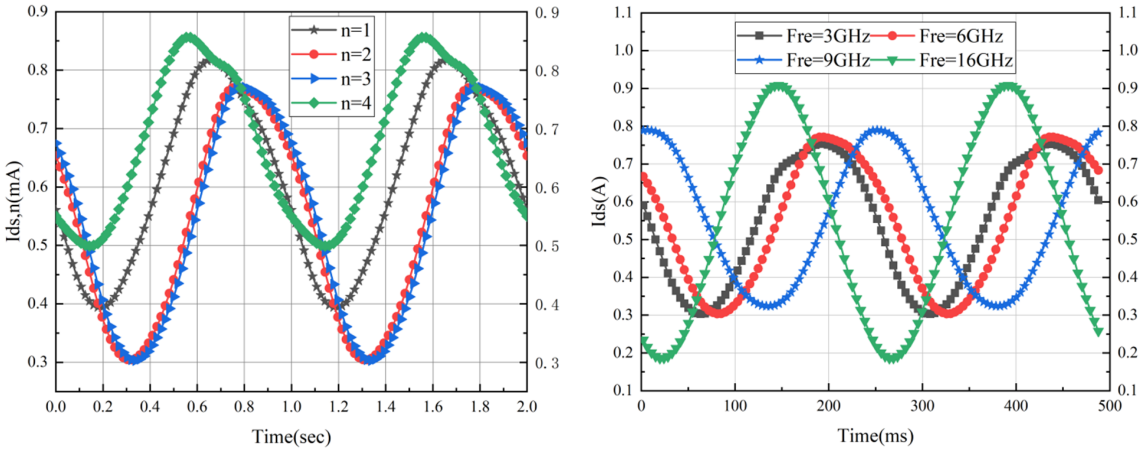


Figure 12. Drain current variation: (**a**) Variation of current in each stage of drain with time domain, (**b**) Drain final stage current as a function of frequency.

Table 1. The cell NDPA design.

GaN NDPA Design	FET Number	W_Q (mm)	$R_{d,n}$ (Ohm)	Z_0 (Ohm)
FET Rds (Ohm/mm) = 94	1	0.5	188	188
RL (Ohm) = 50	2	0.32	294	115
Calculated total FET width (mm) = 1.88	3	0.32	294	84
Number of cells = 4	4	0.32	294	64
Supply voltage (V) = 28				

Figure 13 shows the small-signal changes when the gate bias voltage changes from −0.2 V to −2 V. When the gate voltage bias is −0.2 V, the drain current is 790 mA. When the gate voltage bias is −1.5 V, the drain current is 335 mA. When the gate voltage is offset at −2 V, the drain current is 154 mA. The small-signal gain decreases gradually with the increase in the gate bias voltage, the return loss S11 changes little with the gate bias voltage, and the return loss S22 fluctuates at high frequencies with the increase in the gate bias voltage.

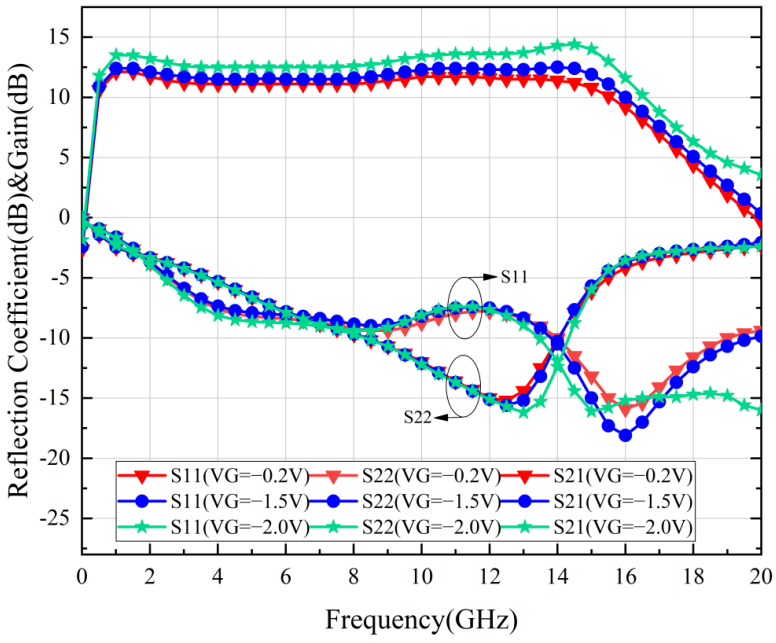


Figure 13. Influence of gate bias voltage on small signal.

There are errors between the capacitance and inductance in the model library and the actual devices. Therefore, the sensitivity analysis and simulation of the key components of the circuit are carried out. Figure 14 shows the sensitive elements in the NDPA circuit. It can be seen from Figure 14a that the value of the gate absorption resistance R and the value of the length of the microstrip line L3 have a great impact on the overall performance of the circuit. Figure 14b shows the Monte Carlo analysis of the length of the microstrip line L3, which is part of the gate artificial transmission line used to connect the first-stage gain unit and the second-stage gain unit. The Monte Carlo simulation is used to sample 2000 points. The median length of L3 is 272 μm. The actual simulation length is 271 μm.

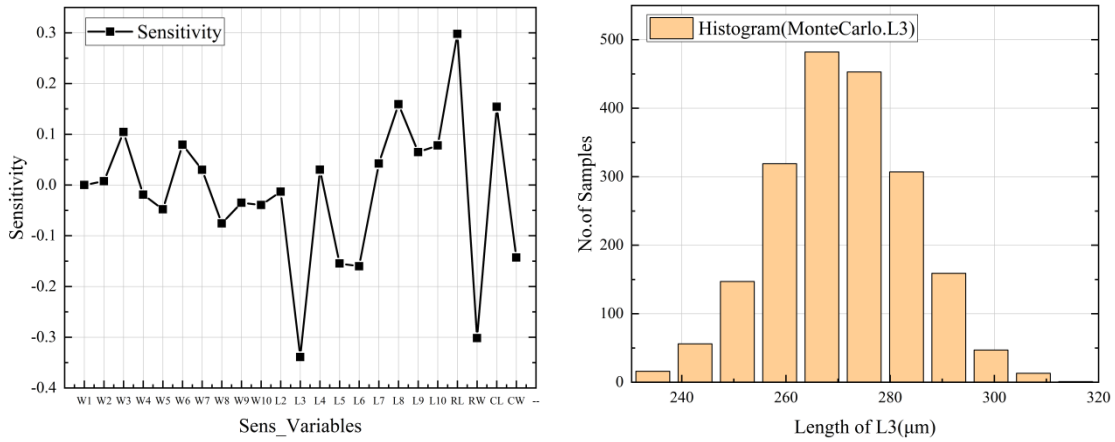


Figure 14. Layout simulation results: (**a**) Sensitivity analysis of key components, (**b**) Monte Carlo simulation of the length of L3.

4. NDPA Simulation Results

Through the analysis in Section 3, this work designs a four-stage NDPA, the gate width of which is 1.88 mm. In order to trade-off chip size and gain, the actual design gate width is 1.46 mm. The final design total area is 1.6 × 2.5 mm^2. Figure 15 shows the final layout of the NDPA.

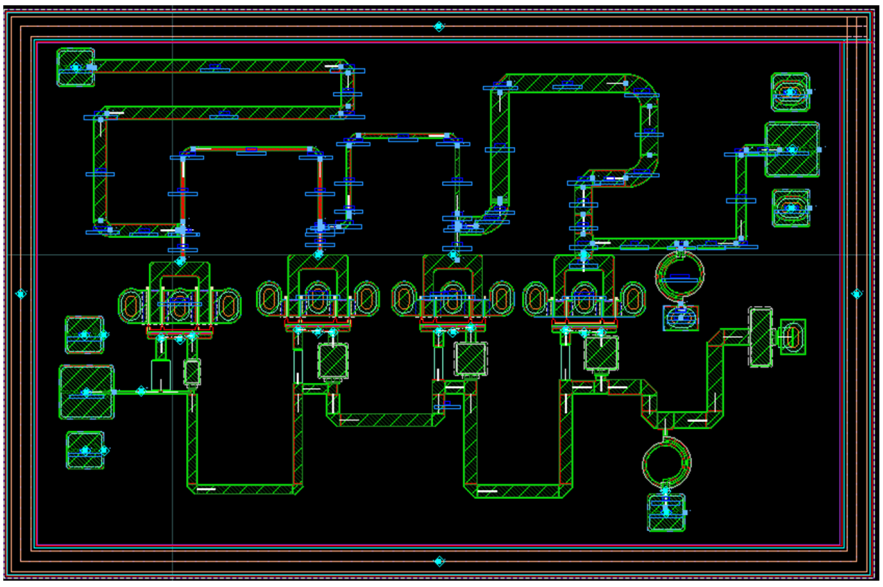


Figure 15. Schematic diagram of NDPA layout.

In the electromagnetic simulation, the gap from the ideal is fully considered and a harmonic simulation is carried out. Harmonic simulations were performed with a drain bias of 28 V and a drain current of 335 mA. The small-signal data diagram of the layout simulation is shown in Figure 16a. The electromagnetic simulation S-parameter results show a typical small-signal gain of 9.1 dB to 11.6 dB in the 2–16 GHz frequency range and output return losses of 5–15 dB. Figure 16b plots the large-signal characteristic output power and PAE of the electromagnetic simulation. In addition, the input power is stable at 25 dBm to measure the output power. In the frequency range of 2–16 GHz, the PAE is 16.6–27% and the output power is 35 dBm–37 dBm.

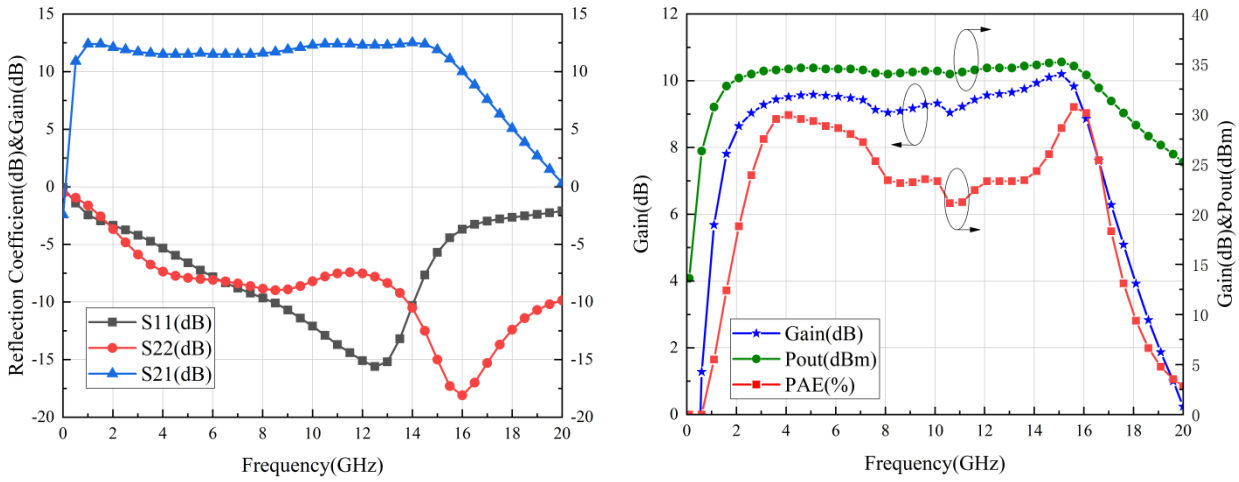


Figure 16. Electromagnetic simulation results: (**a**) Results for small signal, (**b**) Results for large signal.

Figure 17a shows the Monte Carlo analysis of the small-signal gain S21 of the amplifier. The ADS Monte Carlo simulation is used to sample 2000 points. The median S21 is 12.5 dB and the variance is 0.5216 at 12 GHz, so the design has a good robust effect. Figure 17b shows the group delay simulation curve of the NDPA. It can be seen that the group delay is about 75 ps in the working band. The maximum is about 123 ps and the minimum is about 48 ps, so this work has good delay characteristics.

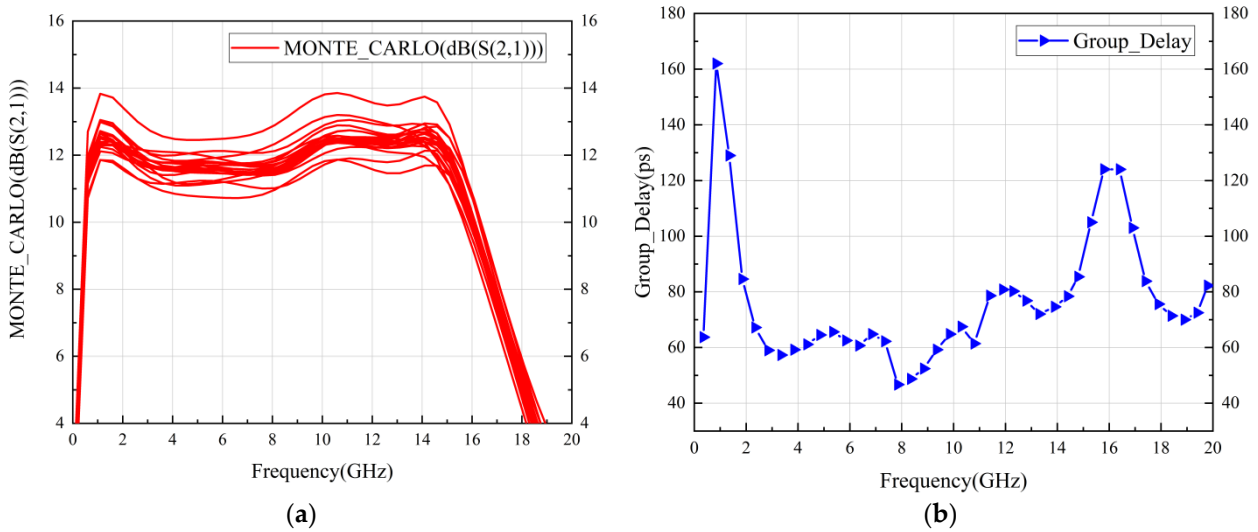


Figure 17. Layout simulation results: (**a**) Monte Carlo simulation results of S21, (**b**) Simulation results of distributed amplifier group delay.

Table 2 presents the performance of the NDPA compared with other published circuits at similar frequencies. The NDPA structure is widely used in the design of UWB PAs, but the problem is that it is difficult to achieve high efficiency over such a wide bandwidth. Of the reported circuits, only that reported here and those from [2,8] exhibit a wider bandwidth. In [29], a harmonic suppression method based on a distributed architecture was proposed. Compared to the results in [29], this work achieves a wider bandwidth. Compared to the listed references, this work achieves the minimum area.

Table 2. Performance comparison with other non-uniform distributed power amplifiers at similar frequencies.

Reference	Frequency (GHz)	Gate Length (GaN)	Stages #	Gain (dB)	Pout (dBm)	PAE (%)	Arae (mm^2)
[2]	4–16	0.15	1	8.7–14.6	37.8–40.2	11.8–33.9	7.8
[3]	6–18	0.25	1	8–12	38.3–41.6	13.6–33.8	8.5
[4]	1–8	0.15	2	30–32	39.7–41.2	29–46	11.4
[5]	2–8	0.25	1	10.1–13.3	38.7–40.1	27.2–35.8	12.18
[8]	2–20	0.15	2	15.8–17.5	33.8–35.4	18.4–36.5	7.5
[15]	2–15	0.25	1	9–10.4	36.35–38.4	20.6–32	10
[17]	2–12	0.25	1	9–14	37–39.3	5–35	4.3
[21]	6–18	0.25	2	15.3–23.3	40.3–43.9	15.5–26.6	10.7
[29]	2–6	0.45	1	8–10.8	42.3–44.6	19–15	12
This work	**2–16**	**0.25**	**1**	**9.1–11.6**	**35–37**	**16.6–27**	**4**

5. Conclusions

In this work, a simulation of NDPA with a 0.25 μm GaN HEMT process was proposed. By adjusting the impedance of the drain ATLs, it is finally matched to the load. The main factors affecting efficiency are analyzed, and the appropriate values are selected in the simulation. Over the frequency range of 2–16 GHz, the simulated results of this NDPA show a power added efficiency (PAE) of 16.6–27%, a saturated continuous wave (CW) output power of 35–37 dBm, a small-signal gain of 9.1–11.6 dB, and output return losses of 5–9 dB.

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