


Article

Growth and Fabrication of GaAs Thin-Film Solar Cells on a Si Substrate via Hetero Epitaxial Lift-Off

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Abstract: We demonstrate, for the first time, GaAs thin film solar cells epitaxially grown on a Si substrate using a metal wafer bonding and epitaxial lift-off process. A relatively thin 2.1 μm GaAs buffer layer was first grown on Si as a virtual substrate, and a threading dislocation density of $1.8 \times 10^7 \text{ cm}^{-2}$ was achieved via two $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ strained insertion layers and $6 \times$ thermal cycle annealing. An inverted p-on-n GaAs solar cell structure grown on the GaAs/Si virtual substrate showed homogenous photoluminescence peak intensities throughout the 2" wafer. We show a 10.6% efficient GaAs thin film solar cell without anti-reflection coatings and compare it to nominally identical upright structure solar cells grown on GaAs and Si. This work paves the way for large-scale and low-cost wafer-bonded III-V multi-junction solar cells.

Keywords: solar cell; flexible photovoltaics; wafer bonding; epitaxial lift-off; heteroepitaxial growth



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1. Introduction

III-V multijunction solar cells have been the most efficient photovoltaic cells by overcoming the detailed balance limit of single-junction solar cells [1–5]. Recently, six-junction III-V solar cells with three compositionally graded buffers have reached a 1-Sun global efficiency of 39.2% [2]. The monolithically integrated six-junction solar cell requires high material consumption and long epitaxial growth time for the three metamorphic graded buffers that are approximately $\sim 5 \mu\text{m}$ thick in total. Therefore, the high material growth time and cost can be an obstacle for the use of III-V multi-junction solar cells in various terrestrial applications, other than for space and military applications. Wafer-bonded III-V multi-junction solar cells are another type of high efficiency III-V technology [6–8]. Four-junction solar cells fabricated by bonding an InGaP/GaAs dual-junction solar cell to an InGaAsP/InGaAs cell showed a record-breaking conversion efficiency of 44.7% under 297-Suns [9]. Although this approach does not require lengthy and material-consuming growth of metamorphic graded buffers, it must consume two expensive III-V wafers, e.g., GaAs and InP wafers, to create one high efficiency multi-junction solar cell. Since the cost of III-V wafer accounts for more than 80% of the total manufacturing cost [10,11], replacing expensive III-V wafers with cheaper Si wafers could be the first step toward more techno-economic and high efficiency III-V multi-junction solar cells.

Growth of III-V materials on Si, however, creates several hurdles to overcome, such as large lattice mismatch, polar/non-polar growth, and thermal cracks [12–16]. The large lattice mismatch issue can be mitigated via dislocation filter layers, thermal cycle annealing, and two-step growth, while the polarity mismatch can be addressed by using an offcut Si wafer [17–22]. The thermal cracks caused by the difference in thermal expansion coefficients during sample quenching can be avoided by restricting the total III-V layer thickness below $\sim 7 \mu\text{m}$ at moderately low growth temperatures [23]. Decades of research on III-V growth on Si have enabled production of 18.0% efficient monolithic GaAs solar cells on Si by addressing these issues [24,25]. However, the possibility of epitaxial lift-off of III-V solar cells grown on Si for wafer-bonded III-V multi-junction solar cells to reduce their manufacturing cost has not been explored.

Here, we demonstrate, for the first time, a thin-film GaAs solar cell grown on an Si wafer then transferred to a polyimide film via a metal wafer bonding and epitaxial lift-off process. The $2.1 \mu\text{m}$ -thick GaAs buffer was grown on a Si wafer to reduce the threading dislocation density to $1.8 \times 10^7 \text{ cm}^{-2}$, measured by electron channeling contrast imaging. An inverted GaAs solar cell structure was grown on the GaAs/Si template and revealed a 10.6% 1-Sun efficiency without anti-reflection coating, demonstrating that a wafer bonding and epitaxial lift-off process is compatible with III-V solar cells hetero-epitaxially grown on Si substrates. We believe that an optimized GaAs solar cell structure with InGaP window layer and back-surface field layer will boost the thin film GaAs solar cell performance further.

2. Material Growth

All samples were grown by a Veeco Gen-930 molecular beam epitaxy (MBE) system. Si substrates, with 4-degree offcut towards [110] plane, were used to prevent formation of anti-phase domains. A high-quality GaAs buffer was grown on an Si substrate after desorbing the native oxide at 900°C for 10 min under As_2 overpressure. After oxide desorption, the substrate was cooled to 400°C for a 100 nm low-temperature GaAs (LT-GaAs) buffer, followed by 400 nm high-temperature GaAs (HT-GaAs) buffer growth at 580°C . Then, $3\times$ thermal cycle annealing (TCA) was performed at $350\sim 650^\circ\text{C}$ to increase the dislocation glide velocity and decrease threading dislocation density (TDD). Afterwards, the substrate temperature was raised to 500°C for the growth of a 200 nm $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ single insertion layer (SIL). Subsequently, the 600 nm HT-GaAs was grown at $1 \mu\text{m/hr}$, followed by $3\times$ TCA, 200 nm $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ SIL, and 600 nm HT-GaAs layer. After the growth of high-quality GaAs buffer, as shown in Figure 1a, electron channeling contrast imaging (ECCI) was performed by Inspect F50 (FEI) to investigate the TDD. The sample was loaded back to the MBE reactor for the growth of GaAs solar cells, as shown in Figure 2a. Cells consisted of inverted GaAs emitter/base structures with $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ window/BSF layers. For the epitaxial lift-off (ELO) process, a 50 nm AlAs sacrificial layer was inserted between the p-GaAs contact layer and the 100 nm GaAs buffer.

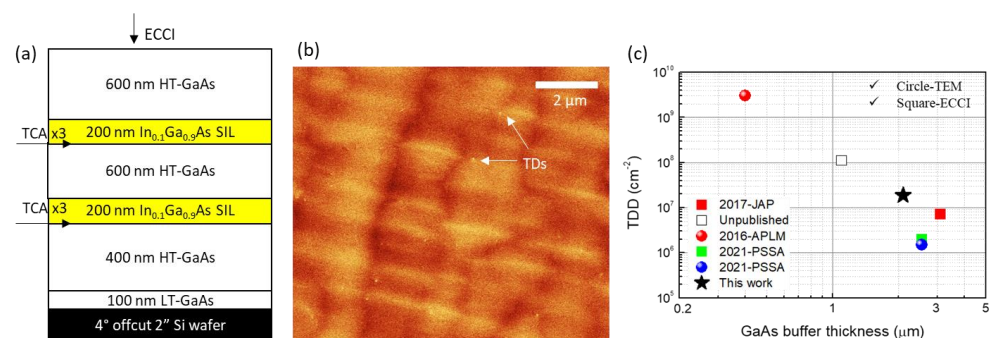


Figure 1. (a) GaAs buffer structure on 4-degree offcut Si using $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ single insertion layer and thermal cycle annealing. (b) An ECCI image of the GaAs buffer surface grown on Si substrate. (c) Threading dislocation density benchmark of GaAs/Si materials reported by other groups.

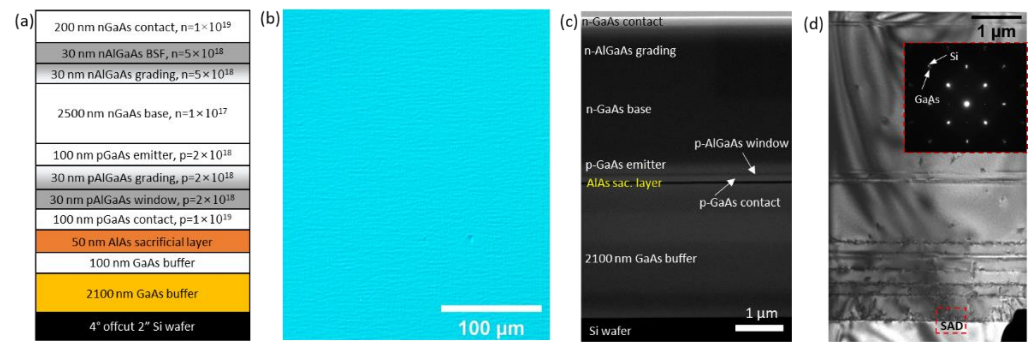


Figure 2. (a) Schematic illustration of GaAs one-junction solar cell grown on Si substrate. (b) Differential interference contrast optical microscopy image. (c) Cross-sectional SEM image of the entire solar cell structure. (d) Cross-sectional bright-field TEM image. Inset shows the selected area diffraction pattern.

3. Results and Discussion

3.1. Material Characterizations

The total GaAs buffer thickness was maintained at 2.1 μm to avoid thermal cracks in the full device sample because a typical GaAs solar cell adds approximately another 3 μm-thick III-V layers on top of the buffer. Reducing the GaAs buffer thickness typically results in higher TDDs [26]. Therefore, it was important to modify the GaAs buffer structure so that the 2.1 μm-thick GaAs/Si template used in this work could still serve as a virtual substrate with a low TDD. ECCI was performed to investigate the TDD. Figure 1b shows a representative ECCI image where white speckles are individual threading dislocations (TDs) propagating to the surface. The TDDs were calculated by taking more than five images per sample for high statistical accuracy. We achieved a TDD of $1.86 \times 10^7 \text{ cm}^{-2}$ from the 2.1 μm GaAs buffer layer. Figure 1c shows a comparison of TDD in GaAs/Si material system reported by other groups.

Figure 2a shows the schematic structure of one-junction GaAs solar cell grown on Si substrate with optimized TCA and $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ SIL. The p-on-n GaAs solar cell has an upside-down structure for metal wafer bonding and ELO process. Figure 2b shows a Nomarski image of the surface with few oval defects and hillocks, which are extremely detrimental to solar cell performance by increasing electrical shunts. The cross-sectional SEM image of Figure 2c reveals the entire GaAs solar cell structure grown on the Si substrate. We also confirmed that the growth of the 50 nm AlAs sacrificial layer for the ELO process did not roughen the layer interface, as seen in the reflection high energy electron diffraction patterns (not shown here). The interfaces in GaAs/Si system were investigated by two-beam condition TEM (Tecnai, FEI) measurement for more clarity to measure the defects. The TEM sample was prepared with Helios G4 HX dual beam (FEI) to make the cross-sections from the actual GaAs buffer on Si. Figure 2d shows a cross-sectional bright field TEM image of the TDs propagating into the GaAs solar cell layer, which were generated at the interface between the GaAs buffer layer and the Si substrate. The compressive strain state of the GaAs buffer was fully relaxed by forming misfit dislocations, as observed in the selected area diffraction image (inset of Figure 2d).

We performed a large area micro-PL on the fully grown sample at room-temperature, as shown in Figure 3a, using a 532 nm green laser as a pump source. The wafer was specular and had no cracks induced by thermal expansion mismatch. Figure 3b shows a $1.5 \times 1.5 \text{ cm}^2$ PL peak intensity mapping measured from the GaAs layer ($\lambda = \sim 840 \text{ nm}$), confirming absence of thermal cracks in the fully grown sample. Furthermore, the PL peak intensity varied within a relatively small range from ~ 3800 to 4200 , except for a small spot on the right corner. Raman spectroscopy (In Via Raman Microscope, Renishaw) was also carried out to investigate the strain state of the III-V layer, especially the residual thermal tension (Figure 3c). Five different locations were probed, as shown in Figure 3a, and were compared with the GaAs solar cell sample grown on a GaAs substrate as a reference.

Transverse optical phonon peaks at 268 cm^{-1} and longitudinal optical phonon 290 cm^{-1} peaks were clearly detected from both [27]. The slight red-shifts from the Si substrate sample compared to the GaAs sample were attributed to the small residual thermal tension in the GaAs epitaxial layer on Si [28]. The excellent homogeneity of material optical property is especially promising for large-scale manufacturing of wafer-bonded multi junction solar cells.

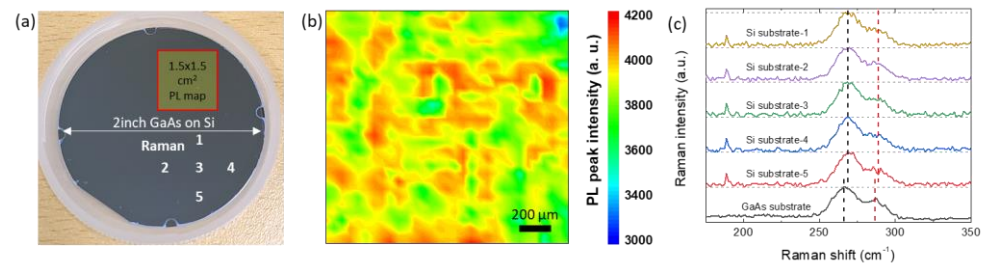


Figure 3. (a) Photograph of a 2-inch GaAs one-junction solar cell grown on Si substrate. The red-line square shows the selected area for micro-PL mapping. (b) Micro-PL mapping image on the selected area in (a). (c) Raman spectra of GaAs solar cell grown on GaAs and Si substrate.

3.2. Device Fabrication and Performance

Figure 4a shows the fabrication procedure of our solar cells. We first deposited Pt/Au (10/50 nm), which served as a bonding material and ohmic contact metal, on the GaAs solar cell sample and the transfer substrate by electron beam evaporation. Then, standard photolithography was performed to define mesas. The samples were etched using a 1:1:5 mixture of phosphoric acid, hydrogen peroxide, and deionized water for a fast ELO. Subsequently, Ar plasma was irradiated for surface activation, which leaves highly reactive radical site layers that substantially enhance surface adhesion. Metal wafer bonding was conducted with a uniaxial pressure of approximately 40 kgf/cm^2 . After the bonding process, the GaAs epitaxial layer was separated from the Si donor substrate by an ELO process in which the AlAs sacrificial layer was etched by immersion in HF-based solution [29–31]. Finally, Pt/Ti/Pt/Au (20/30/20/200 nm) was deposited on the top contact layers by electron beam evaporation. No anti-reflection coating (ARC) was applied on the cells. Figure 4b shows photographs of the GaAs solar cells transferred to a Pt/Au-coated polyimide film. The inset shows an optical microscope image of the transferred mesa epilayer.

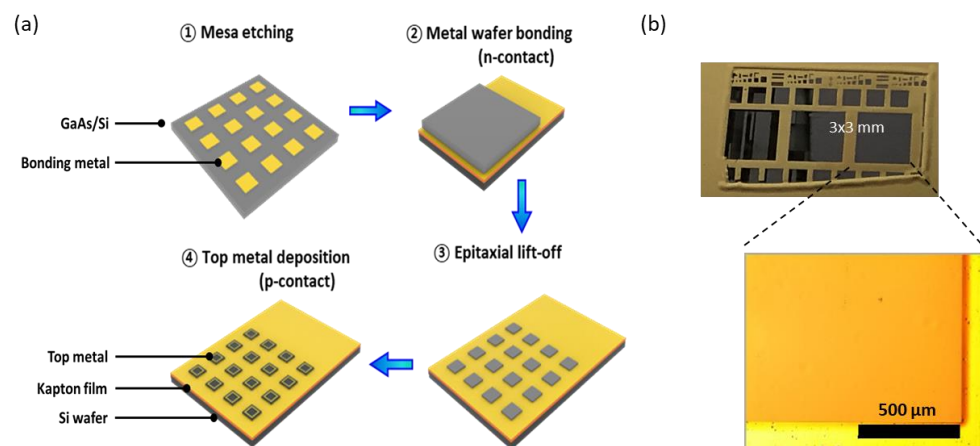


Figure 4. (a) Fabrication procedure for transfer process of GaAs solar cell. (b) Photograph of transferred GaAs solar cell to polyimide. The inset shows the optical microscope image of GaAs solar cell grown on Si substrate.

Figure 5a shows the sample structures of three different GaAs solar cells: inverted p-on-n GaAs cell grown on Si with AlAs sacrificial layer, upright solar cell, and GaAs solar cell grown on GaAs. The current density (J)-voltage (V) characteristics were investigated to compare the electrical properties of the GaAs solar cells. Figure 5b shows dark J-V curves of the GaAs solar cells and all samples showed good rectifying characteristics with low dark current densities. The comparable dark current densities of 1.26 and 2.08 $\mu\text{A}/\text{cm}^2$ between Sample A and B indicated that our ELO process did not degrade the material quality. The inset shows the ideality factor of the GaAs solar cell, which was derived from J-V curves of samples. The ideality factor provides insight on the current flow mechanism; its value is close to 2 when the carrier transport through the p-n junction is dominated by the generation-recombination mechanism. The obtained ideality factor of Sample C grown on a GaAs substrate showed its value to be under 2 at low forward bias voltages, which suggests that the diffusion current was superior over junction recombination current at low forward bias. On the other hand, the ideality factor of Sample A and B showed values above 2 at small forward biases, indicating that the defect-induced recombination and tunneling current was the dominant origin of dark current. Figure 5c shows the J-V characteristics of our fabricated GaAs solar cell in-house under AM1.5G solar spectrum. First, it is of note that our baseline upright GaAs solar cell (Sample C) showed a conversion efficiency of 11.2%. Comparison of the upright GaAs cells grown on GaAs and Si substrate indicated that the presence of $1.8 \times 10^7 \text{ cm}^{-2}$ TDs lowered the open-circuit voltage by 0.13 V and the fill-factor by 7.6%. In addition, Sample B showed a rather lower slope, which was attributed to higher series resistance. The hetero-epitaxial lift-off process seemed to additionally decrease the open-circuit voltage slightly, from 0.79 V to 0.72 V, but it did not affect the fill-factor. Even at low open-circuit voltage, Sample A showed a comparable conversion efficiency of 10.6%, which was slightly smaller than that of the upright cell on GaAs. Moreover, the short-circuit current was increased from 12.1 mA/cm^2 to 19.3 mA/cm^2 , probably due to the light-trapping effect and slight anti-reflection effect of the lift-off etching surface [13,30,31].

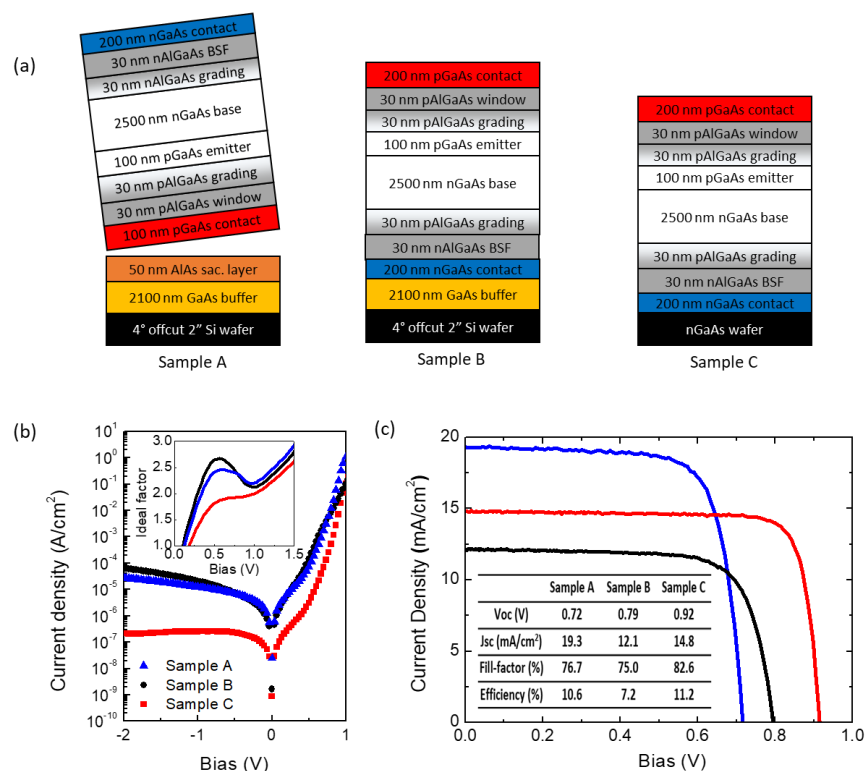


Figure 5. (a) Schematic diagrams of the one-junction GaAs solar cells. (b) Dark current density (J) –voltage (V) characteristics of GaAs solar cell. Inset shows the ideality factor as a function of bias voltage. (c) J–V curves for fabricated GaAs solar cells.

4. Conclusions

In this work, we demonstrate GaAs thin film solar cells grown on a Si substrate and then transferred to polyimide substrate using hetero-epitaxial lift off. The large mismatch of thermal expansion coefficients between GaAs and Si can generate thermal cracks, but a high quality 2.1 μm -thick GaAs buffer with thermal cycle annealing and $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ single insertion layer enabled a thermal crack-free and low threading dislocation density of $1.8 \times 10^7 \text{ cm}^{-2}$. Furthermore, the excellent homogeneity of the material optical property, confirmed by micro-PL and Raman spectroscopy, is especially promising for the large-scale manufacture of wafer-bonded III-V multi-junction solar cells. An inverted GaAs solar cell structure was grown on the GaAs/Si template and revealed a 10.6% 1-Sun efficiency without anti-reflection coatings, demonstrating that a wafer bonding and epitaxial lift-off process may be compatible with III-V solar cells hetero-epitaxially grown on Si substrates. We believe that an optimized GaAs solar cell structure with InGaP window layer and back-surface field layer will boost the efficiency of thin film GaAs solar cells grown on silicon.

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