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Leakage Current Mitigation of Photovoltaic System Using Optimized Predictive Control for Improved Efficiency

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Abstract: This paper proposes an optimized predictive control strategy to mitigate the potential leakage current of grid-tied photovoltaic (PV) systems to improve the lifespans of PV modules. In this work, the PV system is controlled with an optimized predictive control algorithm that selects the switching voltage vectors intelligently to reduce the number of computational burdens. Thus, it improves the dynamic performance of the overall system. This is achieved through a specific cost function that minimizes the change in common-mode voltage generated by the parasitic capacitance of PV modules. The proposed controller does not require any additional modulation schemes. Normalization techniques and weighting factors are incorporated to obtain improved results. The steady state and dynamic performance of the proposed control scheme is validated in this work through simulations and a 600 W experimental laboratory prototype.

Keywords: predictive control; leakage current; PV; optimization; MLI

Citation: Routray, A.; Hur, S.-H. Leakage Current Mitigation of Photovoltaic System Using Optimized Predictive Control for Improved Efficiency. *Appl. Sci.* **2022**, *12*, 643. https://doi.org/10.3390/app12020643

Academic Editors: Jang-Ho Lee and Hwachang Song

Received: 9 December 2021
Accepted: 6 January 2022
Published: 10 January 2022

1. Introduction

Increased consciousness about the significance of human activities has led to increased awareness of renewable energy sources in the 21st century. Solar energy has drawn incredible interest as a possible substitute for conventional energy sources because of its intrinsic advantages, such as its clean nature, lack of moving parts, and sustainability [1–3]. Photovoltaic cells convert solar radiation into electrical energy through the photovoltaic effect. The first-generation photovoltaic cell materials are based on monocrystalline, polycrystalline, and gallium arsenide (GaAs) technologies. The second generation includes amorphous silicon and thin microcrystalline silicon films, cadmium sulfide or telluride, and copper indium gallium selenide based solar cells. The third and fourth generations incorporate nanocrystalline films and stacked multilayers of inorganics based on III–V materials, such as GaAs/GaInP, organic-based (polymer) nanomaterials (e.g., carbon nanotubes), graphene, and their derivatives [4].

The monocrystalline Si cells are manufactured using the Czochralski process [5]. In this process Si ingots are grown from small monocrystalline silicon seeds and cut to yield Si wafers. This produces Si crystals with diameters ranging from 10 to 300 mm and lengths from 50 cm to 2 m. Polycrystalline Si is obtained using the Siemens process [6]. This process consists of gasification of metallurgical grade Si, distillation, and finally deposition to yield ultrapure silicon. The production of GaAs can be condensed into four stages: growth of ingots, wafer processing, epitaxy, and the manufacturing of devices [7]. The traditional production of second-generation photovoltaic cells follows the roll-to-roll process [8]. First, a cylindrical sheet is unfurled (as superficial deposition) and the sheet is washed and printed with an insulating layer. Si is subsequently deposited on the reflector, and the transparent conductive oxide is put on the silicon layer. The third generation (dye-sensitized solar cell) consists of low-cost solar cells in the form of thin films [9]. They are based on the formation of a semiconductor between a photo-sensitized anode and an electrolyte. Fourth-generation photovoltaic cells, such as organic photovoltaic cells, exploit conductive

organic polymers or small organic molecules for light absorption. Perovskite solar cells are comprised of a light-harvesting active layer and a designed perovskite compound (hybrid organic-inorganic lead or tin halide). It is placed between the electron-transport (mesoporous material or TiO_2) and hole-transport layers [10,11].

The grid-tied photovoltaic (PV) converters need to be designed for high efficiency, small size, and low cost and weight [12]. These converters use line-frequency transformers to provide galvanic isolation, which makes the overall system bulky. However, few PV converters use high-frequency converters for galvanic isolation [12]. The high-frequency isolation transformers are smaller than line-frequency transformers, but high-frequency transformer-based power converters have many power stages, which increase the system's complexity and reduce the system's efficiency. Currently, the transformerless PV converters are extensively used in low-power distributed PV generation by imposing DIN VDE 0126-1-1 standards [13]. Due to the removal of transformers, the leakage current appears in the system because of changes in common-mode voltage (CMV) across the parasitic capacitance, which appears between the PV module and the ground [12]. Moreover, the leakage current leads to safety issues in the system, power losses, harmonic distortion in grid current, and electromagnetic interference issues. Therefore, they must be limited within a utilitarian boundary [13].

Solar modules are typically connected to PV converters, which convert variable DC output to AC (line frequency) for commercial grid applications. Several power converters reported in literature, such as two- and three-level inverters, H5, H6, and HERIC, have found commercial and academic research acceptance [14–16]. Traditional inverters are unable to provide high efficiency at higher power ratings; therefore, converter topologies are moving toward multilevel structures. Among the various multilevel inverters, cascaded H-bridge multilevel inverters (CHB-MLI) have several advantages as compared to other converters [17–21]. The use of CHB inverters also opens up the prospect for removal of transformers from PV systems. MLIs are more attractive because of their lower device stress and low dv/dt. A CHB made up of n full bridges ($4n$ power switches) can synthesize $2n + 1$ voltage levels when the supply voltage is the same for each full bridge. Reduction in switches per output voltage levels can be achieved in CHB structures easily, if different supply voltages are selected for each full H-bridge [20]. Due to the higher number of DC voltage sources used in CHB-MLIs, their application is restricted for higher voltage levels. In due course, asymmetrical CHBs will evolve, until DC voltage sources can be replaced by capacitors. The topology used in this paper consists of two asymmetrical H-bridges and is known as hybrid MLI (HMLI) for generating nine output voltage levels. The DC voltage source (in place of a PV panel) supplies one of the full H-bridges, whereas a capacitor supplies the other one. By appropriately controlling the ratio between the two voltages, different output levels can be generated. This facilitates the elimination of bulky transformers, which makes the overall system lighter and more efficient. However, the removal of the transformer gives rise to leakage current. Due to the change in CMV, leakage current flows though the PV panel, which depreciates the lifespans of the PV modules.

Leakage current can be mitigated using several methods, such as by changing converter topology, including filters [22], changing modulation schemes [23,24], and altering control schemes [25,26]. Few methods are employed for changing converter topology (e.g., the conventional H-bridge is modified by adding more switches to form the familiar H5 and H6 converters). The leakage current can be reduced by including an extra filter, as reported in Lai, R. et al. [22]. The switched CMV can be kept constant by using a precise modulation scheme. Modification in the modulation schemes of conventional converters is one of the solutions for reducing leakage current. Multicarrier pulse width modulation (MC-PWM) and space vector modulation (SVM) are two well-known modulation techniques used in MLIs [24,25]. The SVM technique is more productive due to better switching control. However, it requires regress efforts for implementation. In Kang, D.W. et al. [24], SVM is used to reduce the leakage current in transformerless PV inverter topology. How-

ever, switching state selection is not easy in terms of practical implementation. MC-PWM also increases the computational burden because of a higher number of carrier signals.

Among the reported control schemes, model predictive control (MPC) is one of the better control schemes because of its robust dynamic and static characteristics. In this work, an optimized finite control set (FCS) MPC is utilized for overall control and for reducing leakage current from PV panels [27–32]. This paper uses a transformerless HMLI PV system that synthesizes different multilevel output voltage levels. Capacitor voltage balancing and the elimination of leakage current is achieved through a modified FCS-MPC scheme. The number of computational burdens is minimized to attain optimum results by adjusting the selection of switching vectors. The control algorithm is also optimized for compilation in any microcontroller. Normalization and weighted techniques are also implemented to obtain improved results [32].

The proposed control structure and converter architecture are discussed in Section 2. The different voltage levels obtained from HMLI and their impacts on leakage current are also discussed, as are the salient features for the modelling of optimized FCS-MPC, which are particularly useful for PV systems. The modified control scheme also implements current control and capacitor voltage balancing, as discussed in Section 2. The optimization is explained with mathematical concepts. The simulation and experimental results are discussed in Sections 3 and 4, respectively, and conclusions are drawn in Section 5.

2. Modified Topology and Control Scheme

The conventional multilevel cascaded H-Bridge (CHB-MLI) uses an isolated DC source for every H-bridge. The number of voltage levels generated can be generalized to $(2k + 1)$, where k is the number of H-bridges. An inverter with two H-bridges uses two DC sources of equal magnitude for a five-level output voltage generation. However, it requires more DC sources for each H-bridge to generate higher voltage levels, which increases the cost of the system. A capacitor can be used instead of a DC voltage source. Furthermore, the same configuration with one DC source and one capacitor at their respective H-bridges can generate five, seven, or nine voltage levels, respectively. A trade-off has to be made as increasing the voltage levels decreases the magnitude of the maximum voltage generated. The use of a capacitor raises the issue of charging and discharging so that the capacitor voltage can be balanced at the desired value. The balancing of the capacitor can be attained by cascading another control loop in addition to a grid current control loop using conventional PI-based control schemes [15–17]. However, these control loops make the overall system complex. This issue of intricacy is further augmented when additional control schemes are introduced to reduce the leakage current in grid-tied PV converters. This can be smoothly achieved with the proposed proper control scheme.

The modified topology, a hybrid-MLI (HMLI), effectively solves the control challenges created by the incorporation of a capacitor in one of the H-bridges. The modified model predictive control (MPC) implemented in this work uses multivariate, multi-input, and multi-output optimisation problems. The proposed modified circuit is depicted in Figure 1. A block diagram for the overall control scheme is shown in Figure 2. The control loop takes the capacitor voltage (V_{cap}), grid voltage (V_{g}), current (I_{g}), reference current (I_{ref}), grid angle (θ), and weighting factor. The grid angle is generated through a phase-locked loop (PLL). All these control loops use modified MPC to generate the required switching signals fed to the HMLI.

The multilevel output generation property of the MLI is fully used in the proposed modified HMLI. The voltage across capacitors is maintained at a third of the input voltage (V_{DC}), which results in the maximum of different voltage levels possible obtained across two H-bridges (i.e., nine). The 16 combinations of voltage vectors are given in Table 1 to generate these nine levels. However, only nine separate vectors are required out of only 16 voltage vectors to generate the required voltage level. The modified MPC only considers these nine states, thus reducing the computation time significantly. The number of distributed states is also further minimized using optimization, which will be discussed

later in this paper. In addition, two extra switches, S_5 and S_6, are incorporated to minimize the leakage current problem, as shown in Figure 1.

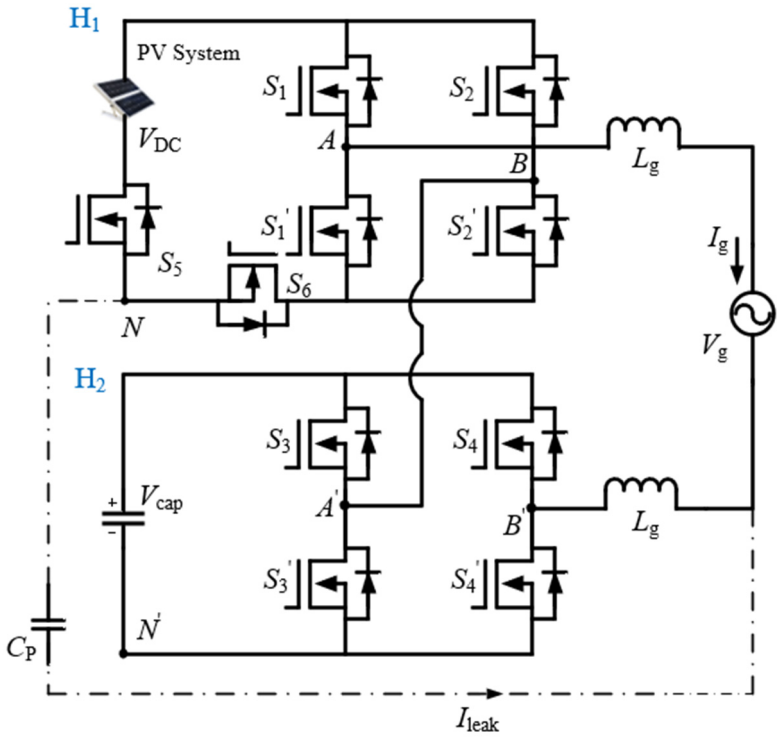


Figure 1. Transformer less nine-level PV-supported HMLI.

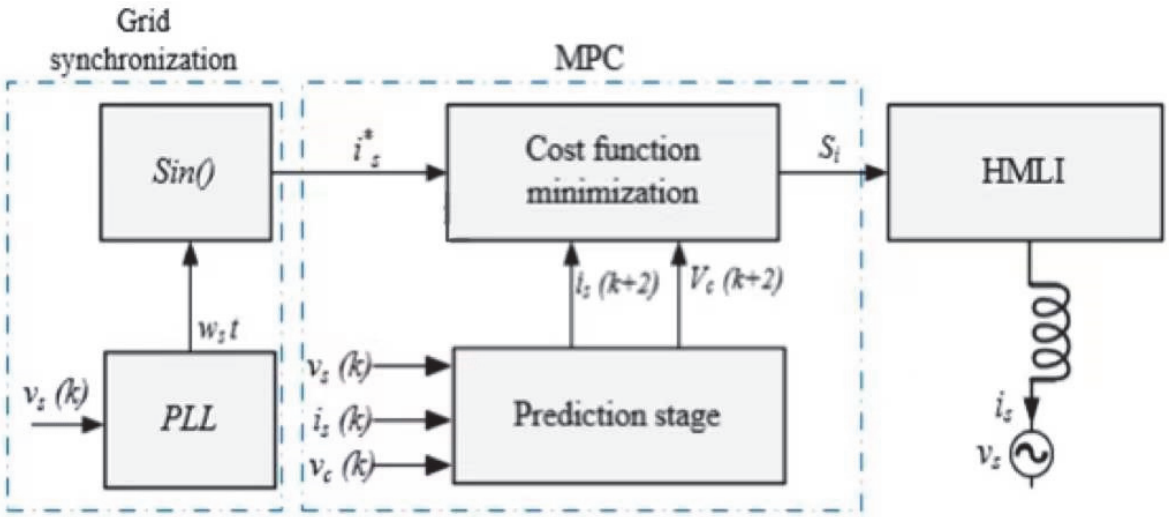


Figure 2. Schematic of the overall system.

Table 1. Generated nine voltage levels.

S_1	S_2	S_3	S_4	V_0
0	0	0	0	0
0	0	0	1	−0.33 V_{DC}
0	0	1	0	0.33 V_{DC}
0	0	1	1	0
0	1	0	0	$-V_{DC}$
0	1	0	1	−1.33 V_{DC}
0	1	1	0	−0.66 V_{DC}
0	1	1	1	$-V_{DC}$
1	0	0	0	V_{DC}
1	0	0	1	0.66 V_{DC}
1	0	1	0	1.33 V_{DC}
1	0	1	1	V_{DC}
1	1	0	0	0
1	1	0	1	−0.33 V_{DC}
1	1	1	0	0.33 V_{DC}
1	1	1	1	0

The parasitic capacitance is formed between the PV module and the ground. The leakage current is generated by a change in the CMV across it. The CMV is the average value of voltage between the output and the reference point. The negative terminal of the DC voltage, (i.e., terminal N) is called the common reference point for the upper H-bridge. Similarly, for the lower H-bridge inverter, N' is the common reference point. The parasitic capacitance is formed for the upper H-bridge. The CMV and leakage current in the two H-bridges are also the same. The CMV voltage (V_{CM}) for the upper full-bridge can be expressed in (1):

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{1}$$

where V_{AN} and V_{BN} are voltages between the mid-point of the upper H-bridge legs to the negative terminal of the DC link. V_{AB} is the voltage between the mid points of the two legs of the upper H-bridge inverter. V_{inv} is the output voltage across the load. The leakage current primarily depends upon the magnitude of the CMV. The CMV can be derived in (2) and (3) as follows:

$$V_{CM} + V_{AN} - V_{Lg} - V_{inv} = 0 \tag{2}$$

$$V_{CM} + V_{BN} - V_{Lg} - V_{A'B'} = 0 \tag{3}$$

V_{inv} has much less effect on parasitic capacitance. Hence, it can be neglected. The filter inductance, L_g, and the voltage drop caused by L_g are considered the same for the two H-bridges for ease of analysis. The mathematical expression of the CMV can be obtained by adding Equations (2) and (3) as follows:

$$2V_{CM} + V_{BN} + V_{AN} - V_{A'B'} = 0 \tag{4}$$

From Equation (4), the CMV can be written as:

$$V_{CM} = \frac{V_{A'B'} - V_{AN} - V_{BN}}{2} \tag{5}$$

Equation (5) is utilized for defining the CMV in several intervals of referenced time.

3. Modelling and Optimization

In this section, the mathematical modelling of current tracking, capacitor voltage balancing, and leakage current mitigation in HMLI is derived.

3.1. Current Tracking

The nine (highlighted) valid switching states of the HMLI defined in Table 1 are used for tracking load current. For grid-tied HMLI with inductive (*R-L*) loads, the analytical expression can be written as in (6):

$$V_{\text{inv}} - R_g I_g - L_g \frac{dI_g}{dt} - V_g = 0 \tag{6}$$

where V_{inv} is output voltage, R_g is grid filter resistance, and L_g is filter inductance.

To predict the current for the next sampling instant, Equation (6) needs to be converted into discrete time. The variation of I_g at two sampling instances, k and $k + 1$, are alienated by a sampling time of T_S. This can be expressed in (7) as follows:

$$\frac{dI_g}{dt} = \frac{I_{g,k+1} - I_{g,k}}{T_S} \tag{7}$$

To derive an expression for current prediction, the relation between V_{inv} and the grid current I_g needs to be expressed in discrete time. The future value of the current can be predicted by using a first-order Taylor series [24]. Considering h as the prediction horizon, the grid current can be written as in (8):

$$I_g(k+h) = \left(1 - \frac{R_g \times T_s}{L_g}\right) \times I_g(k+h-1) + \frac{T_s}{L_g}\left(V_{\text{inv}}(k+h-1) - V_g(k+h-1)\right) \tag{8}$$

As there is more than one term each for different purposes, weighting components will be assigned with each term. However, for the $V_{\text{inv,min}}$ calculation, only the term that regulates current is considered. The cost function (CF) is an essential factor in MPC. Here CF is defined as G_1, G_2, and so on for different parameters. G_1 is taken as a CF for current tracking and grid synchronisation as given in Equation (9). Weighting factors (W_1, W_2, etc.) are assigned to each term of CF, which regulates the robustness of the control parameter. The CF (G_1) for current tracking can be expressed as:

$$G_1 = W_1\left(I_g^* - I_{g,k+1}\right)^2 \tag{9}$$

where I_g^* is the reference amplitude of the grid current.

Substituting Equation (8) in (9),

$$G_1 = \left(I_g^*(k+1) - \left(1 - \frac{R_g \times T_s}{L_g}\right) \times I_g(k) - \frac{T_s}{L_g}\left[V_{\text{inv}}(k) - V_g(k)\right]\right)^2 \tag{10}$$

The conventional MPC iterates over all of the voltage vectors. However, in this work, the voltage vectors are reduced to nine for each voltage level. The voltage vectors are further reduced to three by implementing the optimization discussed below. The optimum voltage can be obtained by differentiating G_1 by V_{inv} to zero, given in (11) as follows:

$$\frac{dG_1}{dV_{\text{inv}}} = 0 \tag{11}$$

The derivative of G_1 w.r.t V_{inv} can be written as in (12):

$$\frac{dG_1}{dV_{\text{inv}}} = \frac{-2T_s}{L_g}\left[I_g^*(k+1) - \left(1 - \frac{R_g \times T_s}{L_g}\right) \times I_g(k) - \frac{T_s}{L_g}\left[V_{\text{inv}}(k) - V_g(k)\right]\right) \tag{12}$$

By solving Equation (12),

$$V_{\text{inv, min}} = \frac{-L_g}{T_s} A \tag{13}$$

$$\text{where } A = \left(1 - \frac{R_g \times T_s}{L_g}\right) \times I_g(k) + \frac{T_s}{L_g}\left(V_g(k) - I_g^*(k+1)\right) \tag{14}$$

The minimum voltage can be written in (15) as follows:

$$V_{\text{inv,min}} = -\frac{L}{T_S}\left(\left(1 - \frac{R \cdot T_S}{L}\right).I_{g,k} - I_{ref}\right) + V_g \tag{15}$$

As the slope of Equation (15) is negative, it ascertains that minimum voltage is generated. V_{inv} is bound to $V_{(\text{p-p})}$. It needs to be cut to allow the choice of the correct voltage vectors. Out of the chosen voltage vectors, a maximum of three are hard-coded. When V_{min} is within the constrained voltage range, the modified MCP loop iterates through only three vectors to predict the vector that will provide the minimum-cost value. A detailed explanation is shown in Figure 3. The program iterates follow CF minimisation. These modifications lessen the running time per multiple iteration. The computational time is reduced because of the modifications, as outlined in Table 2.

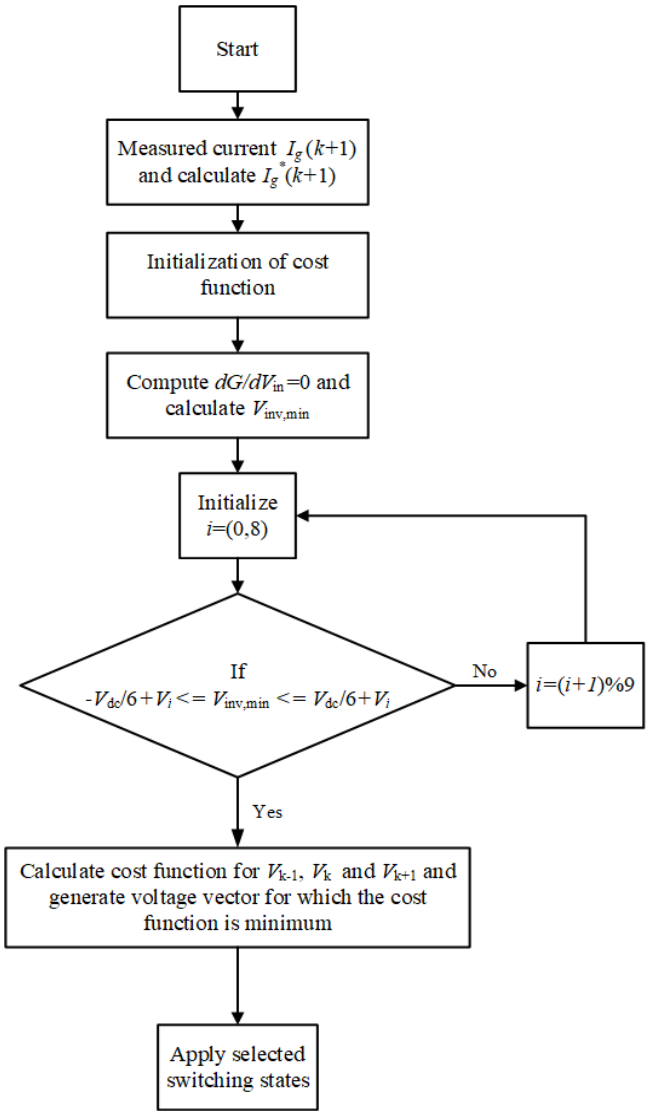


Figure 3. Flowchart of modified MPC optimized algorithm.

Table 2. Effect of modification in MPC control scheme.

Without Voltage Vector Selection	With Voltage Vector Selection
1.0435×10^{-5}	3.3102×10^{-6}
1.0557×10^{-5}	3.1408×10^{-6}
1.0732×10^{-5}	3.2107×10^{-6}
1.0615×10^{-5}	3.1326×10^{-6}
2.0162×10^{-5}	3.6402×10^{-6}
Average time (s) $= 1.0775 \times 10^{-5}$	Average time (s) $= 3.2435 \times 10^{-6}$

3.2. Capacitor Voltage Balancing

For capacitor voltage balance, the capacitor voltage is compared to the desired reference voltage. The charging and discharging occurs because of the switching action of S_3 and S_4, as depicted in Figure 4. Charging occurs when switches S_4 and $S_{3'}$ are turned on and charging occurs when S_3 and $S_{4'}$ are turned on, as shown in Figure 4a,b, respectively. It also depends on the current flowing through the capacitor and is taken to realise a mathematical model of capacitor voltage balance. The voltage of the capacitor (working as source in the H_2 bridge) is repesented by adding it as one more term to the CF. To predict capacitor voltage (V_c) for the next sampling instant, the relation between current and voltage variation can be written in Equations (16) and (17) as follows:

$$\int \frac{i(S_4 - S_3)}{C} dt = \int dV_c \tag{16}$$

$$\frac{i(S_4 - S_3)}{C} T_S = V_{k+1} - V_k \tag{17}$$

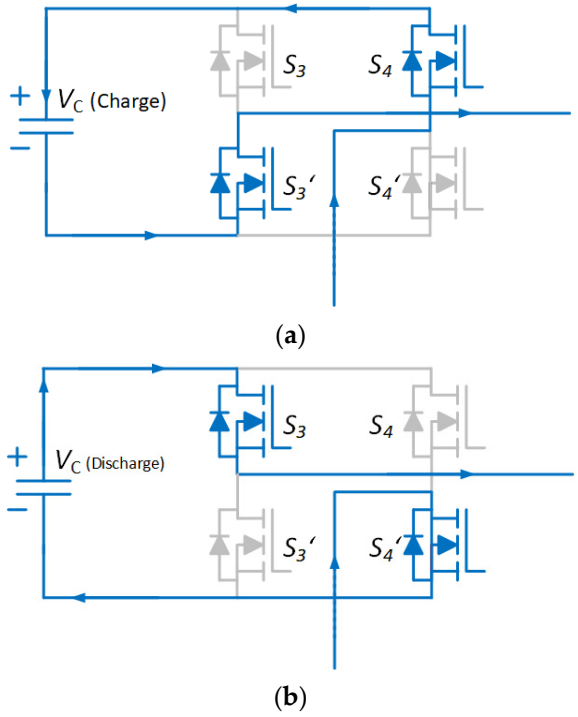


Figure 4. Capacitor voltage balancing: (**a**) charging intervals, and (**b**) discharging intervals.

V_{k+1} and V_k are the capacitor voltages at time instants $(k + 1)T_S$ and kT_S, respectively.

By rearranging the predicted capacitor voltage, $V_c(k+1)$ can be written in (18) as:

$$V_c(k+1) = V_c(k) + [(S_3 - S_4) \times (\frac{i \cdot T_S}{C})] \quad (18)$$

The predicted capacitor is compared with the reference value of the capacitor (33% of the DC voltage source) by adding the modelled term in the CF (G_2) in (19) as follows:

$$G_2 = W_2 . \left(0.33 \times V_{DC} - \left(V_k - \frac{i(S_3 - S_4)}{C}\right)\right)^2 \quad (19)$$

An additional term in Equation (19) needs the switching vectors responsible for the charging and discharging of the capacitor. The adjacent voltage selection reduces the maximum iteration to only three vectors.

3.3. Leakage Current Minimization

To reduce the leakage current, two switches, S_5 and S_6, are included in the circuit. When there is commutation from ON to OFF, the voltage across the parasitic capacitor changes from V_{DC} to 0 and vice versa. This sudden change in voltage results in leakage current. S_5 and S_6 are additional switches and are turned ON for most of the duration of a cycle. When the state of a switch changes from 0 to 1, the adjacent switch (S_5) has same state, and is triggered to turn off to include resistance (R_1) in the leakage current path for reducing the rate of the charging and discharging of the parasitic capacitor. Hence, the leakage current is reduced. Similary, the resistance (R_2) is included when S_6 is triggered to turn off. The flows of leakage current are depicted in Figure 5a,b, respectively. At the instant when a DC source commutates from being disconnected to connected or vice versa, the surge in current is mitigated and the output waveforms are kept intact. The power loss cause by the addition of a resistor to the leakage current path is negligible, as the magnitude of the obtained leakage current is much less and a maximum of two switches are in conduction mode throughout the operation of HMLI. Also, the energy loss caused by the charging and discharging of a parasitic capacitor (C_p) for input voltage V_{dc} in a time period of T can be given as:

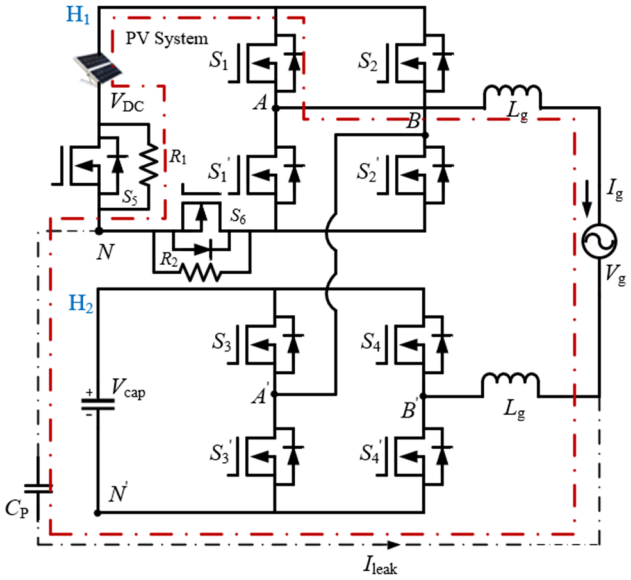
$$P = \frac{C_p V_{DC}^2}{T} \quad (20)$$

with C_p = 100 nF and V_{dc} = 100, power loss is less than 1 W.

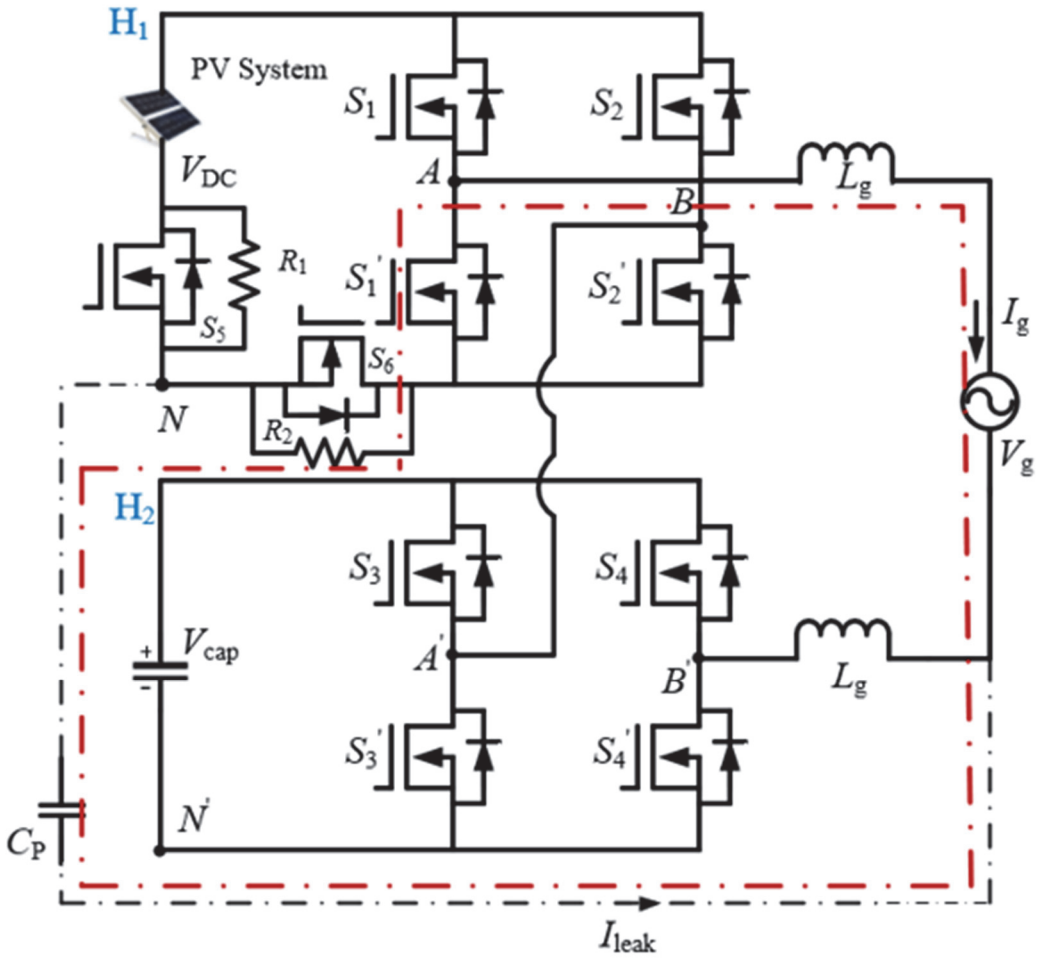
3.4. Weighting Factor and Normalization

There are two ways to choose the weighting factors related to the control objective [28]. The first one is offline and the second one uses mathematical dependencies in the control objective to reach the selected result. Here, W_1 is taken as 0.8 and the W_2 is varied between 1.9 to 18, because of only two terms in Equations (9) and (19), respectively. This can be different for different working conditions. In this work, a normalization method that evaluates the maximum variations of every state variable is used as an extra optimization norm in CF, as given in Equation (20). The modified MPC minimizes the normalized and weighted CF for the switching-state selections.

$$\mathrm{CF} = \sqrt{\left(\frac{G_1}{max(I_{g,i}(k+1)) - min(I_{g,i}(k+1))}\right)^2 + \left(\frac{G_2}{max(V_{cap,i}(k+1)) - min(V_{cap,i}(k+1))}\right)^2} \quad (21)$$



(**a**)



(**b**)

Figure 5. Leakage current path: (**a**) through S_5 (R_1), and (**b**) through S_6 (R_2).

4. Simulation Model and Results

Simulation analysis was carried out to verify the working of the proposed system. In this work, the theoretical analysis of the proposed HMLI system for output current tracking and capacitor voltage balancing and leakage current minimization is discussed in detail. A computer program generated on the basis of the algorithm (shown in Figure 4) is used in the controller design. Simulation was carried out on a MATLAB R2017a with a 64-bit Intel(R) Core ™ i7-4770 CPU operating at 3.40 GHz. Simulations were done on the basis of the presented theoretical analysis and the results of the simulations were subsequently presented.

4.1. Model Description of the HMLI

The HMLI was designed in the MATLAB/Simulink. The various parameter values are listed in Table 3. The first module is supplied by a DC source, while a capacitor is used for the other. For getting a nine-level output of the HMLI, the capacitor voltage needs to be 33% of the input DC voltage.

Table 3. Simulation parameters of HMLI.

Parameters	Values
Inductive load	1.2 mH
Resistive load	20 Ω
DC-Link capacitor	1000 μF
Sampling frequency	10 KHz
DC voltage	150 V
Capacitor voltage	50 V
Reference load current (peak)	6 A

4.2. Simulation Results

The simulation results are at first obtained with an *R-L* load. Figure 6a shows the output voltage waveform. It can be seen that output voltage consists of a nine-level and the peak value of the output voltage is 200 V, which is the sum of the DC-supplied voltage and the capacitor voltage of the other H-bridge.

All the voltage levels observed in the output are 200 V, 150 V, 100 V, 50 V, 0 V, −50 V, −100 V, −150 V, and −200 V, respectively, at 50 Hz. In Figure 6b, the output current and reference current are depicted. From this figure, it can be clearly observed that load current is precisely tracking the reference current. The peak-peak current is 12 A, where the blue line shows the reference current and the red line shows the output current. This demonstrates the quick adaptiveness of the modified MPC algorithm. From these above figures, we can conclude that the system-output voltage and current are perfect according to the theoretical analysis.

The capacitor voltage waveform is balanced at 50 V, as shown in Figure 6c. The capacitor voltage value has a maximum variation of less than 0.25 V (approximately). It is between 50 V and 52 V for a current range of 1 A to 6 A, which shows the effectiveness of capacitor voltage balancing. In Figure 6d, the magnified capacitor voltage is shown for a small interval. In this figure, the capacitor charging and discharging cycles are clearly visible. Whenever capacitor voltage is increased from the reference value, the controller applies the required voltage vector, which discharges the capacitor, and tries to bring it to the reference value. A similar control method is applied to increase capacitor voltage. This process is repeated and the controller balances the capacitor voltage at the desired value. Thus, we can conclude that the simulation is working properly and in accordance with the theoretical analysis.

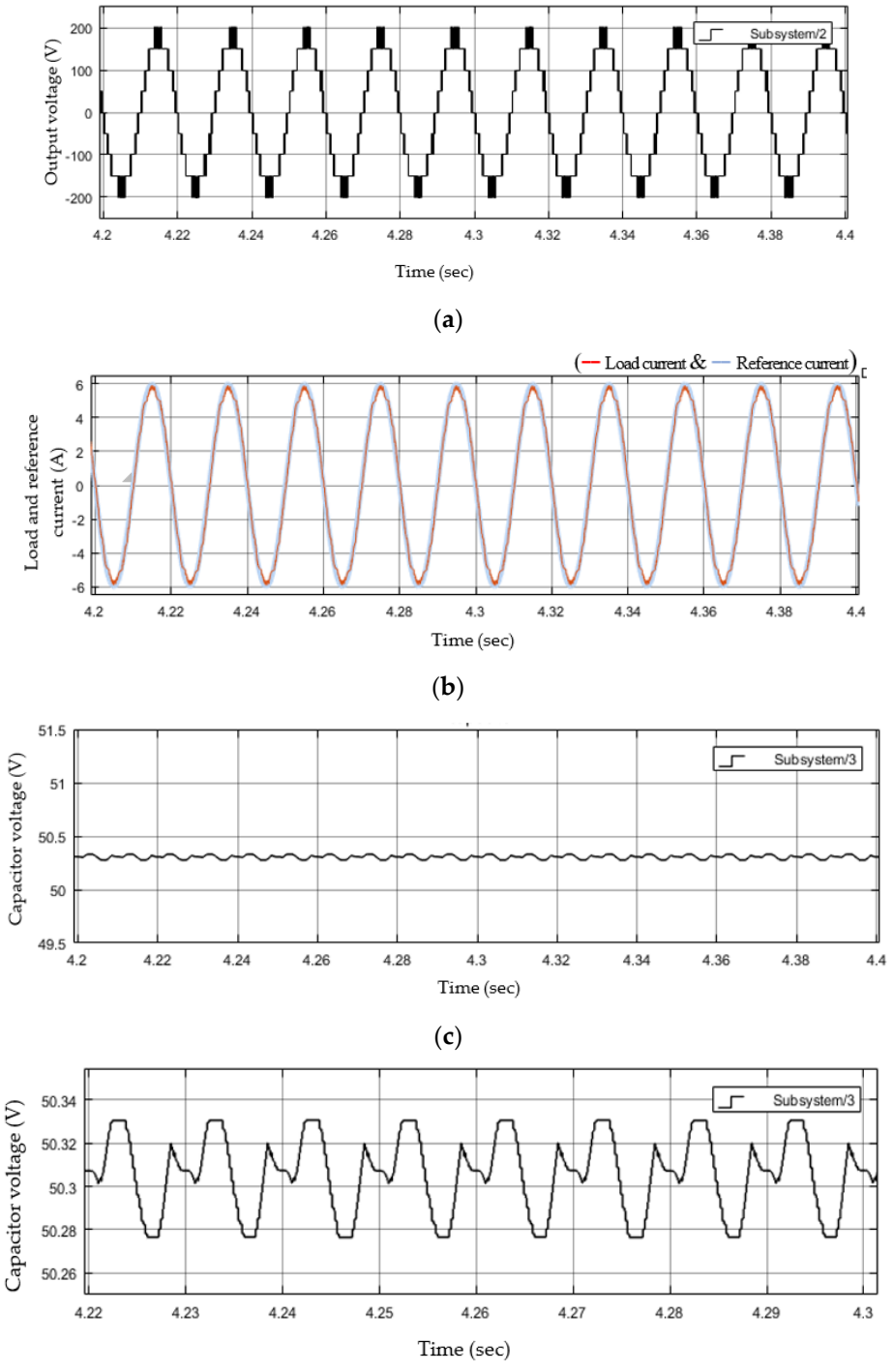


Figure 6. Simulation results of HMLI: (**a**) output voltage waveform, (**b**) load current tracking (– output current & – reference current), (**c**) capacitor voltage with voltage balancing, and (**d**) capacitor voltage charging and discharging.

To show the variation of leakage current in HMLI, the waveform for leakage current and CMV are shown for the transient circuit (TC) in disabled and enabled conditions. Figure 7a,b show CMV and leakage current in the disabled TC and leakage current occurs around 30 mA. Figure 8a,b show CMV and leakage current when the TC is enabled and leakage current occurs around 19 mA.

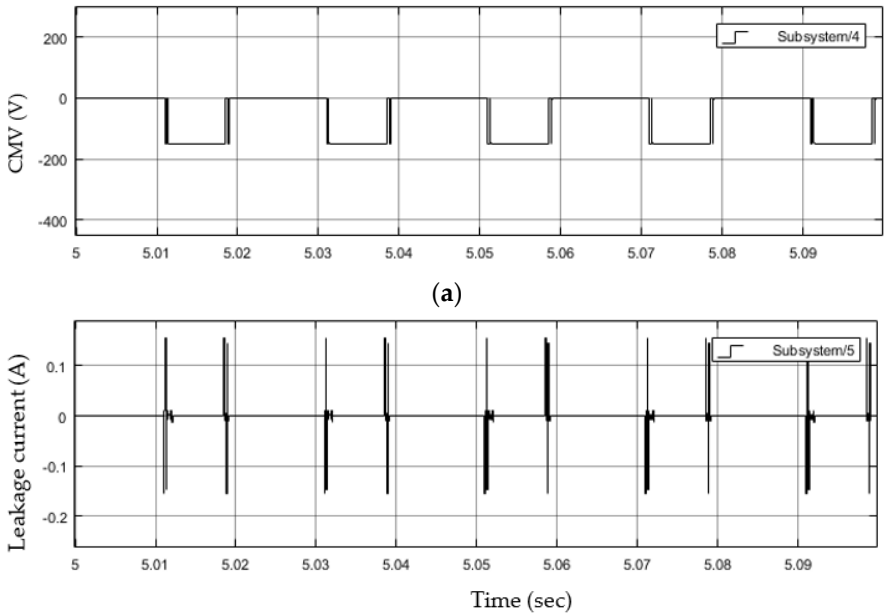


Figure 7. Simulation results of HMLI (disabled TC): (**a**) common mode voltage, and (**b**) leakage current.

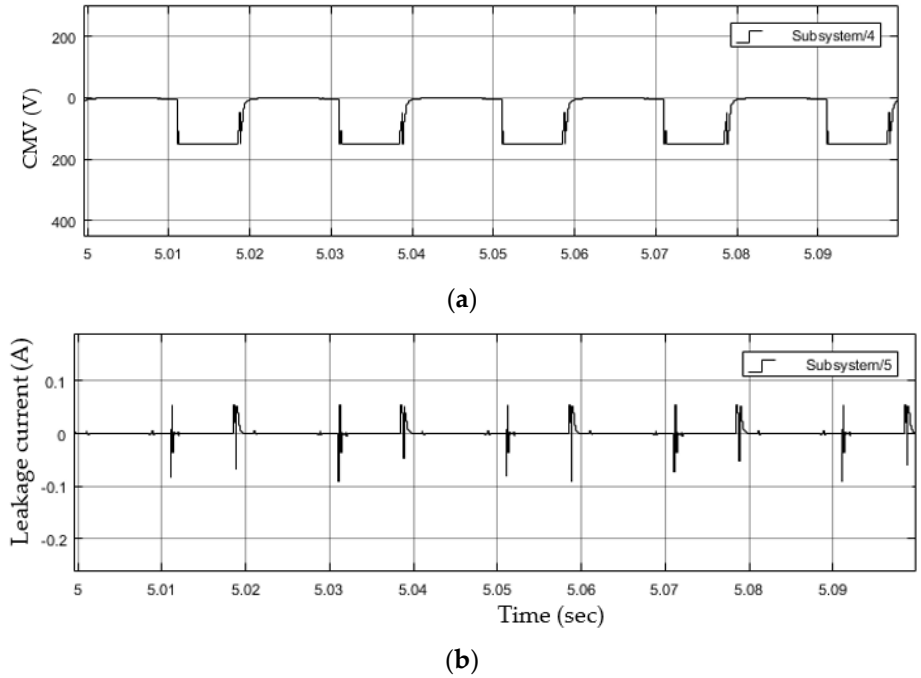


Figure 8. Simulation results of HMLI (enabled TC): (**a**) common mode voltage, and (**b**) leakage current.

4.3. Dynamic Behaviour

For verifying the dynamic performance of the controller, some parameters are changed during the running condition. The simulation is tested when the current reference is changed from 4 A to 6 A and vice-versa. The effect of these transitions on the load current are shown in Figure 9a,b, respectively. From Figure 9a,b, it can be observed that when the reference current is changed at 5 s, the load current is changed to track the reference current. The output current is tracking the reference current accurately whether its amplitude is increased, decreased, or kept constant. Thus, the smooth closed loop control and fast dynamic response of the proposed control scheme is verified.

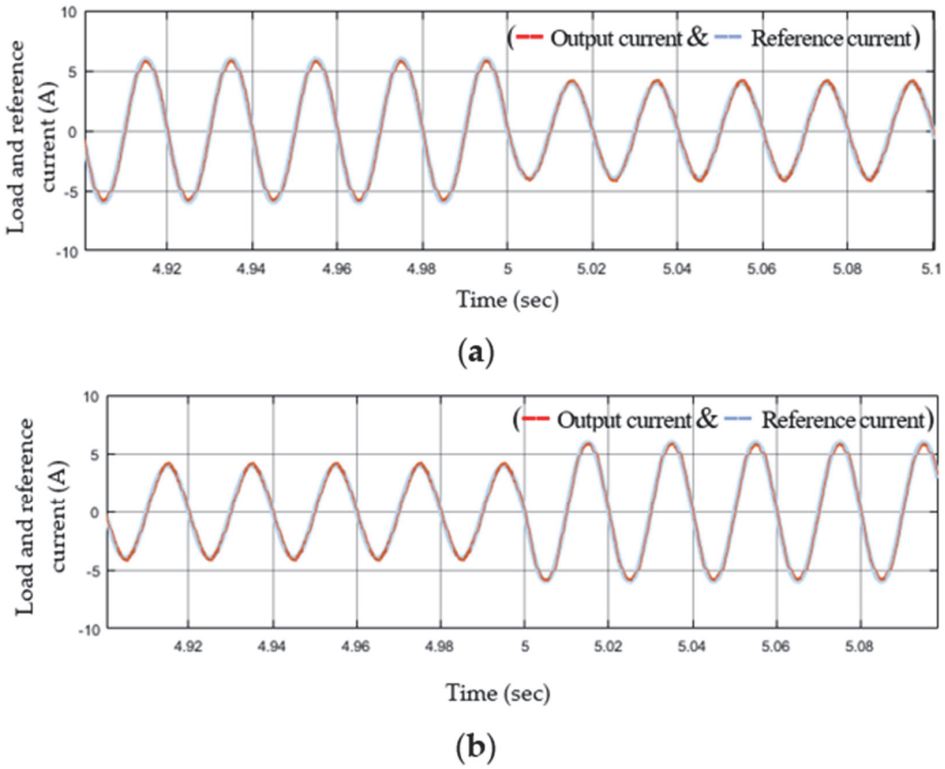


Figure 9. Dynamic results of HMLI: (**a**) load current tracking when decreasing the reference current, and (**b**) load current tracking when increasing reference current.

4.4. Model Description of Grid Connected HMLI

The PV system leakage current standards are provided according to grid safety and regulation. Hence, it is necessary to check leakage current minimization in grid-connected mode. The necessary parameter values are provided in Table 4. The dynamic simulation results are presented here, in which the current is increased at 5 s and decreased at 5.1 s to show the fast dynamic response of the system in grid-connected mode. The grid connection control is implemented using PLL, which provides a phase angle for the current. The provided phase is used with a sine function and a constant magnitude to generate the current reference. Figure 10a shows output voltage levels of grid-connected HMLI. For the current reference of 6 A, HMLI generates seven levels as there is no requirement for two levels (133 V, −133 V) for low current generation. For the current reference of 7 A, HMLI outputs nine voltage levels (−133.33 V, −100 V, −66.66 V, −33.33 V, 0 V, 33.33 V, 66.66 V, 100 V, and 133 V).

Table 4. Simulation parameters for grid-connected HMLI.

Parameters	Values
Inductive load	2 mH
Resistive load	15 Ω
DC-Link capacitor	1000 μF
Sampling frequency	20 kHz
DC voltage	100 V
Grid voltage	110 V (peak)
Capacitor voltage	33.33 V
Reference load current (peak)	7 A

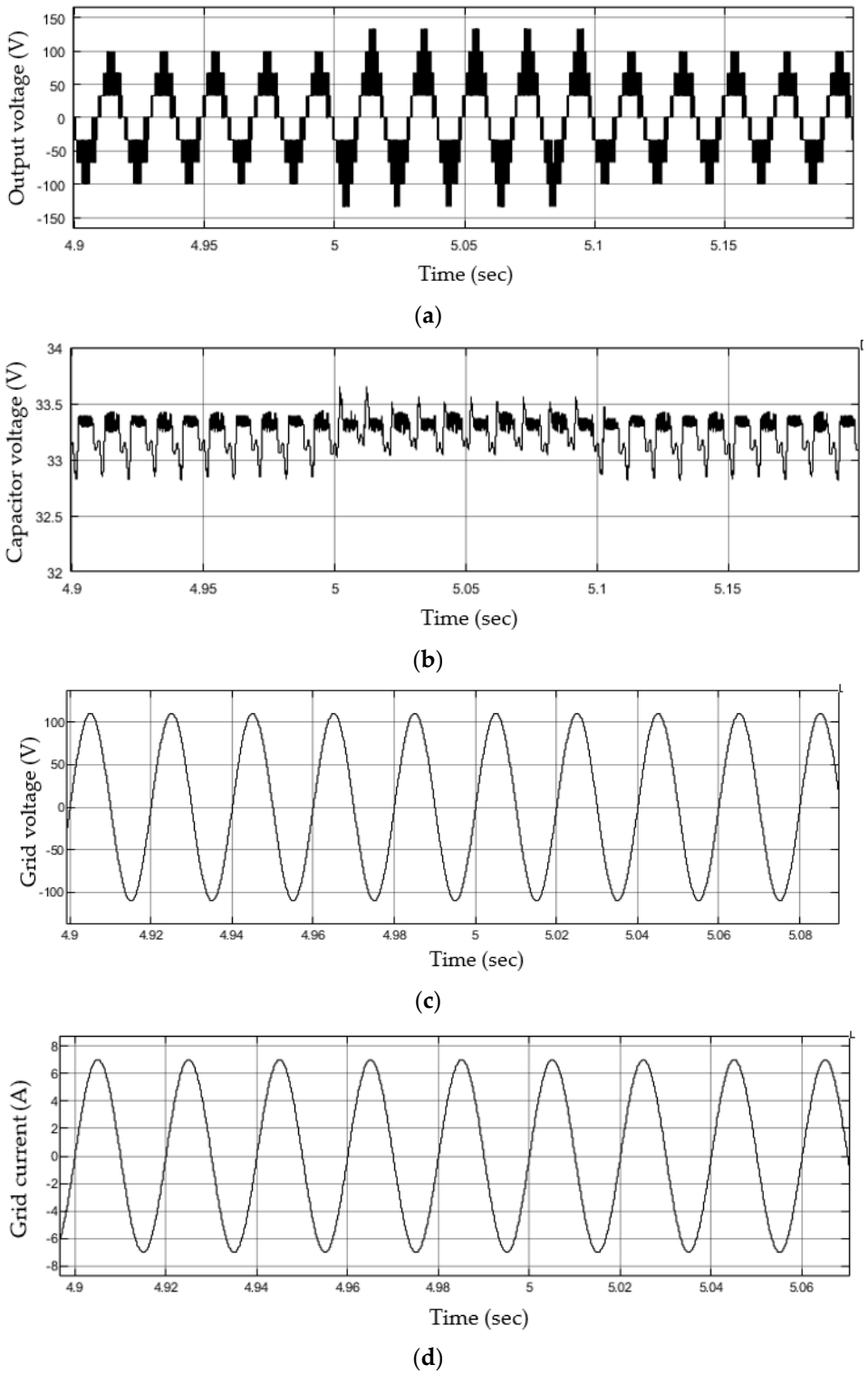
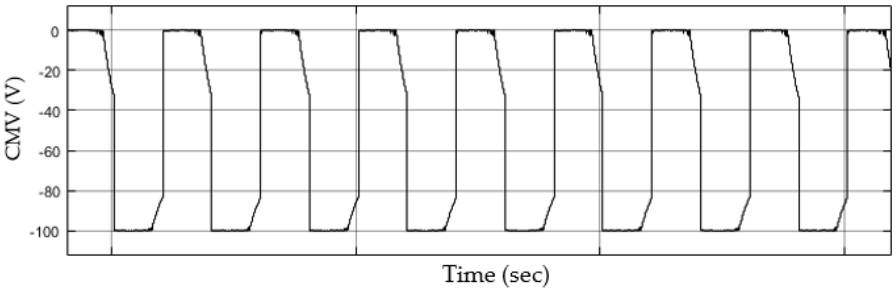


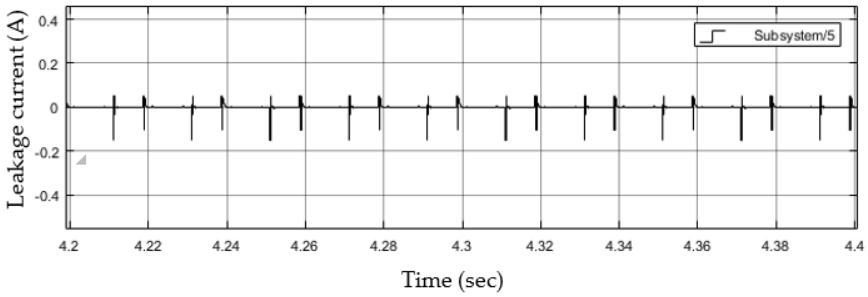
Figure 10. Simulation results of HMLI: (**a**) grid voltage dynamics of HMLI, (**b**) capacitor voltage balancing, (**c**) Grid voltage, and (**d**) grid current.

When the current reference is again decreased to 6 A, the HMLI output voltage generation decreases to seven levels. Similar charging and discharging instances in capacitor voltage can be observed in Figure 10b. The capacitor is provided with charging and discharging vectors in less time as the sampling frequency interval is increased. Figure 10c,d show grid current and grid voltage respectively. Grid current is in accordance with the reference provided and grid voltage does not change because of proper inverter operation.

Figure 11a depicts the CMV of the HMLI. Figure 11b shows the RMS value of the leakage current, measured around 19 mA, and peak to peak it is also less than 300 mA. Both the RMS value and peak-to-peak value are under the regulatory norms. Thus, the simulation results presented here are in accordance with the theoretical expectation.



(**a**)



(**b**)

Figure 11. Simulation results HMLI: (**a**) common mode voltage in grid connected HMLI, and (**b**) leakage current.

5. Experimental Validation

For experimental validation, the system parameters are taken as the same as in the simulation. The components used for the experiment are given in Table 5. The sensor circuits and signal conditioning circuits are designed. The photograph of the experimental setup of the HMLI is shown in Figure 12. In Bridge H1, DC voltage is taken as 100 V and the magnitude of the reference current is set at 6.5 A. To represent the parasitic capacitance of the PV panel, a 100 nF capacitor is inserted into the circuit. Sampling is done at 20 kHz and the setup is tested first for *R-L* loads of 15 Ω and 2 mH.

Table 5. Components used in experiment.

Parameters	Attributes
Voltage sensor	LEM-LV 55 P
Current sensor	LEM-LA 25 P
Microprocessor	TI-TMS320F28335
Switches	IRFPS40N60K
Drivers	FOD-3184

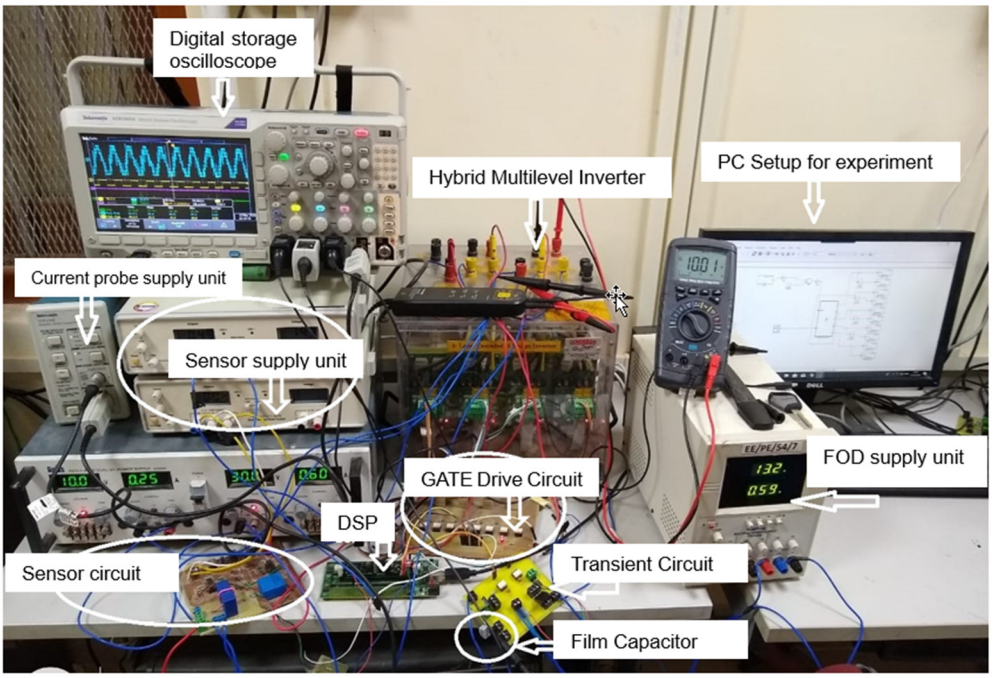


Figure 12. Photograph of the experimental setup.

The experiment was carried for a 600 W laboratory prototype. The steady-state output voltage and load current waveform are shown in Figure 13. The nine-level voltage waveform has been generated at the output of the HMLI. It consists of 0, ±33.33 V, ±66.66 V, ±100 V, and ±133.33 V output voltage levels. The voltage of the capacitor is balanced at 33 V. The output voltage and current magnitude are approximately 84.8 V and 7.05 A (RMS), respectively. The leakage current and CMV waveform are shown in Figure 14. The obtained RMS current is around 20 mA and it can vary within 5% of the given value because of precision errors of the measuring instrument.

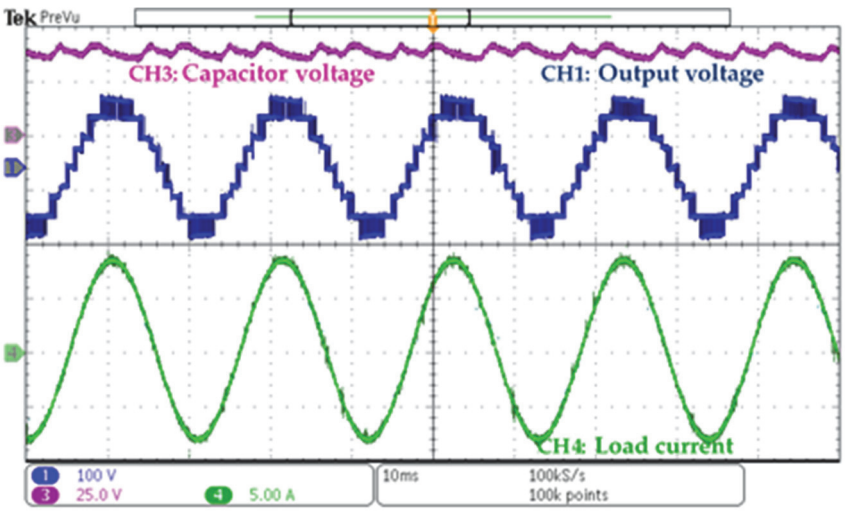


Figure 13. HMLI output voltage (CH1), capacitor voltage (CH3), and load current (CH4) waveform.

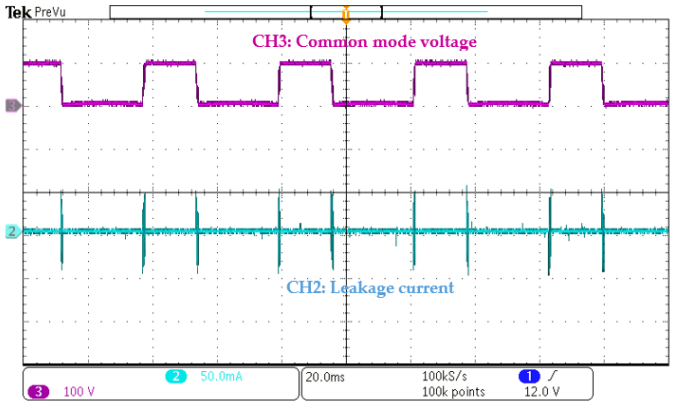


Figure 14. Common mode voltage (CH3) and leakage current (CH2) waveform.

The output voltage of the high voltage (HV) bridge and low voltage (LV) bridge are shown in Figure 15. The important observation to make in Figure 15 is that the voltage switchings of the HV bridge happen only in limited time intervals during a period of grid voltage. Leakage current is also minimized as the legs of HV bridge have a DC supply as a PV panel. The HMLI has also been experimentally validated at grid voltage 110 V (RMS). The grid current is precisely regulated to synchronize with the grid voltage. The grid voltage and current are depicted in Figure 16. The control strategy effectively balances the capacitor voltage balancing and tracks the reference current.

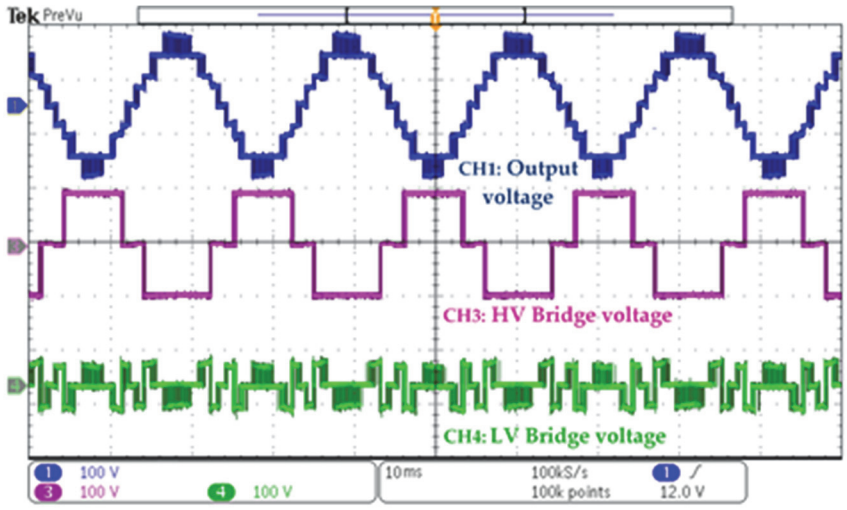


Figure 15. HMLI output voltage (CH1), high-voltage bridge voltage (CH3), and low-voltage bridge voltage (CH4) waveforms.

Figures 17 and 18 show the dynamics of the output voltage for increasing and decreasing currents, respectively. For the low-current value, the control algorithm does not choose high voltage levels as the resistance value is fixed. Hence, at 3 A (peak) current, HMLI generates only five levels. In Figure 17, the current reference is decreased from 7 A (peak) to 3 A (peak) and the opposite sequence is implemented for Figure 18. From both of the figures, it can be confirmed that the proposed MPC provides a fast dynamic response.

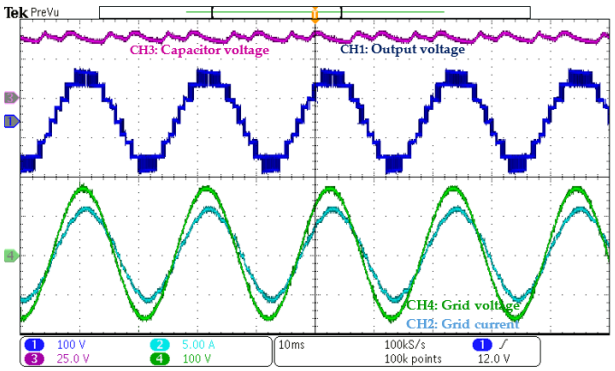


Figure 16. HMLI output voltage (CH1), capacitor voltage (CH3) and grid voltage (CH4), and grid current (CH2) waveforms.

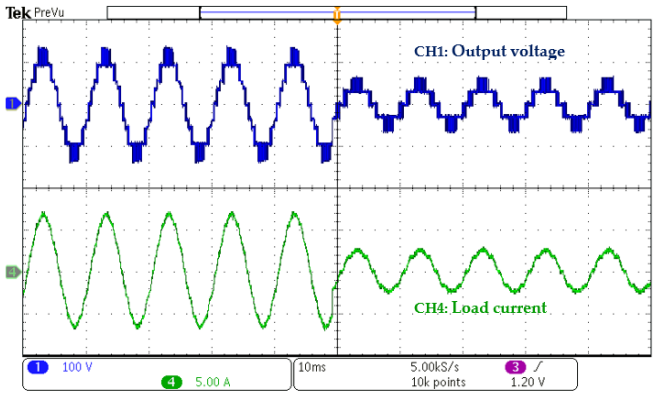


Figure 17. Output voltage (CH1) waveform at a decreasing load current (CH4).

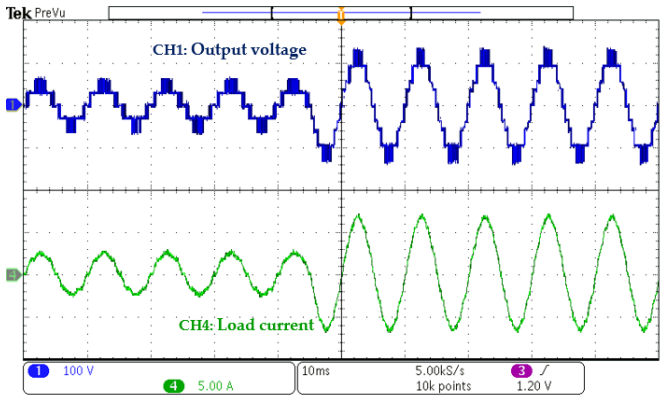


Figure 18. Output voltage (CH1) waveform at an increasing load current (CH4).

The load current dynamics of the proposed controller is also experimentally validated in Figures 19 and 20, respectively, which show that the load current tracks quickly for increased and decreased reference currents, respectively. The system shows excellent dynamic results using the proposed control scheme.

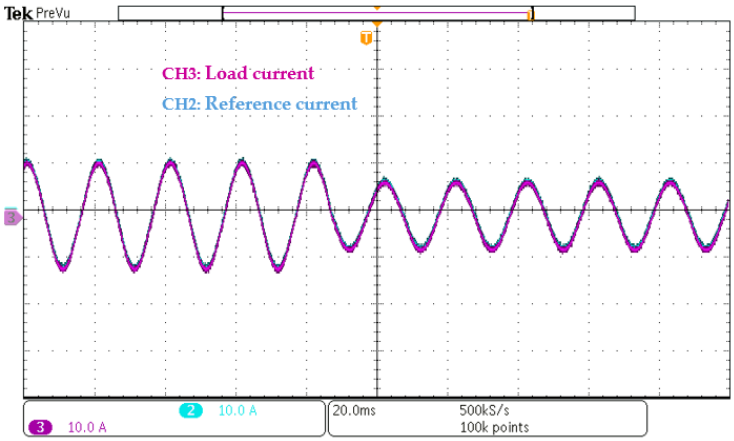


Figure 19. Load current (CH3) waveform at a decreasing reference current (CH2).

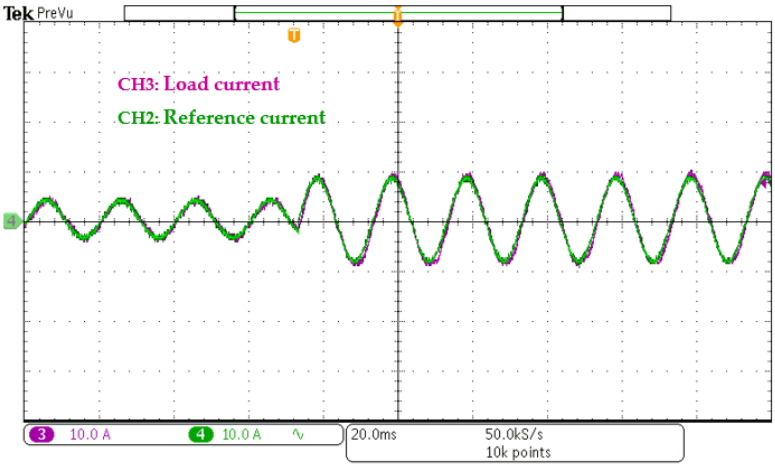


Figure 20. Load current (CH3) waveform at an increasing reference current (CH2).

6. Comparison Results

Generally, in FCS-MPC the number of operations are increased for more voltage vectors and objectives used in the cost function. A computational burden analysis is presented in Table 6. As expected, restricting the required voltage vectors using optimized MPC reduces the burden time. This is also caused by the calculation of $V_{\text{inv, min}}$ before iterating through the vectors. The average execution time in a conventional MPC method is around 110.73 µs and, with optimization, it is reduced to 32.52 µs. Thus, with the proposed MPC-optimization method, an approximate 71% reduction in execution time is achieved.

Table 6. Comparative results in terms of execution time.

Parameters	MPC Conventional Scheme	Proposed Control Scheme
DSP execution time (µs)	110.73	32.52
Reduction rate	-	71.5%

Comparison in Terms of Leakage Current

Comparative results in terms of leakage current and efficiency for various converters are given in Table 7. It can be observed that the proposed controller provides better comparative results in terms of the magnitude of leakage current.

Table 7. Comparative results in terms of leakage current.

Control Technique/Topology	Leakage Current (RMS)	Efficiency %
H5	45 mA	97.59
HERIC	48.8 mA	98.16
Hybrid-bridge topology	80 mA	96.71
Full H- bridge Bipolar modulation	84.5 mA	95.73
PD-MCPWM	98 mA	95.12
Full H- bridge unipolar modulation	2.7 A	93.7
Hybrid topology	2.6 A	97
Proposed	20 mA	98.57

7. Conclusions

In this paper, we propose a modified MPC controller that controls the output current and voltage of the HMLI to a given reference value. It also effectively balances the capacitor voltage. This is achieved through a predictive model and the minimization of specific cost functions to generate switching patterns. The proposed control scheme is also used to reduce the leakage current in modified HMLI and is minimized to an extent of 20 mA experimentally. The steady state and dynamic performances are demonstrated through extensive simulation results. A 600 W laboratory prototype was developed to validate the proposed system through experimentation. The experimental results are in accordance with theoretical analysis. The transient behavior explains the smooth and fast dynamic responses of the controller. All control is achieved without using additional modulation techniques.

Author Contributions: Conceptualization, A.R. and S.-H.H.; writing—review, A.R. and S.-H.H.; investigation, A.R.; editing, A.R. and S.-H.H. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by National Research Foundation of Korea (NRF) grant funded by the Korea Government (MSIT) (No. NRF-2021R1F1A1061713).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Benner, J.P.; Kazmerski, L. Photovoltaics gaining greater visibility. *IEEE Spectr.* **1999**, *29*, 34–42. [CrossRef]
2. Haeberlin, H. Evolution of inverters for grid connected PV-systems from 1989 to 2000. In Proceedings of the 17th European Photovoltaic Solar Energy Conference, Munich, Germany, 22–26 October 2001; pp. 426–430.
3. Alsadi, S.; Khatib, T. Photovoltaic Power Systems Optimization Research Status: A Review of Criteria, Constrains, Models, Techniques, and Software Tools. *Appl. Sci.* **2018**, *8*, 1761. [CrossRef]
4. Jayawardena, K.D.G.I.; Rozanski, L.J.; Mills, C.A.; Beliatis, M.J.; Nismy, N.A.; Silva, S.R.P. 'Inorganics-in-Organics': Recent developments and outlook for 4G polymer solar cells. *Nanoscale* **2013**, *5*, 8411–8427. [CrossRef]
5. Sampaio, P.G.V.; González, M.O.A. Photovoltaic solar energy: Conceptual framework. Renew. *Sustain. Energy Rev.* **2017**, *74*, 590–601. [CrossRef]
6. Xakalashe, B.S.; Tangstad, M. Silicon processing: From quartz to crystalline silicon solar cells. *S. Afr. Pyrometallurgy* **2011**, *1*, 83–100.
7. Szweda, R. Gallium Arsenide. In *A Market and Technology Overview 1999–2004*, 3rd ed.; Elsevier: Amsterdam, The Netherlands, 2000; ISBN 978-1-85617-364-3.
8. Izu, M.; Ovshinsky, S.R.; Deng, X.; Krisko, A.; Ovshinsky, H.C.; Narasimhan, K.L.; Young, R. Continuous roll-to-roll amorphous silicon photovoltaic manufacturing technology. *AIP Conf. Proc.* **1994**, *306*, 198–218.
9. Gong, J.; Liang, J.; Sumathy, K. Review on dye-sensitized solar cells (DSSCs): Fundamental concepts and novel materials. Renew. Sustain. *Energy Rev.* **2012**, *16*, 5848–5860. [CrossRef]
10. Díez-Pascual, A.M.; Luceño Sanchez, J.A.; Peña Capilla, R.; García Díaz, P. Recent Developments in Graphene/Polymer Nanocomposites for Application in Polymer Solar Cells. *Polymers* **2018**, *10*, 217. [CrossRef]

11. Marinova, N.; Valero, S.; Delgado, J.L. Organic and perovskite solar cells: Working principles, materials and interfaces. *J. Colloid Interface Sci.* **2017**, *488*, 373–389. [CrossRef]
12. Kjaer, S.B.; Pedersen, J.K.; Blaabjerg, F. A review of single-phase grid-connected inverters for photovoltaic modules. *IEEE Trans. Ind. Appl.* **2005**, *41*, 1292–1306. [CrossRef]
13. VDE-AR-N 4105: Power Generation Systems Connected to the Low-Voltage Distribution Network—Technical Minimum Requirements for the Connection to and Parallel Operation with Low-Voltage Distribution Networks. DIN_VDE Normo. August 2011. Available online: https://www.vde-verlag.de/standards/0105029/vde-ar-n-4105-anwendungsregel-2011-08.html (accessed on 1 November 2018).
14. Yu, W.; Lai, J.S.; Qian, H.; Hutchens, C. High-efficiency MOSFET inverter with H6-type configuration for photovoltaic non isolated AC module applications. *IEEE Trans. Power Electron.* **2011**, *26*, 1253–1260. [CrossRef]
15. Heribert, S.; Christoph, S.; Jurgen, K. Inverter for Transforming a DC Voltage into an AC Current or an AC Voltage. Europe Patent 1,369,985 (A2), 2 December 2009.
16. Tan, K.S.F.; Rahim, N.A.; Hew, W.P.; Che, H.S. Modulation techniques to reduce leakage current in three-phase transformerless H7 photovoltaic inverter. *IEEE Trans. Ind. Electron.* **2015**, *62*, 322–331.
17. Rodriguez, J.; Lai, J.S.; Peng, F.Z. Multilevel Inverters: Survey of Topologies, Controls and Applications. *IEEE Trans. Ind. Appl.* **2002**, *49*, 724–738. [CrossRef]
18. Lai, J.S.; Peng, F.Z. Multilevel Converters-A new Breed of Power Converters. *IEEE Trans. Ind. Appl.* **1996**, *32*, 509–517.
19. Nabae, A.; Takahashi, I.; Akagi, H. A New Neutral-point Clamped PWM inverter. *IEEE Trans. Ind. Appl.* **1981**, *17*, 518–523. [CrossRef]
20. Peng, F.Z.; Lai, J.S. Multilevel Cascade Voltage-Source Inverter with Separate DC Source. U.S. Patent 5,642,275, 24 June 1997.
21. Guerriero, P.; Coppola, M.; Di Napoli, F.; Brando, G.; Dannier, A.; Iannuzzi, D.; Daliento, S. Three-Phase PV CHB Inverter for a Distributed Power Generation System. *Appl. Sci.* **2016**, *6*, 287. [CrossRef]
22. Lai, R.; Maillet, Y.; Wang, F.; Wang, S.; Burgos, R.; Boroyevich, D. An Integrated EMI Choke for Differential-Mode and CommonMode Noise Suppression. *IEEE Trans. Power Electron.* **2010**, *25*, 539–544.
23. Lee, J.S.; Lee, K.B. New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter. *IEEE Trans. Power Electron.* **2014**, *29*, 1720–1732. [CrossRef]
24. Kang, D.W.; Lee, Y.H.; Suh, B.S.; Choi, C.H.; Hyun, D.S. An Improved Carrier-based SVPWM Method By the Redistribution of Carrier-wave Using Leg Voltage Redundancies in Generalized Cascaded Multilevel Inverter. *J. Power Electron.* **2001**, *1*, 36–47.
25. Mohan, R.M.; Hiralal, S.M. Multilevel inverter to reduce common mode voltage in AC motor drives using SPWM technique. *J. Power Electron.* **2011**, *11*, 21–27.
26. Holmes, D.G.; Lipo, T. Pulse Width Modulation for Power Converters: Principles and Practice. In *Pulse Width Modulation for Power Converters: Principles and Practice*; John Wiley & Sons: Hoboken, NJ, USA, 2003; Volume 18.
27. Baidya, R.; Aguilera, R.; Acuna, P.; Vazquez, S.; Mouton, H.D. Multistep Model Predictive Control for Cascaded H-Bridge Inverters: Formulation and Analysis. *IEEE Trans. Power Electron.* **2018**, *33*, 876–886. [CrossRef]
28. Rodriguez, J.; Kazmierkowski, M.P.; Espinoza, J.R.; Zanchetta, P.; Abu-Rub, H.; Young, H.A.; Rojas, C.A. State of the art of finite control set model predictive control in power electronics. *IEEE Trans. Ind. Inform.* **2013**, *9*, 1003–1016. [CrossRef]
29. Zhang, J.; Yang, Y.; Hu, M.; Fu, C.; Zhai, J. Model Predictive Control of Active Suspension for an Electric Vehicle Considering Influence of Braking Intensity. *Appl. Sci.* **2021**, *11*, 52. [CrossRef]
30. Nagpal, H.; Staino, A.; Basu, B. Application of Predictive Control in Scheduling of Domestic Appliances. *Appl. Sci.* **2020**, *10*, 1627. [CrossRef]
31. Lee, J.H. Model predictive control: Review of the three decades of development. *Int. J. Contr. Autom. Syst.* **2011**, *9*, 415–424. [CrossRef]
32. Kakosimos, P.; Abu-Rub, H. Predictive Control of a Grid-Tied Cascaded Full-Bridge NPC Inverter for Reducing High-Frequency Common-Mode Voltage Components. *IEEE Trans. Ind. Electron.* **2018**, *14*, 2385–2394. [CrossRef]