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A Simple Circuit and Control Topology to Produce Bipolar Non-Inverted and Inverted Voltage Step-Down Features

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Abstract: Single-phase AC–AC converters with a direct power conversion approach are receiving rapid development as they have the ability to produce the regulated non-inverting and inverting form of the input voltage at the output. This feature enables them to correct the line voltage profile once they are used as dynamic voltage restorers if there is an issue of voltage sag or swell in the power distribution system. The regulated non-inverting and inverting form of the output voltage may also be used to obtain the step change in the output frequency, as it is required in many industrial drive systems. However, the realization of such existing circuits needs a large number of components and semiconductor devices, especially switching transistors. The operating control (on and off) of the transistors is directly associated with the use of gate control circuits. The count of such circuits is critical as their volume and cost are much greater than the operating transistors. The number of conducting semiconductor devices in the existing converters is also a big source of high conversion losses, thus leading to lower efficiency. This article introduces a new circuit topology realized only with the use of one full bridge of four IGBTs and a full bridge of four diodes. The use of four switching transistors only requires four gate control circuits that drastically reduce the overall volume and size. All the operating modes of the proposed topology require the conduction of fewer semiconductor devices, which helps to lower the conduction losses. Detailed analysis and description were carried out to validate the attractive features of the developed circuit once compared with the existing circuit topologies. For validation purposes, the computer simulation was carried out on Simulink software. The results obtained from this environment were compared with the real results gained from a practically developed laboratory test bench. The voltage regulation characteristics of the output voltage by employing pulse width modulation (PWM) were confirmed for two values of the non-inverting and inverting outputs.

Keywords: dynamic voltage restorer; sag and swell; industrial drives; gate control circuits; conversion losses; output frequency; pulse width modulation

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1. Introduction

The behavior of the power system in the modern age is highly complicated due to the presence of non-linear loads, devices, and green energy resources. The presence of such systems or devices raises power quality issues. The flow and reliability of the power include the use of robust optimization and artificial intelligence control. A comprehensive review and details related to this area are reported in [1]. The application area of the AC–AC converters includes grid voltage compensation during the voltage sags or swells and speed control systems of industrial loads such as grinding mills employed in mining and steel rolling processes. Currently, the power quality of the grid voltage is highly affected due to the use of non-linear devices and loads in modern power systems. The disturbance of the power system includes the fluctuations of load voltage or unequal voltage problems in a

three-phase system. The short duration voltage variation may be categorized as voltage sag once line rms voltage is reduced. It is known as voltage swell if line rms voltage increases beyond a certain level or value. The correction of such voltage variation can be achieved with a series injection of voltage. These voltage compensators may include flexible AC transmission devices, also known as FACTS devices or controllers [2,3]. The line voltage can be corrected by adding and subtracting injected voltage to increase and decrease the overall line voltage once there is a reduction or an increase in the line voltage [4]. These features of the injected voltage can be practiced with the inverting and non-inverting output voltage forms of the converters. The traditional voltage injection approach converts the DC voltage of a DC source to AC with the help of a voltage source inverter. A transformer at the final stage facilitates the injection of inverter voltage to the line voltage [5,6]. The limited capacity of the DC sources may avoid the solution for longer-duration problems. This drawback is tackled by obtaining the DC voltage from the AC line by employing an AC-to-DC converter. In both previous approaches for voltage compensation, a DC link capacitor is always present between the DC source and inverter, and its use leads to the problem of low reliability [7–9]. In these converters, improving the power quality for input and output is a big challenge. This issue is addressed and tackled in the converters implemented with the multilevel approach, as reported in [10–12]. This power conversion approach may not be effectively employed for the application where voltage regulation or frequency regulation at a discrete level is required.

The use of direct AC–AC converters avoids the use of a DC-link capacitor to reduce the overall size and increase its reliability, as well as the life of a power converting system. The initially developed direct AC–AC converters have only unipolar voltage gain [13], meaning that their output can only be a non-inverted form of the input voltage with voltage buck and boost operation and the inverted version of the input for voltage buck–boost operation. These converters cannot solve all power systems' issues and cannot be used to govern the output frequencies. Bipolar voltage gain is the mandatory requirement to provide the solution for the preceding problems. The bipolar voltage gain capabilities of the output in the direct AC–AC converters can be achieved through various power converting topologies such as Z-source converters [14,15], PWM control with unified power converting approach [16], and switching cell structure [17]. The z-source structure is initially introduced in high switching frequency inverters to avoid the possibility of the short-circuiting of the input DC source as two high-frequency operating transistors in an inverter leg may remain on at the same time. This may happen as there may be some internal defect in the manufacturing process of the switching transistor, or it may be due to a fault in the generation of the control inputs of the operating transistors. Along with this advantage, the other attractive feature in this category of converters is the ability of output voltage regulation. However, the current rating of the operating transistors has to be increased as there may be a problem of high current surges during the shoot-through period. The high-order component of the z-source arrangement slows down the dynamic response. However, z-source converters reported in [14,15] have no facility to produce the non-inverted voltage buck operation. Therefore, these converters cannot compensate for the voltage sag problem with a depth level of less than 50%, which is one of the most occurring problems (more than 50%) in the power distribution system. This problem also increases the complication once the output pulses try to arrange themselves to govern the output frequency. The converters reported in [16,17] can tackle the preceding problems. However, the main issue in these circuits is the requirement of a large number of operating devices that not only increase the overall volume but also lead to an increase in the system's overall cost.

The variable speed drive system requires frequency control to govern the rotating speed of the motors. Some specific loads, such as steel rolling and grinding mills, only need speed control in some selected discrete levels. Here the required speed may be half, one-third, or one-fourth of the machine's rated speed. The control of the motor speed is directly linked with the frequency control. In this frequency control range, voltage control

is mandatory; otherwise, it leads to the core saturation problem in the connected motors. In the motor speed control mechanism, the ratio of the motor's voltage to frequency should be kept constant to maintain magnetic flux constant. Otherwise, the magnetic core of the motor may be saturated and cause the burning of motors. The bipolar voltage-gain direct AC–AC converter is one of the attractive approaches for the load where the required speed regulation is in discrete levels or steps. These converters can produce output voltage with a controllable amplitude that can be in-phase or out of phase with respect to the input voltage. These features of the produced voltage enable the arrangement of the number of positive and negative half-cycles at the output with either polarity of the source voltage according to the required output frequency. Although the characteristics of this output are always in non-sinusoidal forms as it contains unwanted harmonics [18], they are still favorable in numerous fields, as described in [19–21]. The converter reported in [22] belongs to the category of symmetric voltage gain both for voltage in-phase and out-of-phase operation. In this circuit, the number of required active switches is eight, along with three capacitors and two inductors. The count of active switching devices and passive components is reduced in another symmetrical bipolar voltage gain converter [23], as shown in Figure 1. This circuit can govern the magnitude of the output voltage from zero voltage to the maximum value of the input voltage. Its output may be in-phase or out of phase, with input voltage ensuring the non-inverting and inverting operation. This circuit can effectively be used to vary the output frequency in discrete steps just by modifying the control signals. There is the use of six active switching devices and eight diodes. There is always the conduction of two transistors and two diodes to produce the required output. The number of gate control circuits is proportional to the number of active switching devices. The reduction in the use of switching transistors effectively compacts the overall circuit volume and cost.

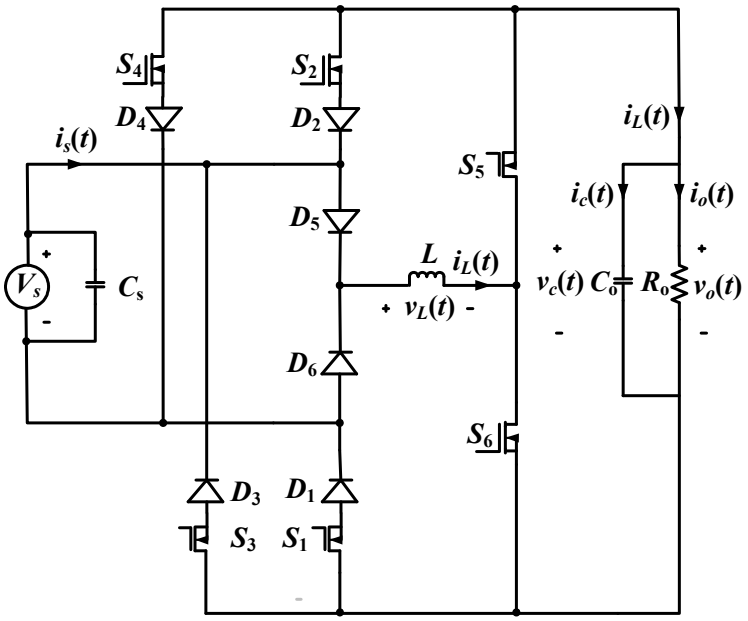


Figure 1. Conventional symmetrical bipolar voltage gain converter.

In existing circuits, the following are the main issues that need to be addressed for a reliable and efficient power conversion process.

1. There is the conduction of more switching devices or components that increases the conduction losses;
2. Using a large number of active switching devices increases the overall size as the volume of the gate control circuit is larger than that of the operating devices;
3. Switching schemes and circuit topologies are complex to realize the required output.

The formerly stated deficiencies, as reported in the literature, are tried to cope with the newly developed circuit topology, as illustrated in Figure 2. There is a use of eight diodes, in which four diodes (D_1 to D_4) operate at low line frequency, contributing to no switching losses as their switching frequency is low. Two diodes (D_7 and D_8) connected across the fast switching transistors (Q_2 and Q_4) never conduct and are only used for protection as they remain reverse biased with respect to the polarity of the source or load voltage. These diodes ensure the elimination of the current interruption problem of the inductive current; otherwise, there is a risk of failure of the operating devices due to the generation of high inductive voltage surges. The remaining two diodes (D_3 and D_5) have to operate at a high switching frequency, but their switching losses can also be ignored as they have low reverse recovery times. These diodes only conduct in the PWM-off intervals of the high-frequency operating transistors. The instantaneous currents of these conducting diodes are the same as the filtering inductor's current. These diodes can contribute to conduction losses.

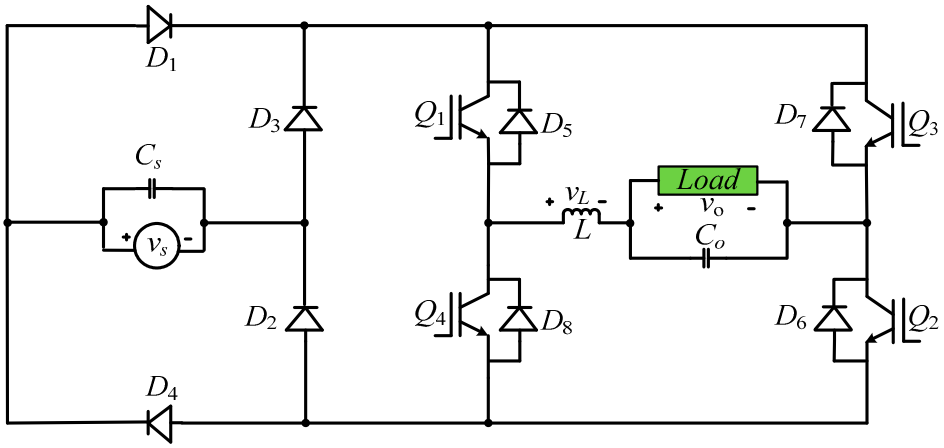


Figure 2. Proposed compact size bipolar voltage gain AC–AC converter.

The noticeable feature of this recommended circuit is the use of only four transistors instead of six, as used in [23]. This would help compact the converter in terms of size and overall cost, as these values of the gate control circuit are much larger than the operating transistor. Input and output (load) terminals are connected to capacitors to main their power quality indexes at acceptable levels. One inductor always remains connected in series with the load for the switching intervals in which the power is stored and transformed to the load. A reliable low film value capacitor with low losses may be connected at the output of the rectifier circuit or the input of the inverter. A summary of the noticeable characteristics of the proposed circuit may be enlisted as:

1. There is the use of a fewer number of active switching devices;
2. There is also a reduction in two gate control circuits compared to the circuit in [23];
3. The overall impact of this achievement is the reduction in size, cost and conversion losses;
4. Only two commercially available single-phase diode and inverter modules may be effectively employed to obtain the required results;
5. The problem of control complication is tackled by introducing a simple switching algorithm that can be successfully used to produce the non-inverting and inverting outputs.

The remaining arrangement of this manuscript includes the description of possible operating modes in Section 2. It also includes the design procedure to find out the values of the filtering components employed at output and input to tackle the problem of their power quality. Section 3 covers the detailed analysis where the attractive characteristics of the proposed circuit are compared with the available similar existing circuits. The test results gained from the computer simulation environment and the practically developed model are represented in Section 4. A case study was introduced in Section 5 to explore

one of the application areas of the proposed circuit for grid voltage compensation. The conclusion is stated in Section 6.

2. Operating Principle of the Proposed Circuit

This section details all operating modes of the established circuit, indicating how the output can be produced as a non-inverting and inverting form or version of the input voltage. This study is detailed with the help of the control signals and current conduction loops formed to transfer power from input to output. The low and high-frequency operating behavior of the active switching devices is governed with respect to the control algorithm, as illustrated in Figure 3. This figure clarifies the non-inverting and inverting behavior of the output voltage with any half cycle or polarity of the input voltage. In the given output voltage waveform, the output voltage is a non-inverting form of the input voltage for the first and second half cycles of the first and second cycles of the input voltage. Similarly, the output is an inverting version of the input for the second and first half cycles of the first and second cycles of the input voltage, respectively. There is a switching of one low and one high-frequency transistor at any time instant during its operation. The role of the full-bridge rectifier circuit shown on the front-end side is to fold the sinusoidal input voltage (v_s) into its absolute form across the input terminal of the inverting voltage circuit. The magnitude of this absolute version of the sinusoidal and input voltage is the same. The role of the inverter circuit is to transform this voltage into its non-inverted and inverted form with voltage regulating capabilities available across the load terminal in the form of output voltage (v_o). With respect to the absolute form of the input sinusoidal voltage, the non-inverted and inverted voltage buck operation can be completed in four operating modes. However, there is a requirement for a detailed operation to show how the input power is transferred from the source side to the output via the filtering inductor and how the stored energy of the inductor is transferred to the output during turn-on and off periods of the high-frequency PWM control, respectively. With the help of all these current conducting loops, the value of the inductor voltage and capacitor current for PWM on and off intervals can be computed to find the state space representation or voltage transfer ratio for any polarity of the input or output voltage. The detail of how this target is achieved with the operation of the active switching devices is described under the heading of non-inverting and inverting operations.

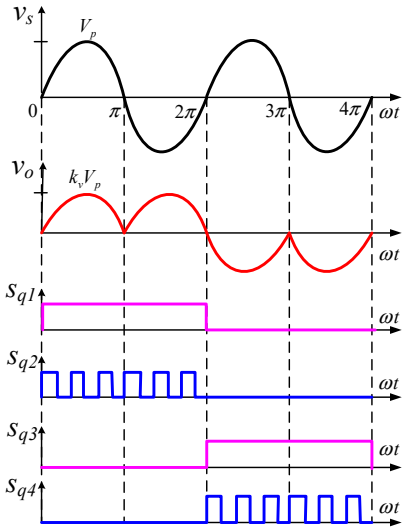


Figure 3. Control signals producing the non-inverting and inverting outputs.

2.1. Non-Inverting Voltage Buck Operation

In this operation, the phase difference between the input and output voltage is maintained at zero means that the output voltage is positive and negative, respectively, for the positive and negative value of the input voltage. This operation is split to mode I, where

input and output voltages are positive, but in operating mode II, input and output voltages are negative. In both cases, output and input voltage are in-phase, ensuring zero phase difference between them. The operation of each mode may be divided into two segments that are categorized with respect to turn-on and turn-off intervals of a high-frequency PWM control signal. The equivalent circuits in which the input source transfer its power to output for the operation of mode I and II are illustrated in Figure 4a–d, respectively. These figures illustrate the voltage step-down operation for positive and negative half cycles of the input voltage. During the operation of mode I, the active switching transistor Q_1 maintains its on-state for the period in which the input voltage is positive. However, the switching transistor Q_2 operates in conduction and non-conduction mode during PWM kT and $(1-k)T$, in which output inductor 'L' store energy from input and release the energy towards the output. The diodes D_5 to D_8 remain reverse biased once transistors Q_1 and Q_2 are conducted to store the input power to output inductor 'L', as may be viewed in Figure 4a. The diode D_7 starts conducting to divert the flow of the inductor from transistor Q_2 to D_7 once Q_2 turns off. This behavior of the operating devices ensures the continuous flow of the inductor current, as seen in Figure 4b. For the operation of mode II, where the input voltage is negative, and the required output voltage is also negative, the role of transistors Q_1 and Q_2 is exchanged with transistors Q_3 and Q_4 (see Figure 4c,d).

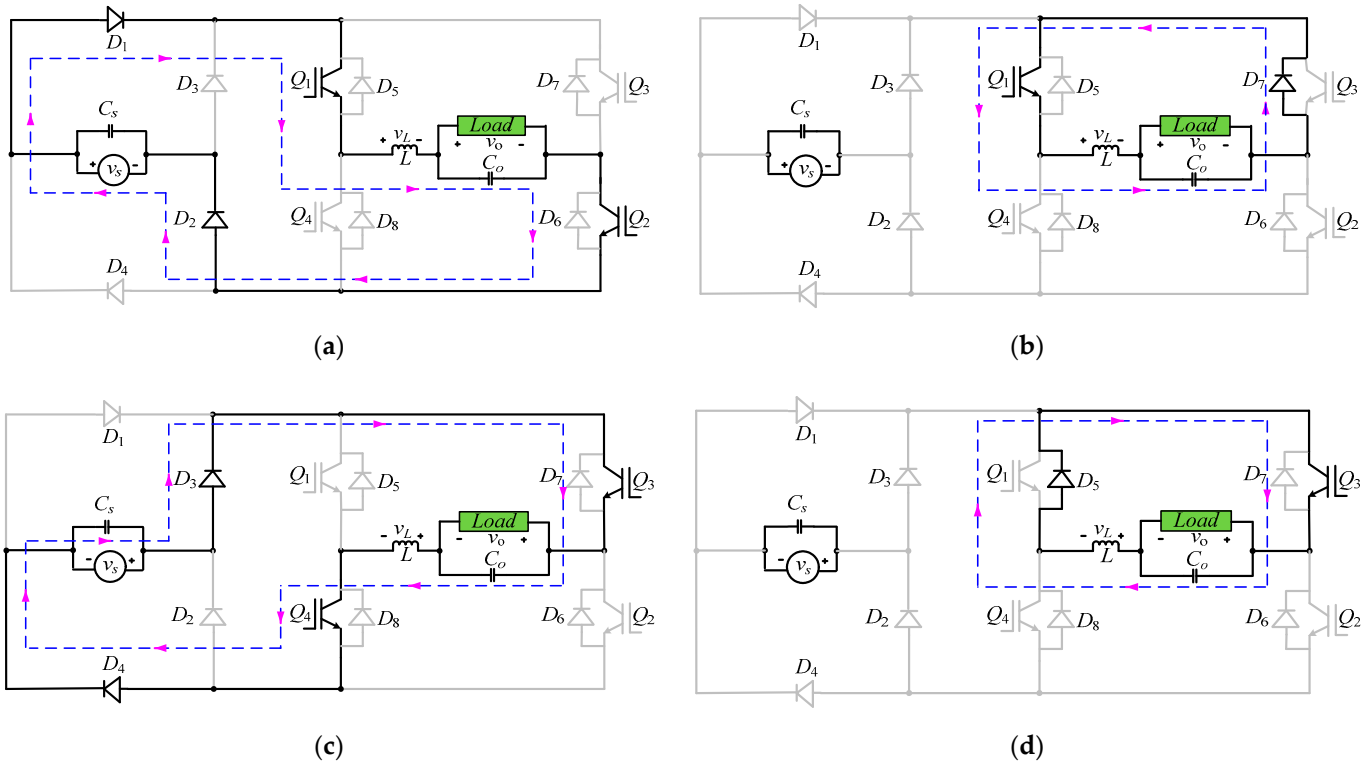


Figure 4. Equivalent power transfer circuits for non-inverting voltage buck operation: (**a**,**b**) for mode I and (**c**,**d**) for mode II.

Loop analysis theory may be used to find the equations of instantaneous inductor voltage for the operation of modes I and II.

$$v_L(t) = v_s(t) - v_o(t) \tag{1}$$

$$v_L(t) = -v_o(t) \tag{2}$$

It is clear from Figure 4a,c that the inductor voltage is a difference between the input and output voltage. The input voltage is zero as a source is isolated, as seen in Figure 4b,d. The average value of the inductor voltage is always treated as zero as its energy absorbed

in the on-period of the PWM signal is released to load during the off period of the PWM signal. This concept may be employed to find the voltage gain k_v.

$$\frac{1}{T}\int_0^T v_L(t)dt = \frac{1}{T}\int_0^{kT}[v_s(t) - v_o(t)]dt - \frac{1}{T}\int_0^{(1-k)T} v_o(t)dt \tag{3}$$

$$\frac{V_o}{V_s} = k = k_v \tag{4}$$

The overall voltage gain is directly linked with the duty cycle control (k), which validates the voltage buck operation.

2.2. Inverting Voltage Buck Operation

This operation reverses the polarity of the output voltage with respect to the input voltage. The explanation of this behavior can be easily understood with its operation in modes III and IV. In the operation of mode III, where the output is negative for positive input voltage, the requirement of the operation is performed with the conduction of transistors Q_3 and Q_4 by establishing a current conduction path in which power is being stored in the inductor and also consumed by the load, as can be seen from the underlined path of Figure 5a. In this operation, as the output is an inverted form of the input, the inductor voltage is the sum of the input and output voltage, as can be analyzed from the loop analysis of Figure 5a.

$$v_L(t) = v_s(t) + v_o(t) \tag{5}$$

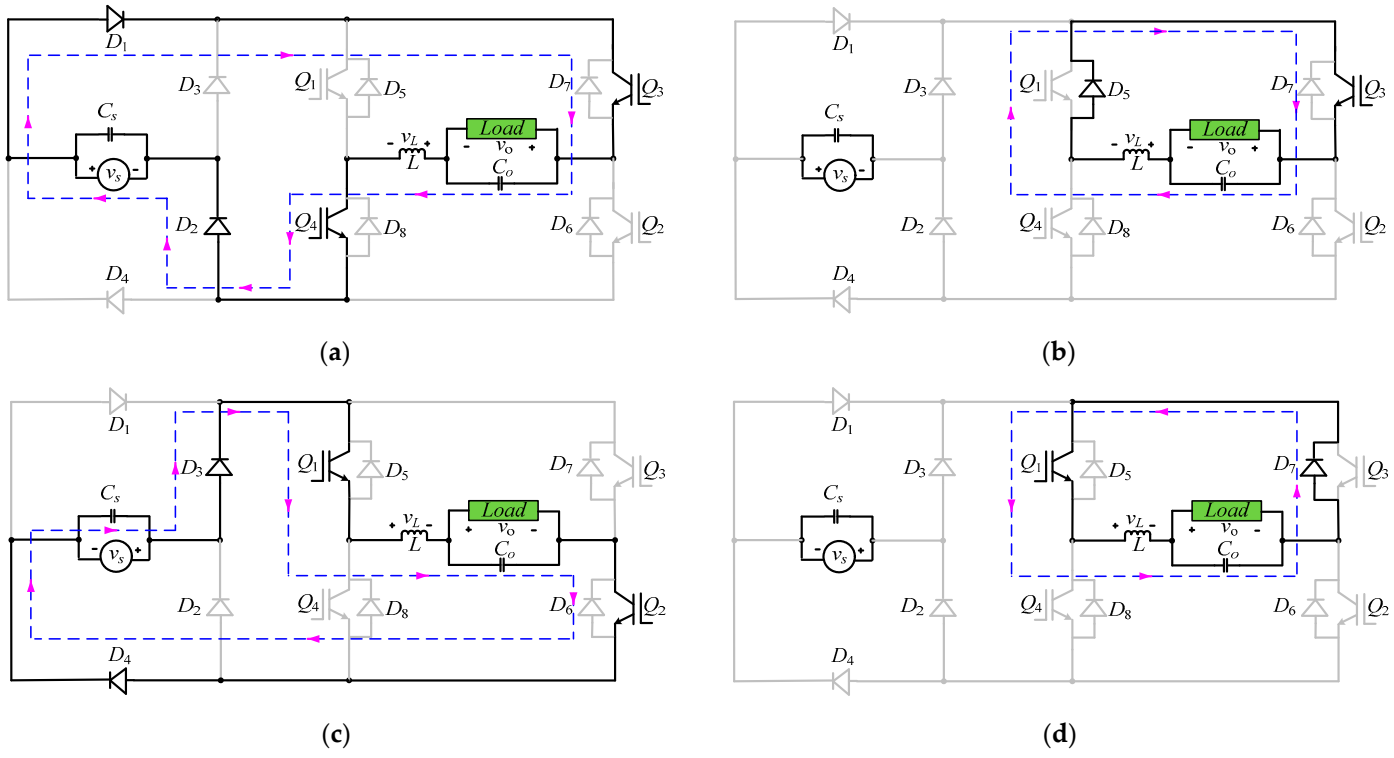


Figure 5. Equivalent power transfer circuits for inverting voltage buck operation: (**a**,**b**) for mode III; (**c**,**d**) for mode IV.

In the second interval of operating mode III, the conduction of transistor Q_4 and diode D_6 facilitates the recovery of the stored energy of the inductor, as depicted in Figure 5b.

There is no change in the value of the inductor voltage, as seen in the operation of modes I and II.

$$v_L(t) = -v_o(t) \tag{6}$$

The inverting requirement of output voltage for the negative input voltage is achieved by shifting the switching behavior of the transistors Q_3 and Q_4 to Q_1 and Q_2, respectively. The power transferring loops of Figure 5c,d illustrate how the input power is stored in the inductor PWM on interval and is released to load during the PWM off interval.

Equations (5) and (6) also hold their states for the inverting operation of the input voltage. Equation (3) can be modified to determine the voltage transfer ratio for voltage inverting buck operation.

$$\frac{1}{T}\int_0^T v_L(t)dt = \frac{1}{T}\int_0^{kT} [v_s(t) + v_o(t)]dt - \frac{1}{T}\int_0^{(1-k)T} v_o(t)dt \tag{7}$$

$$\frac{V_o}{V_s} = -k = -k_v \tag{8}$$

The negative signs with Equations (7) and (8) ensure that the output voltage always exists in the inverted form of the input voltage. This section comprehensively explains the circuit operation employed to regulate the output voltage from some minimum level (ideally zero volts) to the value of the input voltage in non-inverting and inverting forms. The control of the duty cycle helps regulate the output voltage.

2.3. Filtering Components and Their Design

The detail of the procedure to design or determine the values of the filtering components, including the energy storing inductor and input and output capacitors, is described in [24]. These components help to improve the power quality of the output voltage and input current by lowering their ripples. For example, the output capacitor (C_o) not only helps to minimize the ripples in the output voltage but also supplies some reactive power in case of inductive load. Similarly, the capacitor connected to the input side (C_s) eliminates the harmonics or ripples that are resulted due to high switching operation of the semiconductor devices. This capacitor also helps to improve the power quality concerns of the input current. The role of the series inductor (L) is to store the input power in the form of a magnetic field in the on-interval of the switching interval and then release it to load in the off interval of the switching period. In variable frequency operation, the developed topology can also be used to lower the load frequency in some selected discrete steps. There may be a capacitive coupling problem between the rotor and stator due to generated high-frequency harmonics. Moreover, the presence of the series filtering inductor blocks the high-frequency harmonics from going toward the load. The ripple contents in the inductor current and output voltage are represented by the current ripple factor (k_{ir}) and capacitor ripple factor (k_{vr}). As a rule of thumb, these values are taken as 20% of the inductor current and 10% of the output or input voltage, respectively. The switching frequency, duty cycle, input voltage, average inductor current, and output or input currents for these calculations are taken as 25 kHz, 0.6, 120 V, 5 A, and 1 A, respectively. Based on these values, the value of the energy storing or filtering inductor is computed as

$$L = \frac{V_s k(1-k)}{k_{ir} I_L f_s} = 1.15\,\text{mH} \tag{9}$$

The ripples of the output capacitor are linked with its capacitance. Its value with the given condition is calculated as

$$C_o = \frac{kI_o}{k_{vr} V_o f_s} = 3.47\,\mu\text{F} \tag{10}$$

A similar approach and the same given values are used to find out the value of the input capacitor is as

$$C_s = \frac{I_s(1-k)}{k_{vr}V_s f_s} = 1.3\,\mu\text{F} \tag{11}$$

Therefore, these values are approximated to 1 mH, 4.7 µF, and 2.2 µF for filtering inductor, output, and input capacitors, respectively.

3. Validation through Comparative Analysis

The effectiveness of the proposed circuit can be proven by computing the peak value of the switching currents of the semiconductor devices as it is used to compute their average and rms value. The maximum break-over voltage and the value of the conversion losses, especially conduction losses, are the main parameters for the comparative analysis. The number of active transistors used is a key factor that determines the overall size and cost of the switching converter. For the on–off operation of a switching transistor, the control signal is applied at its control terminal with respect to its reference terminal. However, in high switching AC–AC converters, the reference terminal of the used transistors is always not at the same potential level. Thus, the switching operation of a transistor cannot be successful without employing a gate control circuit. Therefore, the number of gate control circuits is almost equal to the number of switching transistors. The realization of a gate control circuit requires large space due to the use of a large number of passive components and semiconductor devices. Therefore, mostly the cost and size of a gate control circuit exceed the required space and size of a transistor. The use of a large number of switching transistors always remains a big challenge for the design engineer. The proposed topology may be one of the possible choices for the design as its implementation only needs four switching transistors, as in [23], ensuring a reduction in two switching transistors.

The voltage rating of the semiconductor devices is determined by the value of the maximum break-over voltage that develops across them during their off-state condition. In this regard, the maximum break-over voltage of the employed transistors and diodes (switching devices) is equal to the peak value of the input voltage.

$$V_{p(sd)} = V_{s(p)} \tag{12}$$

In a similar approach, the peak value of the switching devices depends on the instantaneous value of the inductor current. This value in voltage buck operation is equal to the instantaneous output current. The value of the peak ripple current is ignorable as the selected switching frequency is very high. The peak value of the switching devices' current may be approximated by the peak load current.

$$I_{p(sd)} = I_{o(p)} \tag{13}$$

With the connection of the output capacitor, the load current can be treated in sinusoidal form as

$$i_o(\omega t) = I_{o(p)} \sin(\omega t) \tag{14}$$

The maximum conduction period of a diode or a transistor in the proposed converter or converter in [23] cannot exceed the half period of the input voltage. The conduction losses of a transistor with its internal resistance R_Q or a diode with given forward voltage V_D and forward resistance R_D in the above-stated period can be computed by considering the sinusoidal characteristics of switching current as

$$P_{cond(diode)} = \frac{V_D I_{o(p)}}{\pi} + \frac{I_{o(p)}^2}{4} R_D \tag{15}$$

$$P_{cond(transistor)} = \frac{I_{o(p)}^2}{4} R_Q \tag{16}$$

In the proposed circuit, during the one period of the output voltage for the value of voltage gain (k_v) of 0.5, there is the conduction of three transistors and three diodes in the half period equivalent form. The total conduction losses of these devices are calculated as

$$P_{cond} = \frac{3V_D I_{o(p)}}{\pi} + \frac{3I_{o(p)}^2}{4}\left(R_Q + R_D\right) \tag{17}$$

However, with the above-stated condition, the converter's output in [23] needs the conduction of four transistors and four diodes. Correspondingly, their overall conduction losses can be obtained as

$$P_{cond} = \frac{4V_D I_{o(p)}}{\pi} + I_{o(p)}^2\left(R_Q + R_D\right) \tag{18}$$

Switching losses of the operating diodes at low and high frequencies are ignorable as they have low switching frequencies and low values of their reverse recovery times, respectively [12]. The switching losses of the high-frequency operating transistor depend on the value of voltage and current at which they change their switching states, meaning on to off or off to on. These losses are also governed by their rise (t_r) and fall times (t_f). In this calculation, the value of the voltage and current may consider constant, and their variation can be negligible in one high-frequency switching period. The maximum losses of one high-frequency (f_s) operating transistor are calculated here as

$$P_{sw(transistor)} = \frac{1}{6} f_s V_{s(p)} I_{o(p)} \left(t_r + t_f\right) \tag{19}$$

The switching losses of the transistors operating at low frequencies are always ignorable, and only high-frequency operation transistors can be considered for this calculation. There is a high switching frequency operation of two and four transistors in the proposed converter and converter described in [23]. The maximum switching losses of these converters are calculated in Equations (20) and (21) of the proposed converter and converter of [23] in the following forms as

$$P_{sw} = \frac{1}{3} f_s V_{s(p)} I_{o(p)} \left(t_r + t_f\right) \tag{20}$$

$$P_{sw} = \frac{2}{3} f_s V_{s(p)} I_{o(p)} \left(t_r + t_f\right) \tag{21}$$

The summary of the comparing performance parameters is given in Table 1 for a quick review and evaluation. Here it can be observed that for the generation of similar characteristics of the output voltage, the proposed topology offers low conduction and switching losses by using a low number of the operating transistor. Therefore, the proposed converter may be one of the favorable choices for circuit developers or designers as it is attractive in terms of overall size, cost, circuit, and control simplicity.

Table 1. Validation of the performance characteristics.

Comparing Parameters	Proposed Converter	Converter in [23]
Count of diodes	8	8
Count of transistors	4	6
Count of gate drivers	4	6
Peak switching voltage	$I_{o(p)}$	$I_{o(p)}$
Peak switching voltage	$V_{s(p)}$	$V_{s(p)}$
Average conduction losses	$\frac{3V_D I_{o(p)}}{\pi} + \frac{3I_{o(p)}^2}{4}\left(R_Q + R_D\right)$	$\frac{4V_D I_{o(p)}}{\pi} + I_{o(p)}^2\left(R_Q + R_D\right)$
Peak switching losses	$\frac{1}{3} f_s V_{s(p)} I_{o(p)} \left(t_r + t_f\right)$	$\frac{2}{3} f_s V_{s(p)} I_{o(p)} \left(t_r + t_f\right)$

4. Confirmation from Simulated and Practical Results

This section confirms the theoretical and real value analysis of the previously discussed concepts. Here it is proved that the proposed circuit can vary the load peak or rms voltage with the control of the duty cycle. For this purpose, two values of the output voltage were selected. One value of the output voltage is less than the half value of the input voltage, while the other is greater than this level. The peak value of the input voltage was set to 170 V peak to obtain the 50 V and 100 V peak voltage by adjusting the value of the duty cycle control near about 0.3 and 0.6, respectively. The other value of the duty cycle control may be employed to obtain any desired value of the output voltage. With this voltage regulation capability of the output voltage, its non-inverting and inverting features were also tested for the application of voltage control and frequency control. Half frequency output voltage waveform also verifies the voltage regulating features and voltage non-inverted and inverted forms of input voltage. The test of the features mentioned above was separately validated with simulation results from MATLAB software and practical results obtained from hardware setup.

4.1. Verification with Simulation Results

The simulation platform is one of the favorable and simplest environments to test and analyze the characteristics of any switching converter prior to its practical realization. Here, it is possible to obtain or develop a model of any solid-state device or components and even any segment of the power converting circuit. There is no need to sense the polarity of the input voltage as it is mandatory for real-time implementation, as generated control inputs are inherently aligned with source voltage. The switching transistor was modeled by using an ideal block of a fully operating switch. Its internal parameters were modified in accordance with the values obtained from the datasheet of the transistor used in the circuit employed for practical verification. An inductor of 1 mH was connected in series with the load, and a 4.7 μF capacitor was connected across the 150 Ω load, as shown in the proposed circuit in Figure 2. The voltage gain of the converter for the simulation result was set to 0.5, and an improvement in the power quality of the output was gained with a switching frequency of 25 kHz. The plots of Figure 6a,b validate that the proposed topology can produce non-inverting and inverting forms of the input voltage, and their value is governable with the adjustment of the duty cycle control. The plot of Figure 6c indicates that step variation in the load frequency can be made possible with the proper setting of the non-inverting and inverting forms of the input voltage. In the present form, there are two consecutive positive and two negative pulses that double the period of the output voltage with respect to the input. Increment in the output period lowers its frequency accordingly. An alternative way can be adopted to set some other values of the output frequencies.

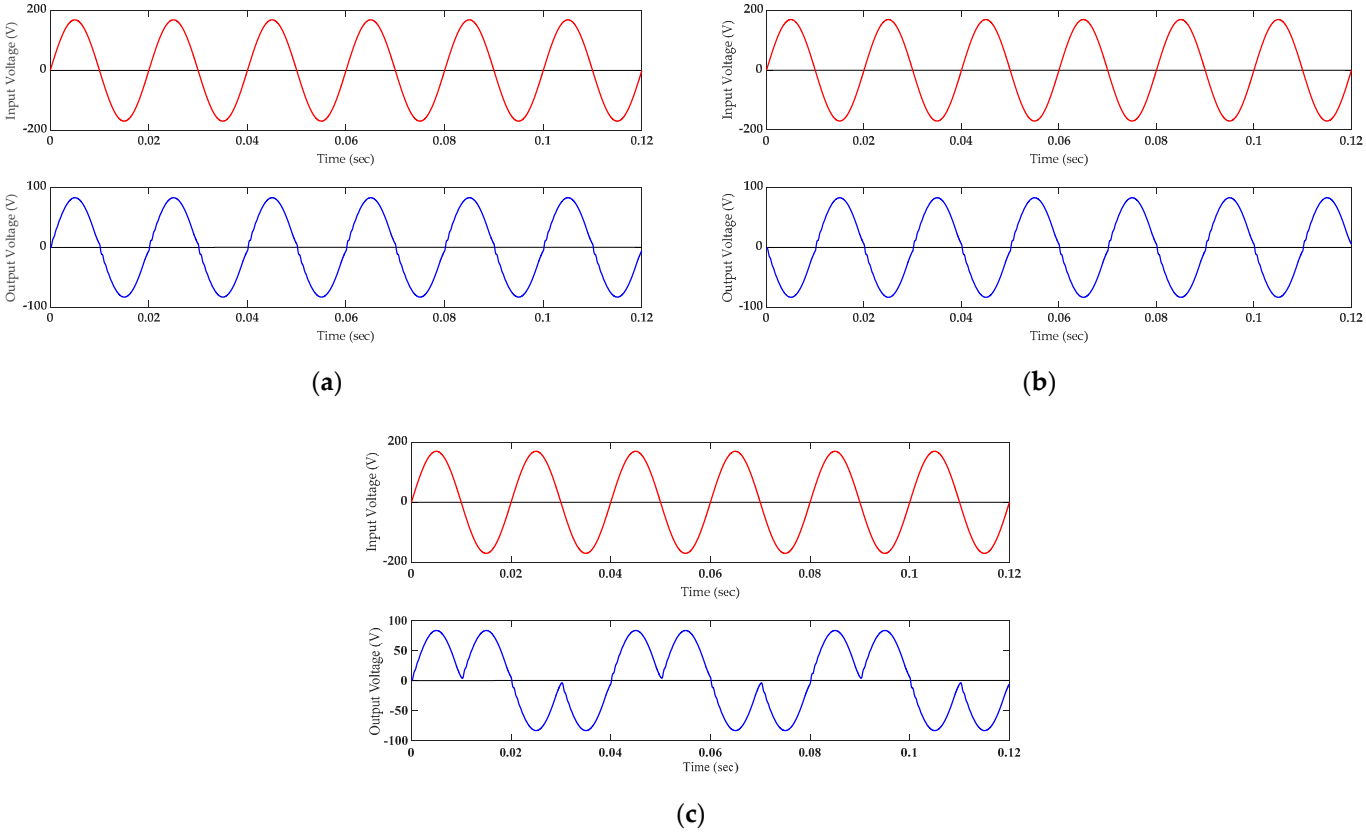


Figure 6. Simulation waveforms of output voltage (blue) with respect to input voltage (red) for the voltage gain of 0.5: (**a**) voltage in-phase form; (**b**) voltage out-of-phase form; (**c**) frequency regulation form.

4.2. Verification with Practical Results

The practically obtained results are more valuable than the simulation results because they include real-time limitations that may not be presented in the values obtained from other plate forms, such as simulation and mathematical results. The practical setup consists of eight diodes (MUR3040) with low reverse recovery times in the nanosecond range. These diodes have voltage and current ratings of 400 V and 30 A, respectively. Four high switching speed IGBTs (IXGH 40N60C2) were used as active switching transistors to operate at 20 kHz to 25 kHz switching frequency successfully. These transistors have voltage and current up to 500 V and 75 A, respectively. There are four operating transistors, of which two operate at low frequencies, and their reference point is not at ground voltage level (floating). In contrast, the reference terminals of the high-frequency switching transistors are connected to the ground voltage level. Therefore, the difficulty level of the low and high-frequency operating devices is not the same. This issue was tackled by using four similar gate drive circuits realized with four hybrid chips (EXB840) to avoid any possible miss operation of any transistor, whether it is a low or high-frequency operating transistor. A load of 150 Ω impedance was selected for the safe operation of the converters. An inductor of 1 mH was used in series with the load to store the energy from input and deliver to load in the on and off PWM intervals, respectively. Two capacitors, 2.2 µF and 4.7 µF, were connected across the input and output terminals to ensure and maintain the power quality parameters within an acceptable range. These values are designed in Section 2.3 by following the design procedure stated in [24]. The plots of Figure 7a,b represent the non-inverted and inverted forms of the output voltage. The maximum value of the voltage at the output is nearly 50 V with a given peak of input voltage of 170 V. The generation of the control signals may be produced from a microcontroller (STM controller or Arduino controller) or microprocessor. The voltage bipolar behavior of the output is also validated in Figure 7c, where the output frequency was adjusted to one-half of the input frequency. It is clear from the observation of

this figure that the first and fourth pulses are in-phase with the line voltage, but the second and third pulses are out of phase. This pair of pulses means first–forth and second–third show input voltage conversion into non-inverting and inverting forms. In Figure 7, the peak value of the output voltage was kept at less than half the value of the maximum input voltage. The plots of Figure 8a–c explore the similar behavior as represented in Figure 7, except that the peak value of all output pulses, which are approximately 100 V, is greater than half of the maximum value of the source voltage. It was confirmed from the plotting of these all waveforms that the magnitude or rms value of the output voltage can be adjusted between the zero and maximum output voltage. This is ensured with high-frequency switching, but its effect is not reflected on the output side as there is the use of a series inductor and parallel capacitor across the output terminal. The output frequency can also be changed to some selected output frequencies.

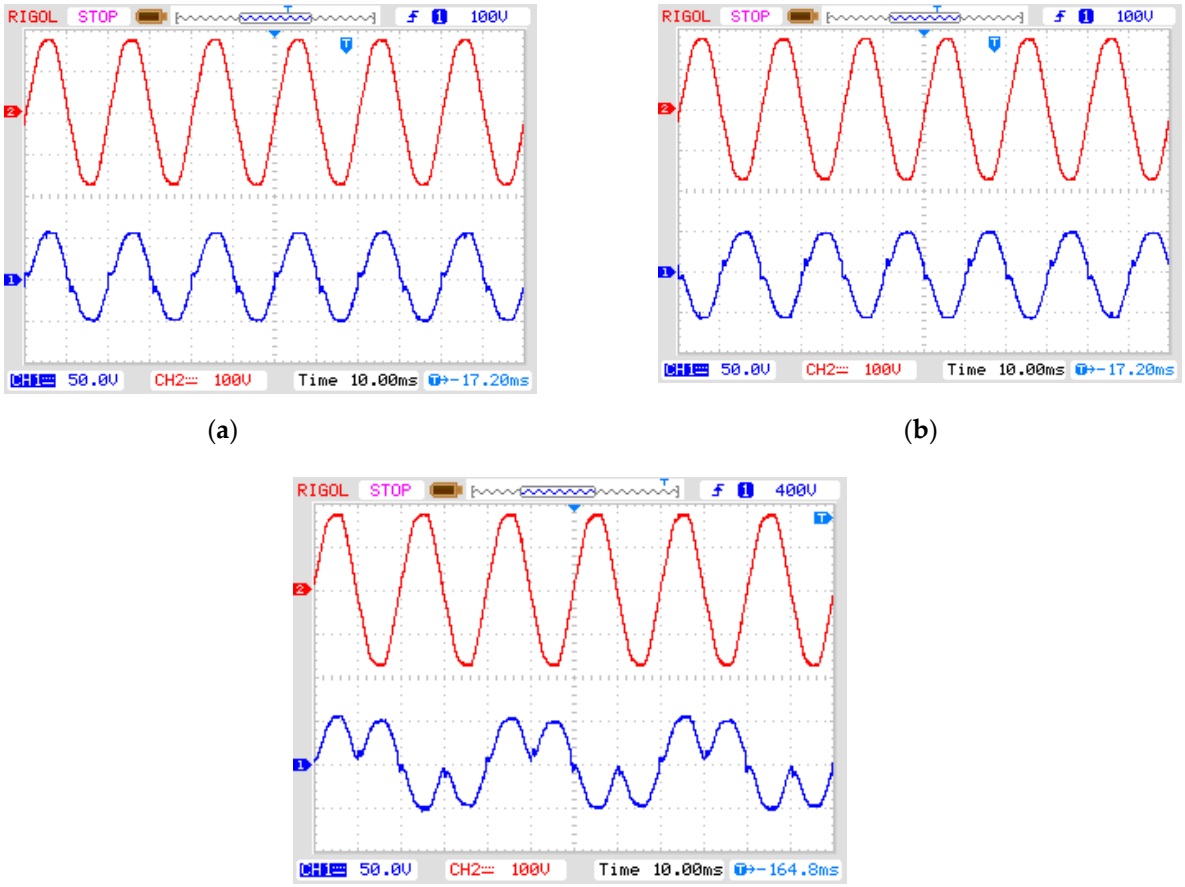


Figure 7. Recording of output waveforms (blue) with respect to input voltage (red) with a voltage gain of 0.3: (**a**) voltage in-phase form; (**b**) voltage out-of-phase form; (**c**) frequency regulation form.

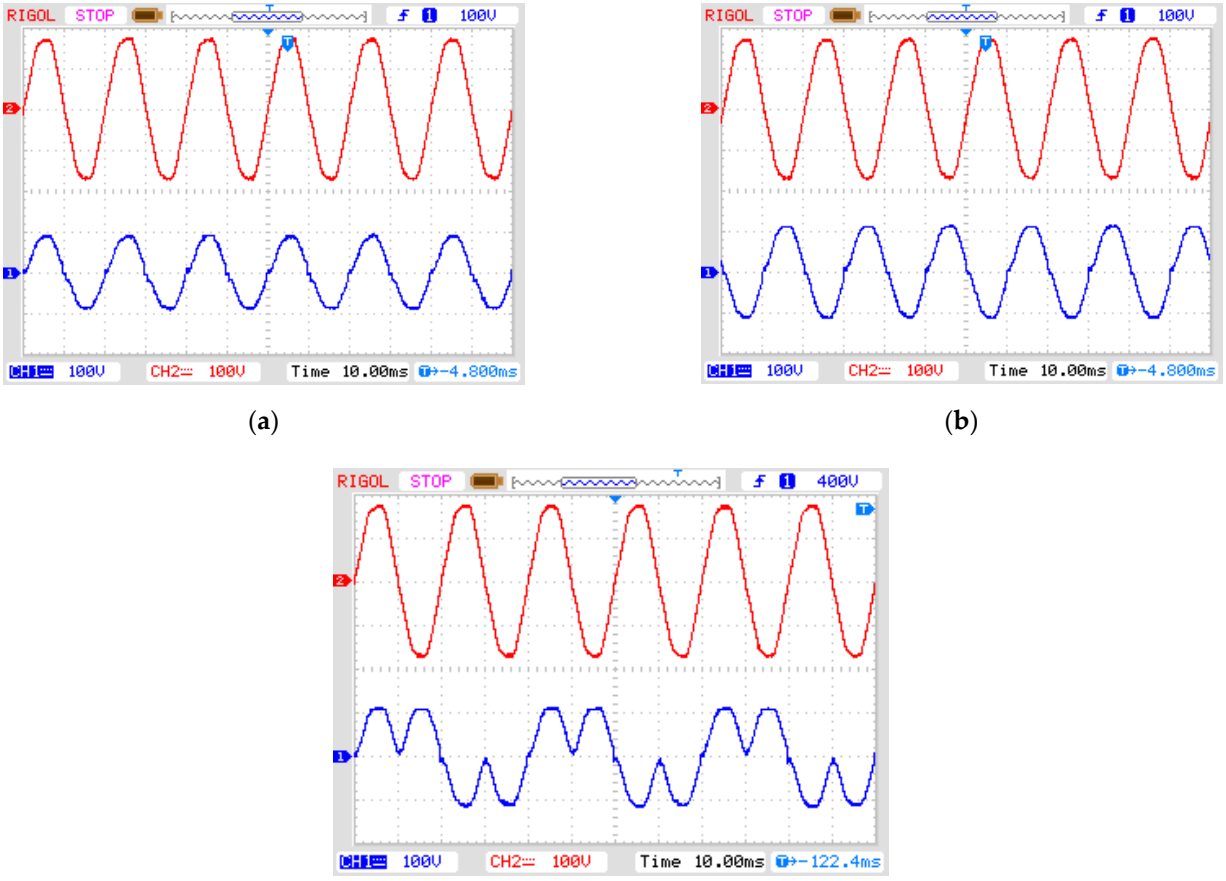


Figure 8. Recording of output waveforms (blue) with respect to input voltage (red) with a voltage gain of 0.6: (**a**) voltage in-phase form; (**b**) voltage out-of-phase form; (**c**) frequency regulation form.

5. A Case Study—Application as a Grid Voltage Compensator

As already remarked, the basic requirement of the proposed converter is to obtain the bipolar voltage gain outputs with voltage step-down characteristics. The converter with these capabilities can be employed in many applications, for example, grid voltage compensation during the voltage sag or swell problem that requires the non-inverted and inverted outputs for their compensation, respectively. The primary roots of these problems are line faults, especially line-to-ground faults. Voltage sag with a depth level of less than 50% is one of the most occurring problems reported in [25]. Here, a voltage sag compensation approach-based interphase mechanism was developed. This approach was based on the series connection of dynamic voltage compensators in each phase of the three-phase system. Each dynamic voltage compensator consists of two bipolar voltage controllers, and their inputs are connected to the non-faulty phases. Two-line frequency transformers were used to interconnect the outputs of the two AC voltage controllers. The output windings of these two transformers were connected in series to obtain the compensating voltage. The phase alignment of this voltage with the voltage of the faulty phase is one of the big issues with this approach. There is no such problem in the second voltage compensating approach, where the dynamic voltage restorer is connected in the same phase in which voltage correction is required. This arrangement is shown in Figure 9.

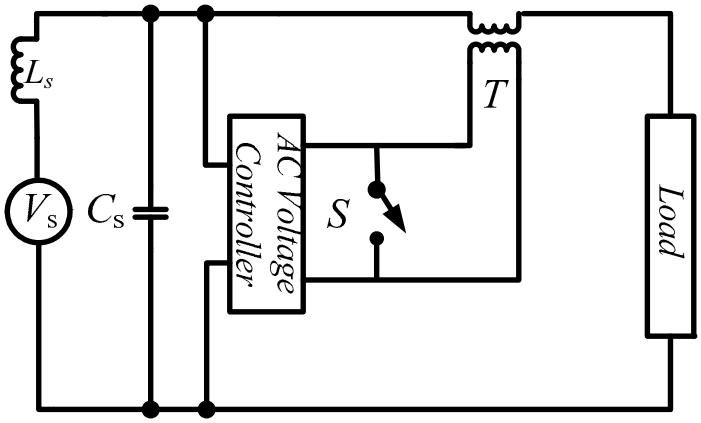


Figure 9. Test circuit for the voltage compensation process.

In this system, the switch (*S*) connected to the output of the AC voltage controller normally remains closed, and in this case, no voltage is injected into the line. It only opens once the voltage correction in the line is required, and this process is initiated upon the detection of the problem. Here, the line frequency transformer (*T*) facilities the injection of the compensating voltage. The detailed process of Figure 9 is outlined in the form of the block diagram presented in Figure 10.

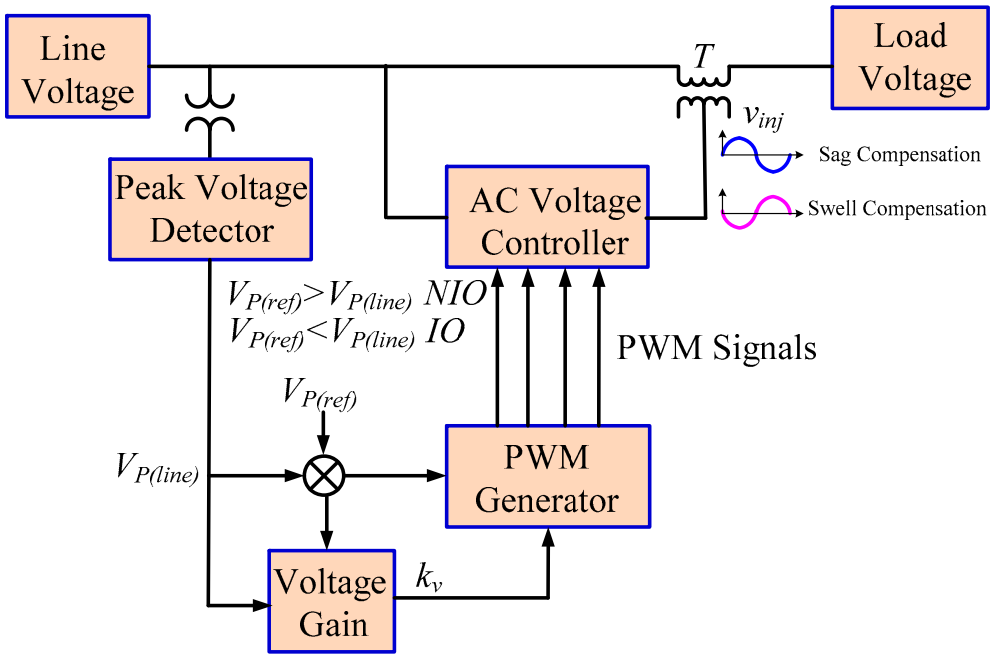


Figure 10. Block diagram of the voltage compensation process.

The detection of the problem with the depth level was carried out by comparing the line peak voltage ($V_{p(line)}$) with the peak value of the reference voltage ($V_{p(ref)}$). The peak line voltage was obtained with the help of the peak voltage detector. If the line voltage is less than the reference voltage, it indicates a voltage sag problem in the line, and the AC voltage controller has to produce the non-inverted output (*NIO*) to compensate for the problem. On the other hand, if the line voltage is greater than the reference voltage, then there is a problem of voltage swell, and the AC voltage controller has to produce the inverted output (*IO*) to tackle this issue. The magnitude adjustment of the compensating voltage that is available at the input of the series connected transformer is somehow critical as the change in the load voltage is also reflected in the input voltage of the AC voltage

controller, which means if load voltage is reduced, then input voltage of the converter is also reduced and vice versa. In order to address this problem, the required voltage gain was computed with the information of line and reference voltage as.

$$k_v = \frac{\left|V_{p(ref)} - V_{p(line)}\right|}{V_{p(line)}} \tag{22}$$

The simulated outputs of the voltage compensating system in Figure 10 are shown in Figure 11a,b for the correction of the line voltage during the voltage sag and swell issues, respectively, with a depth level of 20%. Here, as an example, the required load voltage was 100 V peak. Therefore, the peak value of the reference voltage was set to 100 V. If there is a problem with a voltage sag with a depth level of 20%, then the line or load voltage is reduced to 80 V. In this situation, the required peak value of the injecting voltage is 20 V, which has to be produced by the AC voltage controller in non-inverting mode from 80 V peak input. For this purpose, the required voltage gain is 0.25, which generates a 20 V peak non-inverted output, as may be observed from Figure 11a. If there is a voltage swell issue with a similar depth level, then line peak voltage is increased to 120 V. Once again, AC voltage has to produce a 20 V peak output with voltage inverted form. The voltage gain for this output is 0.1667, as the input voltage of the converter is now 120 V. These values of the voltage gain are also confirmed from the calculation of Equation (22).

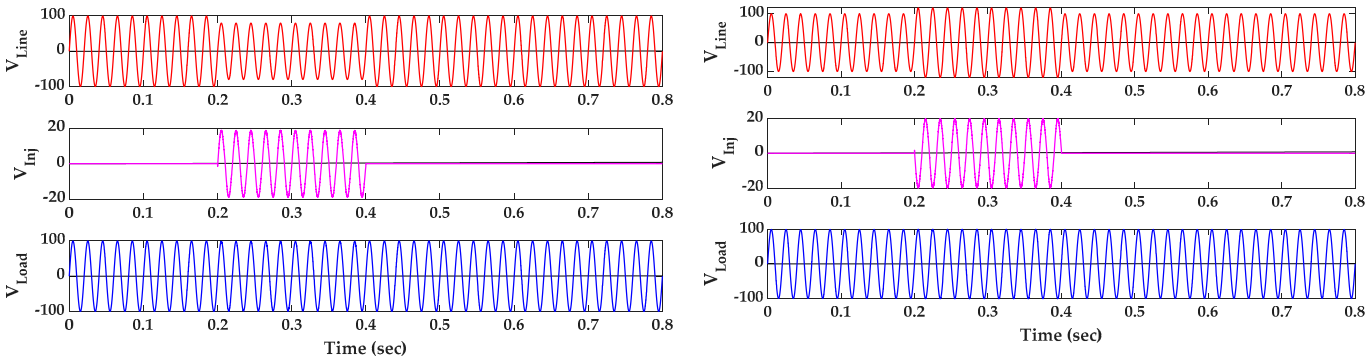


Figure 11. Grid voltage compensation during the problem of (**a**) voltage sag and (**b**) voltage swell.

It was concluded that any voltage change in the grid or line voltage might be corrected with the compensating voltage generated by the AC voltage controller that can deliver non-inverted and inverted outputs with the required voltage gain. For the correction of the line or grid voltage for voltage sag and swell issues, the converter's output voltages have to be added and subtracted from the line with the help of a series connected transformer.

The flow chart in Figure 12 also facilitates obtaining a quick review of the line voltage correction process.

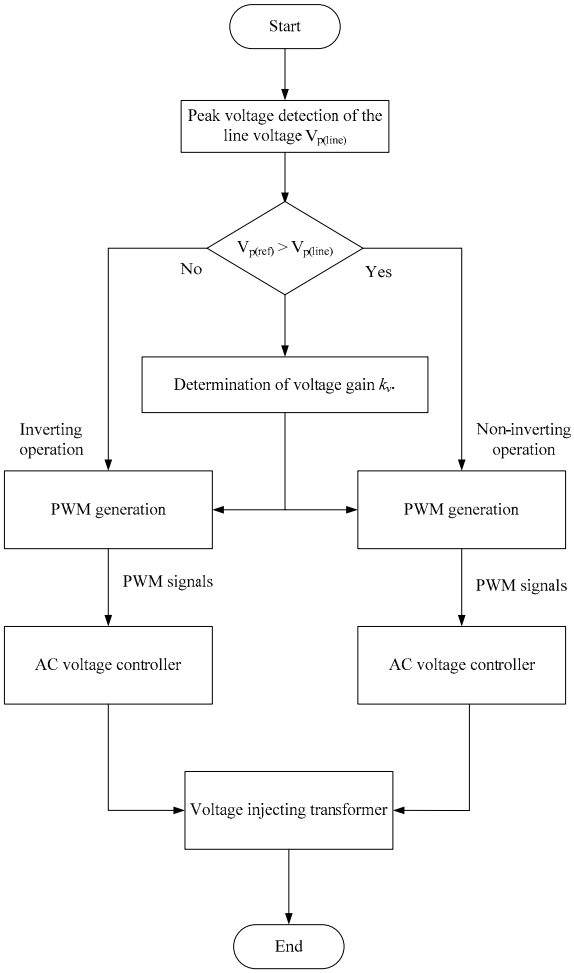


Figure 12. Flow chart of voltage correcting system.

6. Conclusions

A compact-sized direct AC–AC converter was introduced in this research article. It has a symmetric bipolar voltage gain with a buck feature that has the ability to govern the value of the output voltage from zero volts to the maximum value of the input voltage. These characteristics increase its potency to use in grid voltage correction during the problems of voltage sag and swell. It can also be effectively employed in AC drive systems as a step-down frequency controller that may be developed for a heavy-duty load such as grinding or steel rolling mills. It can avoid the problem of core saturation as there is a possibility to control both the voltage and frequency. The frequency of the output voltage can be changed by controlling the time periods of the low-frequency operating transistor, and the adjustment in the output voltage is possible with the PWM control of the high-frequency operating transistors. The circuit and control topology is very simple, and there is the use of only four fully controlled solid-state devices. This feature drastically reduces the size, coat, and conversion losses. The operation of voltage and frequency control was detailed with the help of an equivalent circuit and switching strategy. The validation of the developed topology was carried out by comparing its performance parameters with those of the existing converters. Further justification of the developed converter was proved from simulation, and practical results were gained for voltage and frequency control. In future work, a feedback controller can be introduced into the loop to compensate for the perturbations in the line voltage or load current to keep the output voltage regulated. This way, an overall loop frequency response can also be carried out.

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