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A New SEPIC-Based DC-DC Converter with Coupled Inductors Suitable for High Step-Up Applications

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Abstract: In this paper, a new hybrid SEPIC dc-dc converter with coupled inductors suitable for photovoltaic applications is presented. First, the way how the new topology was derived will be presented, continuing with its analysis and design equation as a standalone dc-dc topology. The analysis will consist of a steady-state equations derivation, a static conversion ratio calculation based on which the semiconductor voltage and current stresses are evaluated, leading to the continuous conduction mode (CCM) operation conditions. The converter will then be simulated as a first validation of the theory using the dedicated Caspoc power electronics package. To finally validate the theoretical design, a prototype will be built in order to practically demonstrate the feasibility of the proposed solution and to reveal its main practical features and limitations. A comparative study to several other similar topologies will be carried out to identify its most desirable features. Finally, an application of the new hybrid converter will consist of a complete solar energy conversion system using a photovoltaic panel. The maximum power point tracking (MPPT) algorithm will be elaborated. The solar system together with the MPPT will first be modeled, then simulated and practically implemented and tested.

Keywords: SEPIC converter; steady-state analysis; static conversion ratio; photovoltaic system

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1. Introduction

The European Union (EU) expects greenhouse gas emissions to be eliminated by 2050 and 100% replaced by renewable energy sources [1–3]. Solar energy is considered to be the largest source of energy [3]. In this context, solar energy technologies have experienced an increase in research to offer better efficiency at a lower cost. In order to achieve these goals, power electronics also deals with the conversion and storage of solar energy, the development of algorithms and control methods, etc. Dc-dc converters play an important role in the conversion systems of photovoltaic panels (PV). In the literature, several solutions are proposed depending on the type of conversion that is required [4–60]. If the output voltage is required to be higher than the input voltage, a step-up converter needs to be used. The classical Boost topology is the simplest step-up converter with the lowest number of components [13]. One disadvantage of this converter is that if the required output voltage is much higher than the input voltage, this type of conversion cannot be achieved because of the intrinsic non-ideal components losses. However, on the market, different solutions, beginning with non-isolated high step-up dc-dc converters like: cascaded converters [14–17], semiquadratic converters [18], quadratic converters [19–21], stacked step-up converters [22,23], hybrid converters [24–27], multi-input converters [28], multiphase converters [17,29] and ending with isolated step-up topologies [30] have been reported.

If a step-down converter is required, one of the solutions could be the traditional Buck converter [13]. If an extremely low conversion ratio is required, it cannot be obtained with the classical Buck converter, but different converters have been proposed in the

literature, such as cascaded [31,32], quadratic [33], multiphase [34] or hybrid step-down converters [24–27], etc.

In this paper, a new SEPIC-based step-down/step-up converter is presented, and it is compared to other types of step-down/step-up topologies. Similar to the classical Buck and Boost converters, the Buck-Boost converter has the advantage of having the lowest number of components among the step-down/step-up topologies [13]. The disadvantage of this converter is the control, which is difficult because the transistor is floating, and the output voltage polarity is opposite to that of the input voltage. In the literature, different Buck-Boost-type topologies can be found, beginning with a buck-boost converter with positive output voltage, presented in [35], a bidirectional buck-boost converter [36–38], cascaded [39], quadratic [40] or multi-input converters [41,42], etc. Also, the classical Ćuk, SEPIC and ZETA converters [13,61] are of step-up/step-down nature.

The classical transformerless SEPIC converter has the advantage that the output voltage has the same polarity as the input voltage [13]. The authors in [24–27] are using a switched capacitor or switched inductor structure that it is inserted into the traditional SEPIC topology for increasing the step-up or step-down capabilities. In reference [43], it is shown that a quadratic SEPIC converter can be used in microgrid applications to obtain a high-voltage gain at a low-duty cycle and it exhibits a continuous input current, like in the classical transformerless SEPIC. Another structure with a reduced input current ripple and higher step-up capabilities is presented in [44]. In [45–60], different structures of nonisolated SEPIC converters with some examples of design, analysis and control are presented. In [61], the classical SEPIC with isolation is presented, analyzed, and implemented.

The new SEPIC-based converter introduced in this paper employs coupled inductors and exhibits a static conversion ratio that is higher than the classical one. In Section 2, the development of the novel proposed converter and the dc analysis are presented. The theoretical waveforms, the peak-to-peak ripples, the semiconductor current and voltage stresses, the CCM operation conditions and the theoretical comparative study to other step-down/step-up topologies are presented in Section 3. The next section provides a design example. The simulation and the experimental results developed are presented in Section 5. In Section 6, the suitability and feasibility of the proposed SEPIC converter in a photovoltaic application is proven. The perturb and observe (P&O) method will be implemented as a MPPT algorithm, and the whole PV system will be validated by both simulations and experiments. The last section is dedicated to some discussions.

2. Steady State Analysis of the Proposed Hybrid SEPIC-Based Converter with Coupled Inductors

In [24], Prof. Ioinovici et al. proposed a new hybrid SEPIC converter with a switching Up 3 structure. The architecture of this topology was analyzed in [24,62] and is presented in Figure 1.

Figure 1. SEPIC hybrid converter with a switching Up 3 structure presented in [24].

The idea of developing the novel converter proposed in this paper started by coupling the inductors L_1 and L_2 . The authors also used this technique in other published research [63–66]. The coupling is assumed to be ideal and the numbers of turns corresponding to L_1 and L_2 are denoted as N_1 and N_2 respectively. The transformer ratio n defined as:

$$n = \frac{N_2}{N_1} \quad (1)$$

can be higher, lower, or equal to unity.

In this paper, the case when the transformer ratio is assumed to be lower than unity will be analyzed. It can be shown that, in this situation, diode D_3 is always off and therefore it can be removed from the circuit. Taking this into account, the proposed topology is presented in Figure 2. It is obvious that it is simpler and cheaper than the previous one because one magnetic core and one diode are eliminated. The novel converter obtained consists of one active switch, three passive switches, an individual inductor, and a pair of coupled inductors, combined with one internal and one output capacitor.

Figure 2. The proposed hybrid SEPIC-based converter with coupled inductors.

In order to analyze the converter, all components are assumed to be ideal. Because the inductors are perfectly coupled, they will be modelled by an ideal transformer (IT) that has the transformer ratio n , together with a magnetizing inductor, L_M , equal to L_1 . In Figure 3, the equivalent schematic is presented, and all the analyses will be developed on it considering the CCM operation. Noncapital letters will denote instantaneous variables, and capital letters will specify dc values or maximum values.

Figure 3. Equivalent schematic of the proposed hybrid SEPIC-based dc-dc converter with coupled inductors.

Considering the notations used in Figure 3, the ideal transformer equations are:

$$v_2 = n \times v_1 \quad (2)$$

By solving Equations (4) and (5), the dc voltages across the internal capacitor, V_{C1} , and across the output capacitor, V_{C2} , are found as:

$$V_{C1} = \frac{n+D}{n} \times V_g \quad (6)$$

$$V_{C2} = \frac{D}{1-D} \times \frac{n+D}{n} \times V_g \quad (7)$$

Because $V_o = V_{C2}$, the ideal static conversion ratio can be obtained from (7):

$$M = \frac{D}{1-D} \times \frac{n+D}{n} \quad (8)$$

The next step is to invoke the charge balance principle to calculate the dc magnetizing inductor current, I_{LM} , and the dc output inductor current, I_{L3} :

$$D \times (-I_{L3}) + (1-D) \times \left(\frac{I_{LM}}{1+n} \right) = 0 \quad (9)$$

$$D \times \left(-\frac{V_{C2}}{R} \right) + (1-D) \times \left(\frac{I_{LM}}{1+n} + I_{L3} - \frac{V_{C2}}{R} \right) = 0 \quad (10)$$

From (9) and (10), it follows that:

$$I_{LM} = \frac{D^2}{(1-D)^2} \times \frac{(n+D) \times (1+n)}{n} \times \frac{V_g}{R} \quad (11)$$

$$I_{L3} = \frac{D}{1-D} \times \frac{n+D}{n} \times \frac{V_g}{R} \quad (12)$$

3. Semiconductor Stresses and AC Analysis of the Proposed SEPIC-Based Converter

3.1. Semiconductor Stresses and Ripples Calculation

From the analysis carried out in the previous section, the semiconductor stresses are determined, neglecting the capacitor voltage ripples. These semiconductor stresses are also needed for the converter design.

The maximum voltage across switch S is obtained from the second topological state, while the dc transistor current stress can be found from the first topological state. The voltage across switch S is equal to the sum of the internal capacitor voltage, V_{C1} , and the output capacitor voltage, V_{C2} . By replacing V_{C1} and V_{C2} from (6) and (7), the transistor voltage stress is:

$$V_S = \frac{n+D}{n \times (1-D)} \times V_g \quad (13)$$

The current flowing through the transistor is the sum between i_{LM}/n and i_{L3} . Hence, the dc transistor current stress is: $D \times \left(\frac{I_{LM}}{n} + I_{L3} \right)$. By replacing I_{LM} and I_{L3} from (11) and (12), the transistor current stress is:

$$I_S = \frac{D^2 \times (n+D)^2}{n^2 \times (1-D)^2} \times \frac{V_g}{R} \quad (14)$$

The voltage stress for diode D_1 can be found from the second topological state being equal to $\frac{V_g - V_{C1} - V_{C2}}{1+n}$. Using (6) and (7), it results that:

$$V_{D1} = \frac{D}{n \times (1-D)} \times V_g \quad (15)$$

The current through diode D_1 is equal to i_{LM}/n , and therefore the dc current through D_1 is $D \times \frac{I_{LM}}{n}$. With I_{LM} given by (11), one obtains:

$$I_{D1} = \frac{D^3 \times (n + D) \times (1 + n)}{n^2 \times (1 - D)^2} \times \frac{V_g}{R} \quad (16)$$

Similarly, the voltage stress across diode D_2 is obtained from the first topological state, while from the second topological state, the dc current through diode D_2 results as:

$$V_{D2} = \frac{V_g}{n} \quad (17)$$

$$I_{D2} = (1 - D) \times \frac{I_{LM}}{1 + n} = \frac{D^2 \times (n + D)}{n \times (1 - D)} \times \frac{V_g}{R} \quad (18)$$

The voltage stress across D_4 is the sum between V_{C1} and V_{C2} . Using (6) and (7) it immediately follows that:

$$V_{D4} = \frac{n + D}{n \times (1 - D)} \times V_g \quad (19)$$

As D_4 conducts the sum of the currents $\frac{i_{LM}}{1+n} + i_{L3}$ in the second topological state, taking (11) and (12) into account, the dc D_4 current is found as:

$$I_{D4} = (1 - D) \times \left(\frac{I_{LM}}{1 + n} + I_{L3} \right) = \frac{D \times (n + D)}{n \times (1 - D)} \times \frac{V_g}{R} \quad (20)$$

Peak-to-peak inductor currents and capacitor voltages ripples are also invoked in the design equations and in the CCM operation conditions.

The magnetizing peak-to-peak current ripple can be written as:

$$\Delta I_{LM} = \frac{D \times V_g}{n \times L_M \times f_s} \quad (21)$$

The peak-to-peak current ripple for the inductor L_3 is given by:

$$\Delta I_{L3} = \frac{D \times (n + D) \times V_g}{n \times L_3 \times f_s} \quad (22)$$

For the internal capacitor C_1 , the peak-to-peak voltage ripple is expressed as:

$$\Delta V_{C1} = \frac{D^2 \times (n + D)}{n \times (1 - D)} \times \frac{V_g}{R \times C_1 \times f_s} \quad (23)$$

The output capacitor peak-to-peak voltage ripple is:

$$\Delta V_{C2} = \frac{D^2 \times (n + D)}{n \times (1 - D)} \times \frac{V_g}{R \times C_2 \times f_s} \quad (24)$$

According to the CCM operation condition, it is necessary that the diodes be on during the whole topological state during which they are planned to conduct. This imposes the condition that the minimum diode current has to remain positive during the corresponding topological state. Taking into account that the converter includes three diodes, this will result in three CCM conditions. As the currents through D_1 and D_2 are equal to $\frac{I_{LM}}{n}$ and $\frac{I_{LM}}{1+n}$ respectively, for these diodes, the CCM condition is the same. In this case, the general condition will be:

$$I_{LMmin} = I_{LM} - \frac{1}{2} \Delta I_{LM} \geq 0 \quad (25)$$

By replacing I_{LM} and ΔI_{LM} from (11) and (21), after some simple algebra the final condition is:

$$\frac{2 \times L_M \times f_s}{R} \geq \frac{(1-D)^2}{D \times (n+D) \times (1+n)} \quad (26)$$

The current flowing through D_4 is $\frac{i_{LM}}{1+n} + i_{L3}$, and i_{LM} while i_{L3} have the same monotonicity. Therefore, the condition is $\frac{I_{LMmin}}{1+n} + I_{L3min} > 0$, where $I_{LMmin} = I_{LM} - \frac{1}{2}\Delta I_{LM}$ and $I_{L3min} = I_{L3} - \frac{1}{2}\Delta I_{L3}$. Replacing the I_{LM} , I_{L3} , ΔI_{LM} and ΔI_{L3} with their formulae from (11), (12), (21) and (22), the CCM condition for diode D_4 becomes:

$$\frac{2 \times L_e \times f_s}{R} \geq \frac{(1-D)^2}{n+D} \quad (27)$$

where the equivalent inductor L_e is:

$$L_e = (L_M \times (n+D)) \parallel \frac{L_3}{1+n} \quad (28)$$

3.2. Steady State Theoretical Waveforms

The theoretical waveforms associated to the converter are presented in Figures 5 and 6.

Figure 5. Main waveforms associated to the passive components of the proposed converter.

Figure 6. Main waveforms associated to the semiconductor devices.

The magnetizing inductor voltage v_{LM} is piecewise constant, exhibiting a rectangular shape, while the magnetizing inductor current i_{LM} is piecewise linear, increasing until $D \cdot T_s$, because v_{LM} is positive in the first topological state and decreasing in the second topological state, when the voltage is negative. Similarly, the same theoretical waveforms are associated for inductor voltage v_{L3} and inductor current i_{L3} . Internal capacitor current i_{C1} and output capacitor current i_{C2} are piecewise constant, resulting in a piecewise linear internal capacitor voltage, v_{C1} , and output capacitor voltage, v_{C2} . The semiconductor waveforms, depicted in Figure 6, result from taking into account that, when “ON”, the semiconductor currents are linear combinations of inductor currents and the same is true for semiconductor voltages. These linear combinations values are also specified in Figure 6.

3.3. Comparative Study to Other Step-Down/Step-Up Topologies

Examining Equation (8), the duty cycle can be expressed in terms of the static conversion ratio and transformer ratio n as a solution of a second-degree equation:

$$D = \frac{-n \times (1 + M) \times \left(\sqrt{n^2 \times (1 + M)^2 + 4 \times n \times M} \right)}{2} \quad (29)$$

The dependency of the static conversion ratio against the duty cycle for the classical isolated SEPIC [61], the hybrid SEPIC from [24] and the proposed hybrid SEPIC-based converter is presented in Figure 7. For a better representation, a detail for a duty cycle between [0–0.5] is provided.

Figure 7. Static conversion ratio against the duty cycle for the classical isolated SEPIC, hybrid SEPIC and proposed converter with the turns ratio as a parameter.

At a first glance, the step-down and step-up allure of the proposed converter can be observed. From (29) and Figure 7, it can be observed that the proposed SEPIC converter starts to step up at a lower duty cycle value, compared to the isolated and hybrid SEPIC, or, in other words, at the same turns ratio, a higher static conversion ratio is achieved for the proposed converter at the same duty cycle, compared to the same converters. Figure 7 also reveals the fact that the lower the value of n , the more step-up is achieved, thus recommending the converter for step-up applications where a big difference between the input and output voltage is needed.

Another comparison, where the comparative parameters are the number of active and passive semiconductors, the number of cores/windings, the total number of components, the system order, the expression of the static conversion ratio M , the expression of the duty cycle D , and the current and voltage semiconductor stresses, is realized in Table 1. The comparison is made between the classical Buck-Boost, classical non-isolated SEPIC, hybrid SEPIC and proposed hybrid SEPIC converter. For a fair comparison, the converters are

supposed to be supplied by the same input voltage V_g , and to deliver the same output voltage V_o on the same load R . Consequently, the conversion ratio M and the output power P_o are the same.

Table 1. Comparison between the main parameters of different step-down/step-up converters.

Parameter	Type of Converter		
	Classical Buck-Boost [13]	Classical Nonisolated SEPIC [13]	Hybrid SEPIC [24]
Switches	1	1	1
Diodes	1	1	4
No. of cores/windings	1/1	2/2	3/3
Total no. of components	4	6	10
System order	2	4	5
Static conversion ratio- M	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D \times (1+D)}{1-D}$
Duty cycle- D	$\frac{M}{1+M}$	$\frac{M}{1+M}$	$\frac{-1-M+\sqrt{(1+M)^2+4 \times M}}{2}$
Switch current stress	$M^2 \times \frac{V_g}{R}$	$M^2 \times \frac{V_g}{R}$	$M^2 \times \frac{V_g}{R}$
Switch voltage stress	$(1+M) \times V_g$	$(1+M) \times V_g$	$\frac{2 \times M}{-1-M+\sqrt{(1+M)^2+4 \times M}} \times V_g$
Maximum diode dc current stress	$M^2 \times \frac{V_g}{R}$	$M^2 \times \frac{V_g}{R}$	$M \times \frac{V_g}{R}$
Maximum diode voltage stress	$(1+M) \times V_g$	$(1+M) \times V_g$	$\frac{-1-M+\sqrt{(1+M)^2+4 \times M}}{3+M-\sqrt{(1+M)^2+4 \times M}} \times V_g$
Parameter	Type of Converter		
	Proposed Hybrid SEPIC		
Switches	1		
Diodes	3		
No. of cores/windings	2/3		
Total no. of components	8		
System order	4		
Static conversion ratio- M	$\frac{D}{(1-D)} \times \frac{n+D}{n}$		
Duty cycle- D	$\frac{-n \times (1+M)+\sqrt{n^2 \times (1+M)^2+4 \times n \times M}}{2}$		
Switch current stress	$M^2 \times \frac{V_g}{R}$		
Switch voltage stress	$\frac{2 \times M}{-n \times (1+M)+\sqrt{n^2 \times (1+M)^2+4 \times n \times M}} \times V_g$		
Maximum diode dc current stress	$\frac{(1+n) \times \left[n^2 \times (1+M)^2+2 \times n \times M-n \times (1+M) \times \sqrt{n^2 \times (1+M)^2+4 \times n \times M} \right]}{n \times \left[2+n \times (1+M)-\sqrt{n^2 \times (1+M)^2+4 \times n \times M} \right]} \times M \times \frac{V_g}{R}$		
Maximum diode voltage stress	$\frac{2 \times M}{-n \times (1+M)+\sqrt{n^2 \times (1+M)^2+4 \times n \times M}} \times V_g$		

Analyzing the results from Table 1, it can be remarked that each topology has only one transistor. The proposed SEPIC-based converter has two additional diodes, in comparison to the classical Buck-Boost or SEPIC converter, and one diode less if it is compared to the hybrid SEPIC from [24]. The lowest system order is the classical Buck-Boost, followed by the classical SEPIC and the proposed SEPIC. From Table 1, it can be seen that the static conversion ratio for the proposed SEPIC topology is $(1 + D/n)$ times higher than the

classical SEPIC, or Buck-Boost converter. Therefore, in the step-up region, a wide static conversion ratio is achieved at a moderate duty cycle, and this can be observed also from the dependency of the static conversion ratios against the duty cycle for the proposed converter, for the classical and the hybrid SEPIC converters presented in Figure 7.

4. Design Example for the Proposed Converter

In the design example, the converter is used in a PV system and, therefore, the requirements for the proposed SEPIC-based converter depend on the PV panel characteristics. Two PV modules MWG-20 will be used for the experiments. The PV modules will be connected in series, in order to increase the input voltage. In standard test conditions (STC) for a solar irradiance $G = 1000 \text{ W/m}^2$ and temperature $T = 25^\circ\text{C}$, one PV module has the following parameters:

Peak power: $P_{max} = 20 \text{ W}$

Maximum power point current: $I_{mp} = 1.14 \text{ A}$

Maximum power point voltage: $V_{mp} = 17.49 \text{ V}$

Short circuit current: $I_{sc} = 1.22 \text{ A}$

Open circuit voltage: $V_{oc} = 21.67 \text{ V}$

The converter was designed according to the following parameters:

Input voltage range was between: $V_g = 30 \div 35 \text{ V}$ – correlated to V_{mp}

Maximum output power: $P_o = 40 \text{ W}$

Switching frequency: $f_s = 100 \text{ kHz}$

Output voltage: $V_o = 120 \text{ V}$

Output voltage peak-to-peak ripple: $\Delta V_{C2} = 300 \text{ mV}$

Transformer ratio: $n = 0.5$

The minimum and maximum static conversion ratios are obtained from Equation (8):

$$M_{min} = \frac{V_o}{V_{gmax}} = 3.42 \quad (30)$$

$$M_{max} = \frac{V_o}{V_{gmin}} = 4 \quad (31)$$

The necessary duty cycle range can be calculated using (29) and will result in $D \in [0.6070, 0.6375]$.

The value for the load resistor is given by:

$$R = \frac{V_o^2}{P_o} = 360 \Omega \quad (32)$$

Imposing the peak-to-peak magnetizing inductor current ripple given by (21) not to exceed 25% of the dc magnetizing inductor current value (11), the magnetizing inductor can be calculated. The condition will be:

$$\Delta I_{LM} \leq \frac{1}{4} \times I_{LM} \quad (33)$$

From Equations (33), (21) and (11) the minimum magnetizing inductor formula can be found:

$$L_M \geq \frac{4 \times (1 - D)^2 \times R}{D \times (n + D) \times (1 + n) \times f_s} \quad (34)$$

In a similar way, the condition for L_3 inductor current will look like:

$$\Delta I_{L3} \leq \frac{1}{4} \times I_{L3} \quad (35)$$

and from (35), (22), and (12) the minimum inductor L_3 value can be found as follows:

$$L_3 \geq \frac{4 \times (1 - D) \times R}{f_s} \quad (36)$$

The equations for the inner and output capacitors are designed imposing that the voltage ripple across the inner capacitor be less than ten percent of its dc value and for the output capacitor to ensure an output voltage ripple less than the value imposed by the specifications.

Using (6) and (23) the minimum required value for the internal capacitor, and from (7) and (24) the minimum required value for the output capacitor can be calculated:

$$C_1 \geq \frac{10 \times D^2}{(1 - D) \times R \times f_s} \quad (37)$$

$$C_2 \geq \frac{D^2 \times (n + D) \times V_g}{n \times (1 - D) \times R \cdot f_s \times \Delta V_{C2}} \quad (38)$$

The minimum value of the magnetizing inductor L_M calculated with Equation (35) will be equal to the value of inductor L_1 , $L_M = L_1 = 1.7$ mH. The value for L_2 is determined using $L_2 = n^2 \cdot L_M$, so $L_2 = 425$ μ H. The minimum inductor value L_3 , calculated from (36) is $L_{3min} = 5200$ μ H. The minimum value of the inner capacitor was obtained from (37) and that for the output capacitor from (38), and they are $C_{1min} = 0.26$ μ F and $C_{2min} = 6.72$ μ F. The inductors were manufactured in the laboratory with the following values: $L_1 = 2$ mH, $L_2 = 503$ μ H and $L_3 = 5900$ μ H. Taking into account the practical values obtained in the laboratory for L_1 and L_2 , the transformer ratio n resulted as $n = 0.5014$. For the capacitors, the following standard values were chosen: $C_1 = 0.33$ μ F and $C_2 = 10$ μ F.

The transistor voltage stress can be calculated from (13), and it is $V_S = 197$ V. According to (14), its average current will be $I_S = 1.33$ A. The voltage and current stresses associated to diode D_1 can be calculated from (15) and (16), respectively, resulting in: $V_{D1} = 108$ V and $I_{D1} = 1.12$ A. The smallest voltage and current stresses are related to the diode D_2 : $V_{D2} = 70$ V and $I_{D2} = 0.21$ A, calculated from (17) and (18). The value of the voltage stress on diode D_4 is equal to the voltage stress of the transistor, $V_{D4} = 197$ V. From (20) diode D_4 current stress is $I_{D4} = 0.33$ A.

5. Simulations and Experimental Results

5.1. Simulation Results

A simulation of the ideal SEPIC-based dc-dc converter with coupled inductors was performed using Caspoc software [67]. This simulation was realized as a first validation of the theoretical considerations. The values of the components are the same as those from the design example. The simulation is made in an operating point, considering the input voltage $V_g = 30$ V, the static conversion $M = 4$. For these values, the duty cycle is $D = 0.6375$.

The dc output voltage, V_o , predicted by the simulation was 120 V, as Figure 8 reveals, exactly as theoretically calculated with (7). In Figure 9, the magnetizing inductor current is presented, confirming its triangular shape, obtained in Caspoc with the help of the mathematical blocks. For inductor L_1 , the first part of the triangular shape of the magnetizing current can be seen in Figure 10. The second part of the triangular shape of the magnetizing current can be seen in Figure 11, as the inductor L_2 current. The voltage and current for inductor L_3 are presented in Figure 12. The correct CCM operation of the converter is proven by the voltages and currents for the coupled inductors L_1 and L_2 , and inductor L_3 . The voltage and current for the inner capacitor are presented in Figure 13 and, for the output capacitor, are depicted Figure 14. In Figures 15–18, the voltage and current for the transistor and diodes are presented.

Figure 8. Output dc voltage.

Figure 9. Magnetizing inductor current i_{LM} .

Figure 10. Voltage (blue) and current (red) of the primary winding L_1 .

Figure 11. Voltage (blue) and current (red) of the secondary winding L_2 .

Figure 12. Voltage (blue) and current (red) for the inductor L_3 .

Figure 13. Voltage and current for the internal capacitor C_1 .

Figure 14. Voltage and current for the output capacitor C_2 .

Figure 15. Voltage and current corresponding to the transistor S .

Figure 16. Voltage and current corresponding to the diode D_1 .

Figure 17. Voltage and current corresponding to the diode D_2 .

Figure 18. Voltage and current corresponding to the diode D_4 .

The simulation results completely validated the theoretical considerations, both qualitatively and quantitatively.

5.2. Experimental Results

A prototype of the proposed SEPIC converter was built in order to prove its functionality. The design parameters were the same as the ones in the design example and simulation. The semiconductors used were: S = STMicroelectronics STW70N60M2 and diodes $D_{1,2,4}$ = Silicon Carbide Diodes from STMicroelectronics STPSC4H065-type. The coupled inductors L_1 and L_2 were built on the same E71/33/32-3C94 FERROXCUBE core, and the turns numbers were manually adjusted in order to obtain the desired inductor values. For inductor L_3 , a separated core of the same type was used. The experimental waveforms were obtained with a fixed input voltage of $V_g = 30$ V, a fixed switching frequency of $f_s = 100$ kHz and a load of $R = 360 \Omega$. In Figure 19, the proposed SEPIC converter, together with the equipment used, can be observed.

Figure 19. View of the experimental setup.

The reference signal that is present in all waveforms on the oscilloscope is the drain-to-source transistor voltage. In Figure 20, the second waveform is the voltage across inductor L_1 (in red) and the third waveform is the inductor L_1 current (shown in cyan). In Figure 21, the first waveform is the drain-to-source voltage, (blue), the second one is the voltage across winding L_2 (red), followed by the current through inductor L_2 (cyan), with the last waveform being the output voltage (purple). The waveforms for inductor L_3 are presented in Figure 22. After the reference signal in blue, the voltage across inductor L_3 (in green) and the current through inductor L_3 (light blue) can be observed, while the last waveform is the output voltage (purple). It is confirmed that the acquired waveforms are in good accordance to those from the simulation.

Figure 20. Oscilloscope waveforms: drain to source voltage (dark blue— v_{DS}); voltage across L_1 (red— v_{L1}); current through L_1 (cyan— i_{L1}).

Figure 21. Oscilloscope waveforms: drain-to-source voltage (dark blue— v_{DS}); voltage across L_2 (red— v_{L2}); current through L_2 (cyan— i_{L2}) and output voltage (purple— V_{out}).

Figure 22. Oscilloscope waveforms: drain-to source-voltage (dark blue— v_{DS}); voltage across L_3 (green— v_{L3}); current through L_3 (cyan— i_{L2}) and output voltage (purple— V_{out}).

In Figure 23, the dependency of the efficiency against the output power at a constant output voltage of 120 V is presented.

Figure 23. The experimental efficiency against the output power.

6. Applicability of the Proposed SEPIC Converter in a PV System

For proving the usefulness of the proposed SEPIC-based converter in a PV application, a PV system with the block diagram presented in Figure 24, was built.

Figure 24. The block diagram of the PV system.

The structure of the PV application is similar with the block diagram presented in [64]. The chosen maximum power point (MPP) algorithm was perturb and observe (P&O), and it was implemented in an ADuCino development board equipped with the ADuCM360 ARM microcontroller (Analog Devices, Greater Boston, MA, USA) [68]. The current transducer used in this application was LEM HO-8-NSM/SP33 [69]. A resistive divider was used to measure the voltage across the PV modules. The MPPT algorithm is described in detail in the authors' work [64].

6.1. Simulation Results of the PV System Using the Proposed SEPIC Converter

To prove the utility of the proposed SEPIC-based converter in the PV system, a simulation that follows the scenario below was performed. All the changes encountered were step changes.

- at start-up $T_1 = 0$ ms, the irradiance was set to $G_1 = 1000$ W/m², and the load resistance was $R = 450$ Ω ;
- at $T_2 = 20$ ms, the load resistance suffered a change to $R = 325$ Ω ;
- at $T_3 = 28$ ms, the load resistance was changed to $R = 350$ Ω ;
- at $T_4 = 37$ ms, the load resistance was modified to $R = 360$ Ω ;
- at $T_5 = 68$ ms, the irradiance was suddenly modified from $G_1 = 1000$ W/m² to $G_2 = 800$ W/m²;
- at $T_6 = 98$ ms, the irradiance was set back to $G_3 = 1000$ W/m²;
- at $T_7 = 133$ ms, the output resistance was changed to $R = 460$ Ω ;
- at $T_8 = 135$ ms, the irradiance was set from $G_3 = 1000$ W/m² to $G_4 = 900$ W/m²;
- at $T_9 = 136$ ms, the output resistance was changed back $R = 360$ Ω ;
- the last change was at $T_{10} = 165$ ms, when the irradiance was modified from $G_4 = 900$ W/m² to $G_5 = 1000$ W/m².

The simulation time was 250 ms. The simulation step chosen was 20 ns, and the results were displayed each one hundred simulation steps. In Figure 25, the input (red) and the output (blue) power against time are represented. With these characteristics, the changings according to the scenario can be easily identified, and it can be remarked that the MPPT control regulates the absorbed power from the panel. The regulated power value is about 40 W at an irradiance equal to 1000 W/m², 30 W at 800 W/m² and around 35 W at a solar irradiance of 900 W/m².

Figure 25. Simulation of input and output power during time according to the proposed scenario.

The current-voltage and power-voltage characteristics of the PV module can be seen in Figure 26. During the simulation, the instantaneous position of the operating point (OP) on the current-voltage (I-V) characteristic is shown with the green arrow, while the black arrow points to the instantaneous position of the operating point on the power-voltage (P-V) characteristic. The system is able to reach the MPP, even if the OP is located before or after the MPP. The MPP can be found at the point marked on the graph with “A”. Because the load was initially set to $R = 450$ Ω , the characteristics passed through the MPP, and overpassed point “E”. Changing the value of the load to $R = 325$ Ω determined the return to point “A”, but overpassed point “A” to the left. Adjusting the resistor to $R = 350$ Ω caused the return to point “A” but slightly exceeded to the right, with small oscillations around point “A”. When $T_4 = 37$ ms, the output resistance was changed to $R = 360$ Ω , which determined the return to and placement in point “A,” corresponding to the MPP. A step transition in solar irradiance from $G_1 = 1000$ W/m² to $G_2 = 800$ W/m² produced a displacement from points “A” to “B” and an evolution on the PV characteristic related to point “C”. A step increase in the irradiance to 1000 W/m² produced a jump of the characteristics from “C” to “D” and a progression of the PV characteristic that ended with

the value of the solar irradiance corresponding to point “A”. Changing the value of the load to $R = 460 \Omega$ determined the exceedance of point “A” to the right. Because at $T_8 = 135 \text{ ms}$, the irradiance was set from $G_3 = 1000 \text{ W/m}^2$ to $G_4 = 900 \text{ W/m}^2$, again a jump took place from point “E” to point “F” and a search of the MPP on the characteristic corresponding to 900 W/m^2 . When the load was changed back to $R = 360 \Omega$, it determined a return to the left of the characteristics, finally reaching the point “G”. The last modification of the solar irradiance, back to $G_5 = 1000 \text{ W/m}^2$ produced a jump from “G” to “H” and a displacement on the solar irradiance characteristic to the point “A”. At the end, small oscillations around point “A” could be observed due to the P&O MPP algorithm.

Figure 26. Simulation of the OP movement on the I-V and P-V PV module characteristics.

The duty cycle evolution that results from the P&O algorithm is depicted in Figure 27. At the end, when the irradiance and the load do not modify anymore, the duty cycle is slightly modified around the expected value of 60%.

Figure 27. Duty cycle evolution against time for the proposed scenario.

Figure 28 presents how the output voltage modifies along the proposed scenario. It is confirmed that the desired dc output voltage value of 120 V can be achieved if the irradiance and the load are high enough and they do not modify.

Figure 28. Output voltage against time during the proposed scenario.

An overall examination of Figures 25–28, clearly reveals the correlations between the input and output power characteristics, current-voltage and power-voltage characteristics, duty cycle and output voltage evolution regarding the time moments when changes occur.

6.2. Experimental Results of the PV System Using the Proposed SEPIC-Based Converter

In this section, the novel proposed converter supplied by two PV panels connected in series and having P&O as a MPPT method is presented. For solar irradiance and PV temperature measurement, a pyranometer [70] was used. The pyranometer produces a voltage (V_{GPV}) proportional to the incident solar irradiance. For the PV temperature measurement (T_{PV}), the other pyranometer voltage (V_{TPV}) is measured and the temperature can be found according to the formula [70]:

$$T_{PV} = \frac{V_{TPV} - 1.84}{0.092} [^{\circ}\text{C}] \quad (39)$$

In Figures 29 and 30, for an irradiance of 885.6 W/m^2 the corresponding $V_{GPV} = 7.38 \text{ V}$ and $V_{TPV} = 8.24 \text{ V}$. According to (39), the PV temperature is equal to $T_{PV} = 69.56^{\circ}\text{C}$. In Figure 29, the oscilloscope capture shows the start-up, which lasts approximately 5 s.

In the down to up order, the first waveform drawn in dark-blue and labeled “ V_{in} ” is the input voltage. In the beginning, it is equal to the open-circuit voltage of the PV panels, of about 42 V, and then it decreases according to the characteristic to about 35 V. The MPP is reached after approximately 5 s, and this can be seen on the third waveform labeled “ V_{out} ” (in purple). The P&O algorithm continuously modifies the duty cycle by increasing and decreasing it with one step. Because the irradiance is constant, the converter is maintained around the same OP. The output voltage in this case is equal to 110 V. The second signal is the input current, labeled “ I_{in} ” and depicted with cyan. The fourth waveform presented, labeled “ P_{in} ”, is the instantaneous power at the input provided by the PV cell. This power is displayed on the oscilloscope, computing the product between the voltage and current at the input. To demonstrate the functionality of the P&O control algorithm, the input power needs to be maximized. As the current increases and the input voltage slightly decreases, the input power provided by solar conversion increases and proves the correct behavior of the control algorithm. In Figure 30, the same waveforms are shown in different order: “ V_{in} ”, “ V_{out} ”, “ I_{in} ” and “ P_{in} ” for the following scenario. Because the measurements were performed on a sunny day, without any cloud in the sky, in order to prove the functionality of the converter driven by the P&O algorithm, after about 10.4 s, a part of the PV panel was shaded for approximately 6 s. The input voltage and power decrease can be observed in Figure 30, and the steps of the P&O implementation are also visible, validating the effectiveness of the P&O implementation.

Figure 29. Oscilloscope waveforms at start-up for: input voltage “ V_{in} ” (dark-blue), input current “ I_{in} ” (cyan), output voltage “ V_{out} ” (purple), and input power “ P_{in} ” (red), in down to up order.

Figure 30. Oscilloscope waveforms for: input voltage “ V_{in} ”(dark-blue), output voltage “ V_{out} ”(purple), input current “ I_{in} ”(cyan) and input power “ P_{in} ”(red), in down to up order.

7. Discussion

A new step-up/step-down converter with a step-up characteristic steeper than that of the classical SEPIC and hybrid SEPIC is introduced. As a result, the new topology is suitable in applications where an output voltage much higher than the input voltage is needed. Inductor coupling introduces an additional degree of freedom, and this allows for the minimization of certain stress values. After deriving the steady state equations and sketching the main waveforms, design equations were provided, and the simulations validated the theoretical concepts. In order to prove the feasibility and usefulness of the proposed converter, a PV solar system was built around it. It is shown that, using the P&O algorithm, the system can be maintained on the MPP and the maximum power capabilities of the PV panel can be used. In addition to its higher step-up capability, the converter has the advantage of offering a non-inverting output voltage and a non-floating transistor, which simplifies the control.

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