Article

Effect of Process Parameters on Mode Conversion in Submicron Tapered Silicon Ridge Waveguides

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Abstract: The modal property and light propagation in tapered silicon ridge waveguides with different ridge heights are investigated for a silicon on insulator (SOI) platform with a 500 nm silicon (Si) thickness. Mode conversion between the transverse magnetic (TM) fundamental and higher-order transverse electric (TE) modes occurs when light is propagated in a waveguide taper. Such a conversion is due to mode hybridization resulting from the vertical asymmetry of the cross-section in the ridge waveguides. The influence of angled sidewalls and asymmetric cladding on mode conversion is also studied. It is shown that a very long taper length (adiabatic) is required for a complete conversion to take place. Conversely, such mode conversion could be suppressed by designing a short non-adiabatic taper. Our results show that significant improvement in performance metrics can be achieved by considering process parameters' effect on mode conversion. With an optimum selection of the etching depth and accounting asymmetries due to angled sidewalls and cladding, we demonstrate an 84.7% reduction in taper length (adiabatic) for mode conversion and a 97% efficiency TM preserving taper (ultra-short). The analysis is essential for applications such as compact polarizers, polarization splitters/rotators, and tapers for TM devices.

Keywords: photonic integrated circuits; silicon photonics; mode hybridization; mode converters; polarization splitter and rotators; tapered waveguides; adiabatic tapers; angled sidewalls

1. Introduction

In recent years submicron silicon-on-insulator (SOI) platform is becoming widely used for ultra-compact complementary metal-oxide-semiconductor (CMOS) compatible Photonic Integrated Circuits (PICs) driven by low cost, low power, and high-bandwidth interconnects [1]. It is possible to design ultra-compact PICs on SOI due to their intrinsic high-index-contrast (Δ) in silicon waveguides. In a high-Δ optical waveguide with vertical asymmetry, mode hybridization is observed at some particular widths, which may cause mode conversion in tapered structures [2,3]. This property can cause problems in TM-type PICs but can be favorable for realizing compact mode converters.

Silicon photonics PICs are mainly demonstrated to work for the TE-polarization due to their strong mode confinement. However, TM-polarization is also very beneficial for many applications, and it has some unique advantages over TE-polarization. PICs operating in the TM-fundamental mode are more tolerant to fabrication variations and demonstrate low propagation losses [4]. Additionally, the TM mode has a stronger evanescent field making it more suitable for sensing applications [5]. An adiabatic taper is an indispensable basic circuit design element for both polarizations [6,7]. However, to construct adiabatic tapers for the TM-polarization, extra care needs to be given. Mode hybridization in adiabatic tapers can cause an undesired conversion between the TM-fundamental and higher-order TE-modes, which results in excess losses and channel cross-talks [8]. Therefore, this

unwanted mode conversion needs to be suppressed by carefully designing tapers so that TM-mode is maintained throughout with near 100% efficiency (TM-preserving tapers) [9].

On the other hand, by tailoring the mode hybridization in an adiabatic taper, several polarization splitters-rotators (PSRs) have been realized [10–24]. The PSR components are required to mitigate birefringence in the SOI platform [25,26]. In a PSR, light is coupled with arbitrary polarization, where it is first split into two orthogonal components. Then, one polarization state is rotated 90 degrees while the other remains unchanged. Waveguide-type integrated PSRs are challenging to realize, as it is not easy to rotate the orthogonal modes in a planar waveguide. Most polarization rotation approaches need complex, non-even standard fabrication steps such as additional Si layer deposition, etching with high alignment accuracy, multistep lithography, non-vertical etching [27,28]. However, the design technique employing the concept of mode hybridization does not involve any complex fabrication. The difference lies in the input TM-polarization is first transferred to high order mode (TE_1) before converting it to TE_0. The devices based on mode hybridization have the advantages of fabrication tolerance and low insertion loss. Here, the key is the mode evolution in the adiabatic taper as a result of mode hybridization. This enables an efficient conversion from TM_0 to TE_1 mode. The latter is then transferred to the TE_0 [10–24]. Note that the footprint of the adiabatic taper can limit the overall dimension of the PSR. Therefore, reducing the size of the adiabatic taper is much desired.

The two most common waveguides in a PIC design are strip and ridge types. In an SOI platform, the under cladding is always SiO_2 (silicon oxide). It is possible to have upper cladding with different materials like silicon nitride, silicon oxide, and air (no cladding). Mode conversion in an SOI strip waveguide with an upper air cladding is reported previously, as this makes it asymmetrical in the vertical direction [2,3]. It is also possible to avoid this mode conversion by introducing SiO_2 top cladding instead of air to eliminate vertical asymmetry [3]. However, for this to happen, waveguides should be fabricated perfectly rectangular (without any sidewall angle). All the fabrication processes introduce some sidewall angles causing waveguides to be inherently asymmetric even with top SiO_2 cladding. As reported in Ref. [29], the sidewall angle should be less than 2^0 to suppress mode hybridization and avoid undesired mode conversion. However, it is very challenging to eliminate the sidewall angle, and a typical value in most of the fabrication processes is around 8^0 [29–31].

The other popular waveguide, particularly for silicon-based integrated optoelectronics is SOI ridge waveguides [32–35]. The ridge waveguide structure is inherently asymmetric in the vertical direction, even when considering SiO_2 upper cladding (without angled sidewalls). Consequently, strong mode conversion is observed between TM_0 mode and higher-order TE polarization in regular adiabatic and bi-level tapers [9]. However, in previous reports, no emphasis was given to various process parameters since strong mode hybridization was easily achieved in an SOI platform with relatively thin silicon thickness. A taper length of <200 microns was sufficient for mode conversion [9,11,12,17,19,24]. Note that, due to strong mode hybridization in ridge waveguides, it is also difficult to depress mode conversion in ultra-short low loss tapers in TM-type PICs. Figure 1a,b show the cross-section of the ideal rectangular waveguide and waveguide with angled sidewalls, respectively.

Even though the SOI platform with 220 nm silicon thickness is very popular, the SOI platform with thicker silicon (400–500 nm) is attractive to achieve efficient coupling between the III-V laser and silicon waveguide [36]. Additionally, various high-performance passive components, such as optical spiral delay lines, ring resonators, and Bragg grating, were also reported with 500 nm thick silicon [37]. For the first time, this paper studies the mode conversion in submicron 500 nm SOI for different waveguide ridge heights and upper claddings. The study paves the way for realizing compact PSRs and robust TM-type circuits. Additionally, it shows that, without optimization, adiabatic tapers for mode conversion would be at least ten times longer (1000s of microns) compared to relatively thinner SOI platforms. To reduce this taper length, we extend the work performed on angled sidewalls

in strip waveguides [29] to the ridge waveguides. By selecting an optimum etch-depth and considering asymmetries caused by angled sidewalls and cladding, we demonstrated an 84.7% reduction in the overall taper length needed for polarization mode converters. It is also shown that ultra-short adiabatic tapers with 97% TM preserving efficiency can be achieved. These results illustrate the importance of accounting for the process parameters while designing TM preserving and mode evolution tapers.
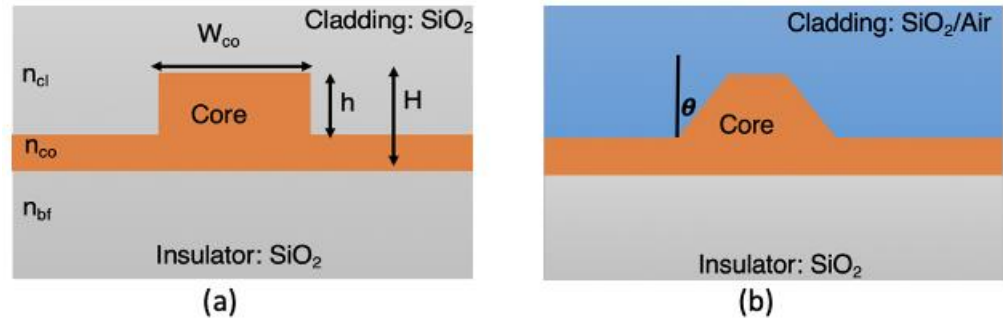
Figure 1. The cross-section for an SOI ridge waveguide (**a**) without sidewall angle (**b**) with sidewall angle.

2. Structure and Analysis

In this work, we consider tapered submicron SOI ridge waveguides. A regular lateral adiabatic taper is considered for studying mode conversion. In the present example, the SOI wafer has total silicon (Si) height H = 500 nm, and the refractive indices of the Si and SiO$_2$ are 3.455 (nSi) and 1.445 (nSiO$_2$), respectively. An SOI wafer with 500 nm Si thickness is available with many Multi-Project-Wafer (MPW) offerings [30,31].

In our analysis, we have considered three different ridge heights, i.e., h = 200 nm (0.4 H), h = 250 nm (0.5 H), and h = 300 nm (0.6 H). For clarity purposes, the etch-depth (h) is given as a ratio to the total silicon height (H). For a deeply etched ridge waveguide, the ridge height (h) is larger than the slab height (H-h), while for low etch-depth, the opposite is true. Figure 1a shows an ideal rectangular ridge waveguide with SiO$_2$ top cladding. However, the fabrication process is not ideal, and it introduces angled sidewalls [Figure 1b]. Since 8^0 is the most commonly reported sidewall angle [29–31], we study the effect of this angle on the mode conversion. We also evaluate mode property and light propagation in a ridge waveguide exposed to air with 8^0 sidewalls. By quantifying the effect of etch-depth, angled sidewalls, and asymmetric cladding on mode conversion in tapered ridge waveguides, designs can be made more compact. Finally, we combine all the findings to reduce the length requirement of an adiabatic taper for 100% mode conversion. Additionally, calculations are done to find the best possible TM preserving efficiency that can be achieved in non-adiabatic short tapers.

2.1. Mode Hybridization Widths

For any waveguide eigenmode, the mode polarization ratio (γ) can be defined as:

$$\gamma = \frac{\int |E_X|^2 dxdy}{\int |E_X|^2 dxdy + \int |E_y|^2 dxdy} \tag{1}$$

where E_x and E_y are the components of the electric field in the x- and y-directions, respectively. This equation is true for any eigenmode. For a typical TE mode, the Ex-component is much stronger than the E_y component, and consequently, the ratio γ is close to 100%. On the other hand, for a TM mode, ideally γ = 0. Therefore, modes are hybridized when $0 < \gamma < 100\%$. In other words, at mode hybridization widths, the E_x and E_y components of two different modes become comparable to each other. By calculating γ for all guided modes at different widths, mode hybridization regions can be identified. However, in this

work, we have used commercial software to determine waveguide widths at which modes are hybridized. A Finite-Difference-Eigenmode (FDE) solver (from Ansys Lumerical) is used to identify the region where mode crossing occurs between TM_0 mode and TE_1 mode. At the core silicon width (W_{co}) of mode crossing, due to vertical asymmetry, TM_0 and TE_1 modes are hybridized [22]. We run FDE simulations, varying the ridge waveguide width (W_{co}) from 0.5 µm to 3 µm. At each step, the effective index (n_{eff}) for the first 4–5 modes are calculated, and we then subtract from it the n_{eff} of the slab mode (without the ridge). For a ridge waveguide, an optical mode is supported if its effective index is higher than the slab mode. We then plot this difference (Δn_{eff}) to determine the width (W_h) at which mode hybridization is observed.

Figure 2a–c shows the Δn_{eff} for the SOI ridge waveguides for different etch depths for oxide-cladded ridge waveguide without any sidewall angle as the width of core silicon (W_{co}) varies from 0.5 µm to 3 µm. The mode hybridization between TM_0 and TE_1 is observed at silicon waveguide widths ($W_{co} = W_h$) of 1.47µm, 1.37 µm, and 1.23 µm for the ridges with etch-depths of 0.6 H, 0.5 H, and 0.4 H, respectively. It can be seen that W_h gets narrower when the waveguide etch-depth is reduced. As the latter is reduced from 0.6 H to 0.4 H, the mode hybridization region shifts from $W_h = 1.47$ µm to 1.23 µm. The simulation shows no significant change in the mode hybridization width (W_h) due to vertical asymmetry introduced by asymmetric cladding and angled sidewalls.

2.2. Taper Design for Efficient Mode Conversion

Due to mode hybridization at W_h, mode conversion between TM_0 and TE_1 will occur when light propagates along an adiabatic taper if its end widths W_1 and W_2 satisfy the condition: $W_1 < W_h < W_2$. In our design, the taper end width is chosen as $W_1 = 1$ µm and $W_2 = 2$ µm (Figure 3). This will satisfy the mode conversion condition for a ridge waveguide with all the selected etch depths ($W_1 = 1$ µm $< W_h = [1.47$ µm, 1.37 µm, 1.23 µm] $< W_2 = 2$ µm). For TM-type PICs, where low loss TM_0 tapers are desired, mode conversion is harmful and causes unwanted losses. One of the simplest methods to avoid such unwanted mode conversion is to design tapers whose end widths are either (W_1, W_2) $< W_h$ or (W_1, W_2) $> W_h$. However, if some design requirements put constraints on the end widths ($W_1 < W_h < W_2$), ultra-short non-adiabatic tapers should be implemented to preserve the TM fundamental mode.

An Eigen-Mode-Expansion method (EME-Ansys Lumerical) is used to simulate the mode conversion efficiency as the taper length (L_{tp}) increases. For scanning length in a very large range, the EME algorithm is very efficient compared to Finite-Difference-Time-Domain solver (FDTD). The simulations are performed for three different ridge heights under three different process conditions. The beam propagation simulation is also done in 3D FDTD to visualize the light propagation along the taper. For beam propagation simulation in FDTD, the same taper lengths of 200 µm (adiabatic) and 10 µm (TM-preserving) are chosen for different process conditions, and conversion ratios obtained are shown as well. The difference between EME and FDTD algorithm in determining the conversion efficiency is only 0.35%. The results are as follows:

2.2.1. (0.6. H) Ridge Waveguide (Ridge Height > Slab Height)

We start our analysis with a deeply etched ridge waveguide. The ridge height is 300 nm (0.6 H), corresponding to a slab height of 200 nm. Figure 4 shows mode conversion efficiencies when the TM_0 mode is launched and coupled to the TE_1 mode. The TM_0 mode propagates along the adiabatic taper with a start and end widths of $W_1 = 1$ µm and $W_2 = 2$ µm, respectively. The simulations are performed for angled sidewalls and different top cladding conditions. From Figure 4, one can realize very highly efficient tapers for TM_0 to TE_1 mode conversion with ~100% conversion efficiency by appropriately selecting L_{tp}. The L_{tp} required for mode conversion is observed to be strongly dependent on the process asymmetries related to the angled sidewalls and cladding material.
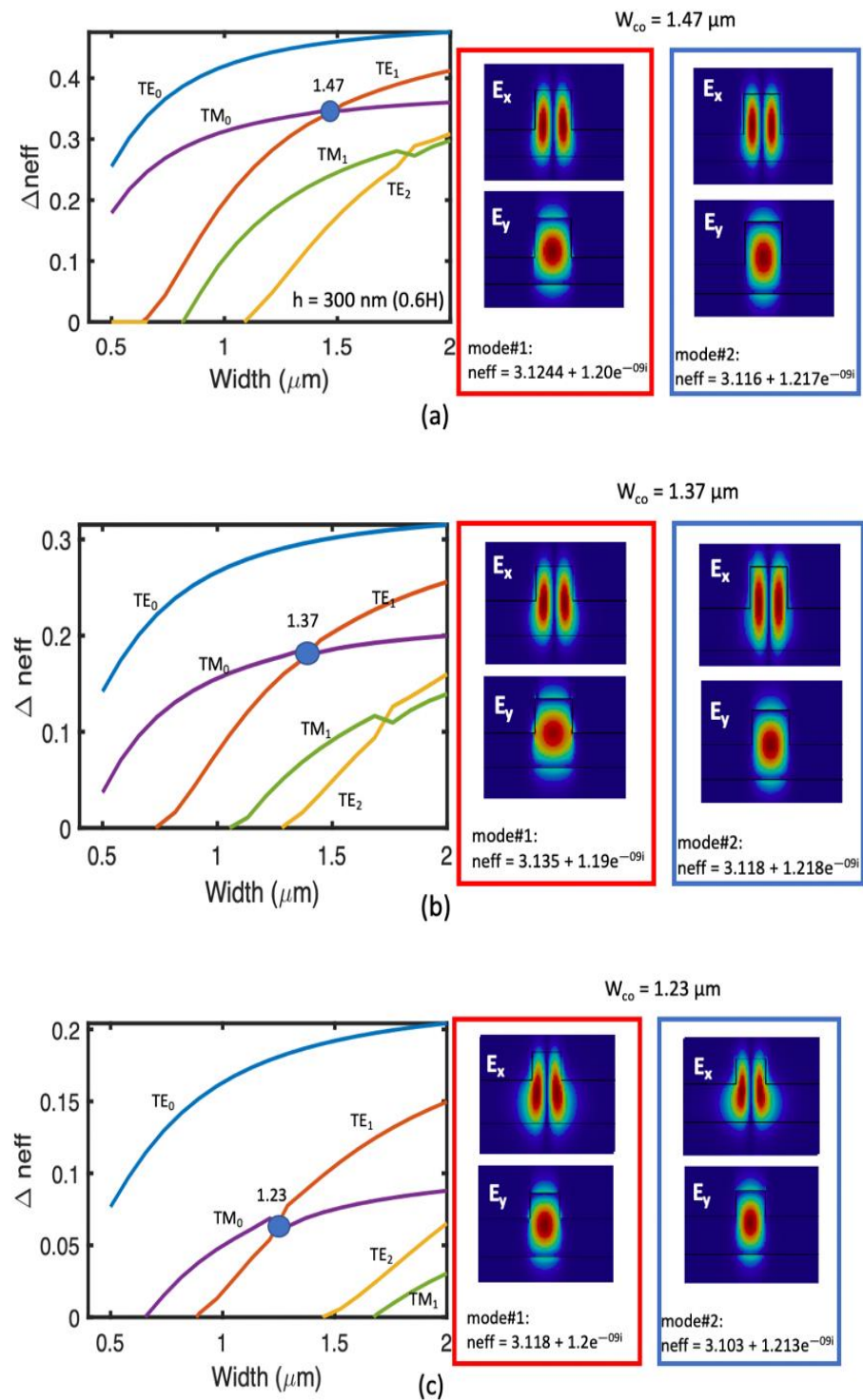
Figure 2. The calculated Δn_{eff} (n_{eff} (mode)-n_{eff}(slab)) for the eigen modes of SOI ridge waveguide with different etch depths along with hybridized mode profiles. (**a**) h = 300 nm (0.6 H); (**b**) h = 250 nm (0.5 H); (**c**) h = 200 nm (0.4 H). The total height of silicon is H = 500 nm and simulations are done at 1550 nm wavelength. Here the sidewall angle $\theta = 0^0$ and n_{cl} = 1.445 (oxide cladding).
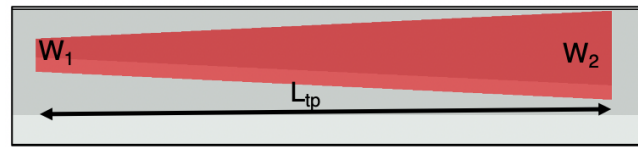
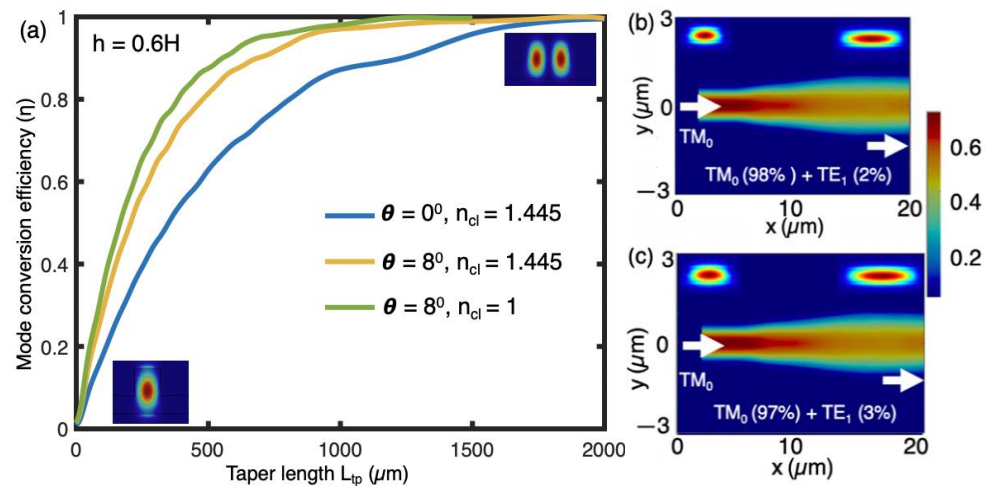**Figure 3.** Schematic of regular adiabatic taper.

Figure 4. (**a**) The mode conversion efficiency (η) as the function of taper length (L_{tp}) when TM_0 mode is launched. (**b**) Light propagation with $\theta = 0^0$ and $n_{cl} = 1.445$. (**c**) Light propagation with $\theta = 8^0$ and $n_{cl} = 1.445$. The total height of silicon is H = 500 nm, ridge height (h) = 0.6 H and simulations are done at 1550 nm wavelength.

Under an ideal rectangular waveguide with symmetric cladding (SiO_2), a taper length of 1820 µm is required for the complete mode conversion. However, when angled sidewalls are accounted for, the size is reduced to 1600 µm. This enhanced mode hybridization corresponds to a 12% reduction in taper length. Alternatively, when an air top cladding and sidewall angle are simultaneously present, the length for 100% mode conversion is reduced to 1110 µm. This corresponds to a total reduction of 39%, which is very significant compared to an ideal case.

It is important to note that mode conversion for SiO_2-cladding waveguide can be significantly reduced by choosing ultra-short taper lengths. From Figure 4, the optimum length is 10 µm, for which the conversion efficiency is very low. For this taper length, the TM_0 mode preserving ability is highest, i.e., 98%, see FDTD (Finite-Difference Time-Domain) simulation in Figure 4b). Since it is not possible to avoid angled sidewalls, it must be considered when designing low-loss TM tapers. Figure 4c shows the transmission efficiency assuming a sidewall angle of 8^0. The drop-in efficiency due to angled sidewalls is only 1%, which is acceptable.

Figure 5 shows FDTD simulation along an adiabatic taper of length 200 µm when the launched mode is TM_0. Figure 5a,b are shown for SiO_2 cladding with 0^0 and 8^0 sidewall angles, respectively, while Figure 5c is shown for angled air-cladding waveguide. As predicted, the conversion efficiency increases with process asymmetries of the angled sidewalls and air-top cladding.
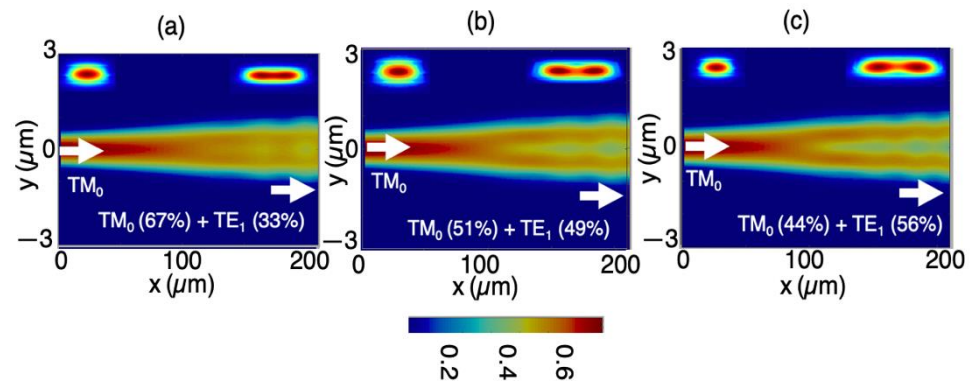
Figure 5. The light propagation in the designed taper L_{tp} = 200 μm (**a**) θ = 0^0 and n_{cl} = 1.445 (**b**) θ = 8^0 and n_{cl} = 1.445 (**c**) θ = 8^0 and n_{cl} = 1. The total height of silicon is H = 500 nm, ridge height (h) = 0.6 H and simulations are done at 1550 nm wavelength.

2.2.2. (0.5. H) Ridge Waveguide (Ridge Height = Slab Height)

The etch-depth of the ridge waveguide is now reduced and made equal to slab height. In this case, both are equal to 250 nm. We observe a substantial increase in mode conversion efficiency as the ridge height is reduced. From Figure 6, even for an ideal case with no sidewalls and symmetric SiO_2 cladding, the taper length for an efficient mode conversion is 985 μm. With angled sidewalls, the required L_{tp} is 750 μm, representing a 25% reduction in the overall length. Finally, when angled sidewalls and air-cladding are considered, the corresponding L_{tp} for mode conversion is 655 μm, which corresponds to a 33.5% reduction compared to an ideal case. When compared with deeply etched ridge waveguide, the effect of angled sidewalls is more pronounced. Since it is not possible to fabricate waveguides without sidewalls, the maximum efficiency is 94.5% for low-loss TM tapers for the sidewall angle of 8^0. For TM polarization preserving taper, Figure 6b and 6c show FDTD propagation in an ultra-short L_{tp} = 10 μm for sidewall angles of θ = 0^0 and θ = 8^0, respectively.
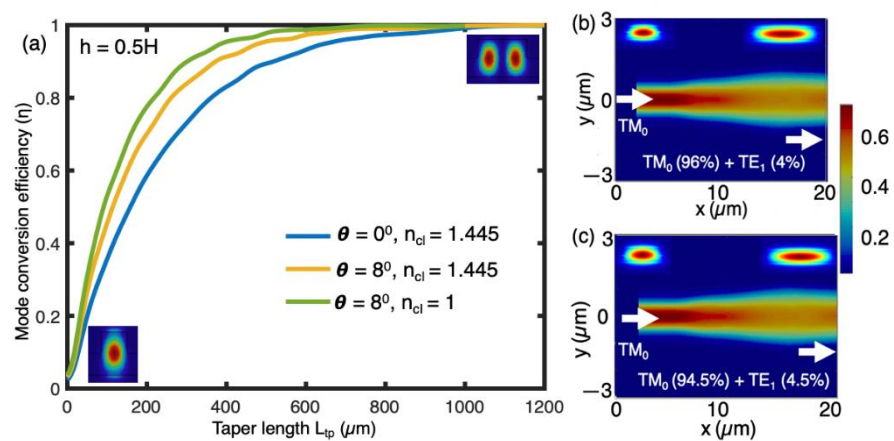
Figure 6. (**a**) The mode conversion efficiency (η) as the function of taper length (L_{tp}) when TM_0 mode is launched. (**b**) Light propagation with θ = 0^0 and n_{cl} = 1.445. (**c**) Light propagation with θ = 8^0 and n_{cl} = 1.445. The total height of silicon is H = 500 nm, ridge height (h) = 0.5 H, and simulations are done at 1550 nm wavelength.

Figure 7 shows the light propagation along an adiabatic L_{tp} = 200 μm taper, similar to Figure 5 but for 0.5 H etch-depth. Compared to Figure 5, an increase in mode conversion efficiency for the same taper length is observed. It is evident that mode conversion in a tapered ridge waveguide is strongly dependent on etching depth. In a deeply etched waveguide, even when maximum asymmetry due to angled sidewalls and air top cladding is accounted, the conversion is only 56%, whereas, for a 0.5 H waveguide, it is 78%.

Therefore, process parameters play an important role in mode conversion, and they must be accounted for in the PIC circuit design. Furthermore, a small change in the etch depth can cause a significant difference in the mode conversion.
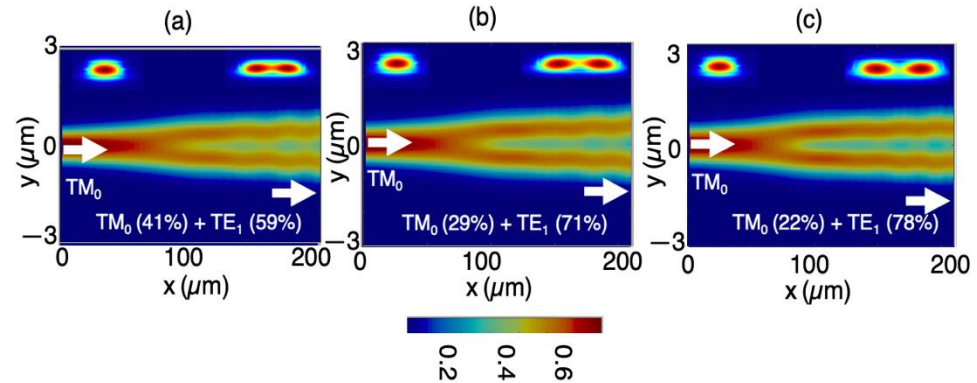
Figure 7. The light propagation in the designed taper L_{tp} = 200 μm (**a**) $\theta = 0^0$ and n_{cl} = 1.445 (**b**) $\theta = 8^0$ and n_{cl} = 1.445 (**c**) $\theta = 8^0$ and n_{cl} = 1. The total height of silicon is H = 500 nm, ridge height (h) = 0.5 H and simulations are done at 1550 nm wavelength.

### 2.2.3. (0.4. H) Ridge Waveguide (Ridge Height < Slab Height)

We finally consider a case of a low etched ridge waveguide in which ridge height is less than slab height. As seen from the 0.5 H waveguide analysis, the mode conversion efficiency increases as the etch-depth is reduced. For a low etched ridge waveguide, the mode conversion efficiency is maximum. It is not possible to further reduce the etch depth to enhance efficiency. Reducing the etch depth below certain limits causes TM fundamental mode to become leaky, and it is not well supported in the waveguide. However, it is still possible to increase the mode conversion efficiency and reduce the taper length requirement by accounting for enhanced mode hybridization due to angled sidewalls and asymmetric cladding. As depicted in Figure 8, a 100% conversion efficiency between TM_0 and TE_1 mode is obtained at a taper length of 440 μm for an ideal case. The taper length is only 376 μm when the waveguide is modeled with a sidewall angle of 8^0. When both angled sidewalls and upper air cladding are considered, the size reduces to 277 μm. Additionally, low etch depth waveguides are reported to show lower propagation loss [37]. This is due to a reduction in the optical mode interaction with the ridge sidewall.
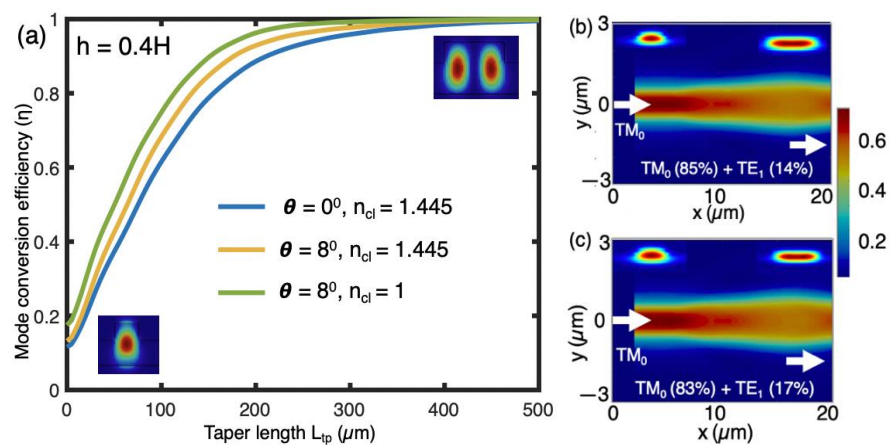
Figure 8. (**a**) The mode conversion efficiency (η) as the function of taper length (L_{tp}) when TM_0 mode is launched. (**b**) Light propagation with $\theta = 0^0$ and n_{cl} = 1.445. (**c**) Light propagation with $\theta = 8^0$ and n_{cl} = 1.445. The total height of silicon is H = 500 nm, ridge height (h) = 0.4 H and simulations are done at 1550 nm wavelength.

Since in a low etch-depth ridge waveguide, very strong mode conversion is observed, it is not recommended to design an ultra-short taper to preserve the TM mode. Figure 8 shows the light propagation in a taper with length L_{tp} = 10 μm. Even for an ideal case without any sidewall angle, the TM mode is maintained with only 85% efficiency. This efficiency further reduces to 83% when modeled with sidewalls.

Figure 9 shows FDTD beam propagation results along the designed taper with L_{tp} = 200 μm. A considerable increase in mode conversion efficiency is observed as expected compared to the deeply etched ridge waveguide (see Figure 5).
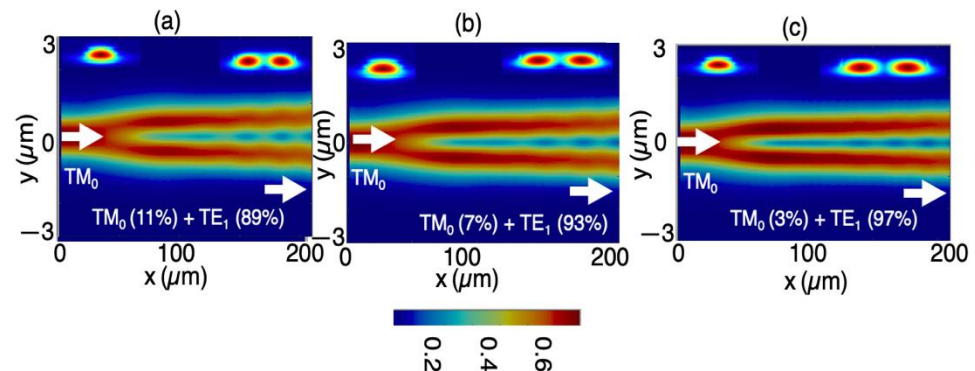
Figure 9. The light propagation in the designed taper L_{tp} = 200 μm (**a**) θ = 0^0 and n_{cl} = 1.445 (**b**) θ = 8^0 and n_{cl} = 1.445 (**c**) θ = 8^0 and n_{cl} = 1. The total height of silicon is H = 500 nm, ridge height (h) = 0.4 H and simulations are done at 1550 nm wavelength.

Table 1 summarizes the important results for all the cases. It is concluded that, for efficient mode conversion, taper length can be significantly reduced by choosing the optimum process parameters. For a 100% mode conversion, we showed that an 1820 μm length taper could be reduced to a length of 277 μm by using a small ridge height and by considering angled sidewalls in an air clad waveguide. This corresponds to a total of 1540 μm (84.7%) decreases in the overall footprint. Even though an ultra-short taper successfully suppresses unwanted mode conversion, the TM_0 mode preserving efficiency is greatly improved if designed with a high etch-depth ridge waveguide.

Table 1. Results Summary.

	Silicon Height H = 500 nm					
	Ridge Height (0.6H)		Ridge Height (0.5 H)		Ridge Height (0.4 H)	
	Mode Converter (L_{tp})	TM Preserving Efficiency (L_{tp} = 10 μm)	Mode Converter (L_{tp})	TM Preserving Efficiency (L_{tp} = 10 μm)	Mode Converter (L_{tp})	TM Preserving Efficiency (L_{tp} = 10 μm)
θ = 0^0 n_{cl} = 1.445	1821 μm	98%	985 μm	96%	440 μm	85%
θ = 8^0 n_{cl} = 1.445	1600 μm	97%	750 μm	94.5%	376 μm	83%
θ = 8^0, n_{cl} = 1	1110 μm	96%	655 μm	94%	277 μm	80%

3. Discussion

The insertion loss (IL) of a photonic device is defined as:

$$IL = -10 \log \left(\frac{P_{out}}{P_{in}} \right) \qquad (2)$$

where P_{in} indicates input optical power and P_{out} indicates output optical power. In addition to surface roughness, the main loss mechanism in these devices is the presence and excitation of unwanted optical modes. In the case of TM to TE_1 mode converter, the percentage of TM mode in the output power contributes towards loss. Therefore, Equation (2) can be modified as:

$$\text{IL (Mode Convertor)} = -10\log\left(\frac{P_{out}(TE_1)}{P_{in}(TM_0)}\right) \tag{3}$$

Similarly, for a TM taper, the excitation of unwanted TE_1 mode is the main source of the loss. The insertion loss of the TM preserving taper can be defined as:

$$\text{IL (TM preserving Taper)} = -10\log\left(\frac{P_{out}(TM_0)}{P_{in}(TM_0)}\right) \tag{4}$$

Therefore, the best low-loss configuration for the mode conversion is the air cladding with a partial etch of 0.4 H (0.176 dB), whereas for the TM preserving taper is the case of symmetric cladding with a ridge height of 0.6 H (0.084 dB). Here we have assumed an rms sidewall roughness of 3 nm.

Mode converters based on mode hybridization in adiabatic tapers are highly tolerant to fabrication tolerance. This is because irrespective of fabrication deviation in width, the mode hybridization width is always found along the taper. However, if the input width (W_1) is too close to the mode hybridization width (W_h), the device is more prone to fabrication variations. Along with width variation, there is also a possibility of thickness variation and changes in the sidewall angle. We study the effect of thickness and changes in sidewall angle (see Figure 10). From this figure, it can be seen that the decrease in the ridge height slightly improves the mode conversion efficiency. Similarly, the increase in sidewall angle had a similar effect on the efficiency. However, fabrication variation does not cause much difference in the performance.
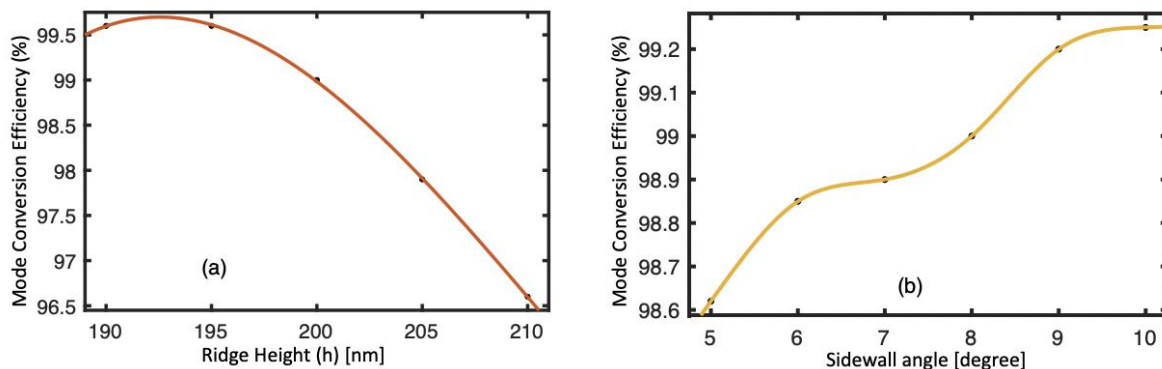
Figure 10. The mode conversion efficiency with (**a**) thickness variation due to fabrication ($\theta = 8^0$) (**b**) Sidewall angle (h = 200 nm) The and simulations are done at 1550 nm wavelength with $n_{cl} = 1$ and $L_{tp} = 277$ µm.

4. Conclusions

In summary, the effect of ridge height, sidewall angle, and asymmetric cladding on mode conversion in a tapered submicron 500 nm SOI ridge waveguide is analyzed. The waveguide is highly asymmetrical in the vertical direction irrespective of top cladding (SiO_2 or air). Therefore, if the taper end widths lie in between the mode hybridization regions, then mode conversion between TM fundamental mode and higher-order TE modes can occur. This mode conversion in the submicron ridge waveguide is strongly dependent on the ridge height. The SOI ridge tapered waveguide with reduced etching depth has efficient mode conversion compared with deeply etched ones. Angled sidewalls and asymmetric cladding can further strengthen the mode hybridization and mode conversion. We demonstrate an 84.7% reduction in length for an efficient mode conversion with a low

etched waveguide (8^0 sidewalls) with air-top cladding. Such efficient mode conversion enables applications like compact polarization rotators/splitters. For general TM-type PICs, such mode conversions are not usually desired because it introduces excess loss and cross talk. It has also been shown that for such applications, PICs should be implemented using ultra-short non-adiabatic tapers designed with deep-etched ridge waveguides. This will ensure TM fundamental mode is maintained in the circuit. This work also shows that 97% efficient TM preserving taper can be designed with a deep-etched ridge waveguide.

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References

1. Chrostowski, L.; Hochberg, M. *Silicon Photonics Design: From Devices to Systems*; Cambridge University Press: Cambridge, UK, 2015; ISBN 978-1-107-08545-9.
2. Vermeulen, D.; Acoleyen, K.V.; Ghosh, S.; Selvaraja, S.; Debackere, P.P.P.; Dumon, P.; Bogaerts, W.; Roelkens, G.; Thourhout, D.V.; Baets, R. Efficient Tapering to the Fundamental Quasi-TM Mode in Asymmetrical Waveguides. In Proceedings of the 15th European conference on Integrated Optics (ECIO 2010), Cambridge, UK, 7–9 April 2010; p. 2.
3. Dai, D.; Bowers, J.E. Novel Concept for Ultracompact Polarization Splitter-Rotator Based on Silicon Nanowires. *Opt. Express* **2011**, *19*, 10940–10949. [CrossRef]
4. Qiu, C.; Sheng, Z.; Li, H.; Liu, W.; Li, L.; Pang, A.; Wu, A.; Wang, X.; Zou, S.; Gan, F. Fabrication, Characterization and Loss Analysis of Silicon Nanowaveguides. *J. Light. Technol.* **2014**, *32*, 2303–2307. [CrossRef]
5. Densmore, A.; Vachon, M.; Xu, D.-X.; Janz, S.; Ma, R.; Li, Y.-H.; Lopinski, G.; Delâge, A.; Lapointe, J.; Luebbert, C.C.; et al. Silicon Photonic Wire Biosensor Array for Multiplexed Real-Time and Label-Free Molecular Detection. *Opt. Lett.* **2009**, *34*, 3598–3600. [CrossRef] [PubMed]
6. Dai, D.; He, S.; Tsang, H.-K. Bilevel Mode Converter between a Silicon Nanowire Waveguide and a Larger Waveguide. *J. Light. Technol.* **2006**, *24*, 2428–2433. [CrossRef]
7. Barkai, A.; Liu, A.; Kim, D.; Cohen, R.; Elek, N.; Chang, H.-H.; Malik, B.H.; Gabay, R.; Jones, R.; Paniccia, M.; et al. Double-Stage Taper for Coupling Between SOI Waveguides and Single-Mode Fiber. *J. Light. Technol.* **2008**, *26*, 3860–3865. [CrossRef]
8. Kohtoku, M.; Hirono, T.; Oku, S.; Kadota, Y.; Shibata, Y.; Yoshikuni, Y. Control of Higher Order Leaky Modes in Deep-Ridge Waveguides and Application to Low-Crosstalk Arrayed Waveguide Gratings. *J. Light. Technol.* **2004**, *22*, 499–508. [CrossRef]
9. Dai, D.; Tang, Y.; Bowers, J.E. Mode Conversion in Tapered Submicron Silicon Ridge Optical Waveguides. *Opt. Express* **2012**, *20*, 13425–13439. [CrossRef] [PubMed]
10. Zhao, Y.; Qiu, C.; Wu, A.; Huang, H.; Li, J.; Sheng, Z.; Li, W.; Wang, X.; Gan, F. Broadband Polarization Splitter-Rotator and the Application in WDM Receiver. *IEEE Photonics J.* **2019**, *11*, 1–10. [CrossRef]
11. Sacher, W.D.; Barwicz, T.; Taylor, B.J.F.; Poon, J.K.S. Polarization Rotator-Splitters in Standard Active Silicon Photonics Platforms. *Opt. Express* **2014**, *22*, 3777–3786. [CrossRef]
12. Guan, H.; Ma, Y.; Shi, R.; Novack, A.; Tao, J.; Fang, Q.; Lim, A.E.-J.; Lo, G.-Q.; Baehr-Jones, T.; Hochberg, M. Ultracompact Silicon-on-Insulator Polarization Rotator for Polarization-Diversified Circuits. *Opt. Lett.* **2014**, *39*, 4703–4706. [CrossRef]
13. Wang, J.; Lee, C.; Niu, B.; Huang, H.; Li, Y.; Li, M.; Chen, X.; Sheng, Z.; Wu, A.; Li, W.; et al. A Silicon-on-Insulator Polarization Diversity Scheme in the Mid-Infrared. *Opt. Express* **2015**, *23*, 15029–15037. [CrossRef] [PubMed]
14. Yin, Y.; Li, Z.; Dai, D. Ultra-Broadband Polarization Splitter-Rotator Based on the Mode Evolution in a Dual-Core Adiabatic Taper. *J. Light. Technol.* **2017**, *35*, 2227–2233. [CrossRef]
15. Xu, H.; Shi, Y. Ultra-Broadband Silicon Polarization Splitter-Rotator Based on the Multi-Mode Waveguide. *Opt. Express* **2017**, *25*, 18485–18491. [CrossRef] [PubMed]
16. Ding, Y.; Ou, H.; Peucheret, C. Wideband Polarization Splitter and Rotator with Large Fabrication Tolerance and Simple Fabrication Process. *Opt. Lett.* **2013**, *38*, 1227–1229. [CrossRef]
17. Socci, L.; Sorianello, V.; Romagnoli, M. 300 Nm Bandwidth Adiabatic SOI Polarization Splitter-Rotators Exploiting Continuous Symmetry Breaking. *Opt. Express* **2015**, *23*, 19261–19271. [CrossRef] [PubMed]

18. Wang, J.; Qi, M.; Xuan, Y.; Huang, H.; Li, Y.; Li, M.; Chen, X.; Jia, Q.; Sheng, Z.; Wu, A.; et al. Proposal for Fabrication-Tolerant SOI Polarization Splitter-Rotator Based on Cascaded MMI Couplers and an Assisted Bi-Level Taper. *Opt. Express* **2014**, *22*, 27869–27879. [CrossRef]

19. Wang, J.; Niu, B.; Sheng, Z.; Wu, A.; Li, W.; Wang, X.; Zou, S.; Qi, M.; Gan, F. Novel Ultra-Broadband Polarization Splitter-Rotator Based on Mode-Evolution Tapers and a Mode-Sorting Asymmetric Y-Junction. *Opt. Express* **2014**, *22*, 13565–13571. [CrossRef]

20. Guo, J.; Zhao, Y. Analysis of Mode Hybridization in Tapered Waveguides. *IEEE Photonics Technol. Lett.* **2015**, *27*, 2441–2444. [CrossRef]

21. Guan, H.; Fang, Q.; Lo, G.; Bergman, K. High-Efficiency Biwavelength Polarization Splitter-Rotator on the SOI Platform. *IEEE Photonics Technol. Lett.* **2015**, *27*, 518–521. [CrossRef]

22. Tu, X.; Li, M.; Xing, J.; Fu, H.; Geng, D. Compact PSR Based on an Asymmetric Bi-Level Lateral Taper in an Adiabatic Directional Coupler. *J. Light. Technol.* **2016**, *34*, 985–991. [CrossRef]

23. Dai, D.; Wu, H. Realization of a Compact Polarization Splitter-Rotator on Silicon. *Opt. Lett.* **2016**, *41*, 2346–2349. [CrossRef] [PubMed]

24. Ma, M.; Park, A.H.K.; Wang, Y.; Shoman, H.; Zhang, F.; Jaeger, N.A.F.; Chrostowski, L. Sub-Wavelength Grating-Assisted Polarization Splitter-Rotators for Silicon-on-Insulator Platforms. *Opt. Express* **2019**, *27*, 17581–17591. [CrossRef] [PubMed]

25. Fukuda, H.; Yamada, K.; Tsuchizawa, T.; Watanabe, T.; Shinojima, H.; Itabashi, S. Silicon Photonic Circuit with Polarization Diversity. *Opt. Express* **2008**, *16*, 4872–4880. [CrossRef] [PubMed]

26. Velha, P.; Sorianello, V.; Preite, M.V.; Angelis, G.D.; Cassese, T.; Bianchi, A.; Testa, F.; Romagnoli, M. Wide-Band Polarization Controller for Si Photonic Integrated Circuits. *Opt. Lett.* **2016**, *41*, 5656–5659. [CrossRef] [PubMed]

27. Deng, H.; Yevick, D.O.; Brooks, C.; Jessop, P.E. Design Rules for Slanted-Angle Polarization Rotators. *J. Light. Technol.* **2005**, *23*, 432.

28. Bayat, K.; Chaudhuri, S.K.; Safavi-Naeini, S. Ultra-Compact Photonic Crystal Based Polarization Rotator. *Opt. Express* **2009**, *17*, 7145–7158. [CrossRef] [PubMed]

29. Dai, D.; Zhang, M. Mode Hybridization and Conversion in Silicon-on-Insulator Nanowires with Angled Sidewalls. *Opt. Express* **2015**, *23*, 32452–32464. [CrossRef] [PubMed]

30. NanoSOI Fabrication Service | Applied Nanotools Inc. Available online: https://www.appliednt.com/nanosoi-fabrication-service/ (accessed on 14 January 2021).

31. Cornerstone MPW. Available online: https://www.cornerstone.sotonfab.co.uk/about-us/cornerstone (accessed on 15 January 2021).

32. Tang, Y.; Chen, H.-W.; Jain, S.; Peters, J.D.; Westergren, U.; Bowers, J.E. 50 Gb/s Hybrid Silicon Traveling-Wave Electroabsorption Modulator. *Opt. Express* **2011**, *19*, 5811–5816. [CrossRef]

33. Boyraz, O.; Jalali, B. Demonstration of a Silicon Raman Laser. *Opt. Express* **2004**, *12*, 5269–5273. [CrossRef]

34. Li, C.; Zhou, L.; Poon, A.W. Silicon Microring Carrier-Injection-Based Modulators/Switches with Tunable Extinction Ratios and OR-Logic Switching by Using Waveguide Cross-Coupling. *Opt. Express* **2007**, *15*, 5069–5076. [CrossRef]

35. Xu, Q.; Schmidt, B.; Pradhan, S.; Lipson, M. Micrometre-Scale Silicon Electro-Optic Modulator. *Nature* **2005**, *435*, 325–327. [CrossRef] [PubMed]

36. Xu, D.; Schmid, J.H.; Reed, G.T.; Mashanovich, G.Z.; Thomson, D.J.; Nedeljkovic, M.; Chen, X.; Thourhout, D.V.; Keyvaninia, S.; Selvaraja, S.K. Silicon Photonic Integration Platform—Have We Found the Sweet Spot? *IEEE J. Sel. Top. Quantum Electron.* **2014**, *20*, 189–205. [CrossRef]

37. Tran, M.A.; Huang, D.; Komljenovic, T.; Peters, J.; Malik, A.; Bowers, J.E. Ultra-Low-Loss Silicon Waveguides for Heterogeneously Integrated Silicon/III-V Photonics. *Appl. Sci.* **2018**, *8*, 1139. [CrossRef]