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Review

In-Plane Monolithic Integration of Scaled III-V Photonic Devices

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Abstract: It is a long-standing goal to leverage silicon photonics through the combination of a low-cost advanced silicon platform with III-V-based active gain material. The monolithic integration of the III-V material is ultimately desirable for scalable integrated circuits but inherently challenging due to the large lattice and thermal mismatch with Si. Here, we briefly review different approaches to monolithic III-V integration while focusing on discussing the results achieved using an integration technique called template-assisted selective epitaxy (TASE), which provides some unique opportunities compared to existing state-of-the-art approaches. This method relies on the selective replacement of a prepatterned silicon structure with III-V material and thereby achieves the self-aligned in-plane monolithic integration of III-Vs on silicon. In our group, we have realized several embodiments of TASE for different applications; here, we will focus specifically on in-plane integrated photonic structures due to the ease with which these can be coupled to SOI waveguides and the inherent in-plane doping orientation, which is beneficial to waveguide-coupled architectures. In particular, we will discuss light emitters based on hybrid III-V/Si photonic crystal structures and high-speed InGaAs detectors, both covering the entire telecom wavelength spectral range. This opens a new path towards the realization of fully integrated, densely packed, and scalable photonic integrated circuits.

Keywords: integrated photonics; silicon-on-insulator; III-V on silicon; hybrid photonic crystals

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1. Introduction

The integration of III-Vs on silicon is a long-standing goal because it would allow us to combine the attractive features of a low-cost, highly developed, and complex silicon platform with the added functionality of active photonic devices such as light sources and detectors. On one hand, there is mature Si technology which benefits from strong light confinement due to a high refractive index contrast between Si and SiO_2 and from highly optimized low-roughness etch technologies. Consequently, this has led to the demonstration of high-speed and low-loss passives [1,2]. On the other hand, there are the III-V-based semiconductors which, due to their direct bandgap, allow for efficient light emission in the near-IR, where Si is transparent. Furthermore, the ability to tune the bandgap by changing the composition allows for the creation of heterostructures and quantum wells, which are essential parts of advanced semiconductor laser designs. Combining these materials directly is challenging, since they are not lattice-matched and have different thermal expansion coefficients and polarities. Thus, growing a planar sheet of III-V on top of silicon typically results in a poor material quality.

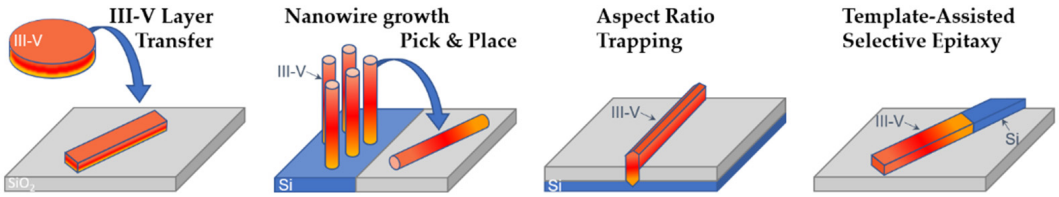
The most common method for advanced integrated photonic applications is the direct-wafer bonding of a III-V wafer or individual III-V components on top of a Si wafer [3–6]. This allows to grow the appropriate stack of III-V material lattice matched on a III-V carrier wafer, which may subsequently be recycled. It is of special interest for adding active components to silicon photonics, as this also allows to transfer high-quality III-V

material onto a pre-patterned silicon or SOI wafer containing passive silicon features [1,7–9], thereby creating hybrid photonic components; at IBM, we are also actively exploring this technique for use in advanced photonic devices [10]. Similarly, stacked devices have also been fabricated by transfer-printing the devices fabricated on the III-V substrate onto a Si photonics chip [11,12]. Light then couples evanescently between the two layers, from the silicon waveguides to the bonded III-V active material or vice versa, depending on whether the application is emission or detection.

For densely integrated photonic circuits foreseeing thousands of individual links, a seamless and local monolithic integration of III-V material is highly desirable. Vertical III-V nanowires (NWs) on silicon have been realized by selective-area growth through metal organic chemical vapor deposition (MOCVD), where the III-V material is grown out of an oxide mask [13,14] or by extending device designs to nanowire arrays [15,16]. However, the typical vertical orientation of the NWs makes the large-scale integration and electrical actuation of more advanced devices challenging. While the planar growth of NWs has been demonstrated [17–19], it is yet to be successfully implemented for photonic applications. Instead, NW pick-and-place techniques have been used successfully to demonstrate high-performance proof-of-concept devices by placing a III-V nanowire within a resonant cavity for either emission [20] or detection [21].

Aspect ratio trapping (ART) is another epitaxial technique which allows for the use of high-quality material in a horizontal device [22,23]. Here, the propagation of defects after growth nucleation is terminated in one direction within an oxide trench. Nano-ridge lasers were fabricated by this method in [23–26], but further development is necessary for implementing arbitrary geometries and doping profiles.

An overview of the above fabrication methods is presented in Figure 1 with a focus on the integration scheme with Si and the III-V growth direction, which defines the inherent orientation of heterostructures or doping profiles and therefore is a determinant for the device architecture. For example, vertical-cavity surface-emitting lasers (VCSELs) are some of the most scaled and high-performance on-chip lasers, but they inherently emit out of plane and are therefore less suitable for waveguide integrated designs. We note that the desirable in-plane or lateral doping profile for the placement of electrical contact can be implemented for all the above methods in additional steps, either through the consecutive regrowth of III-V material on both sides or by ion implantation. This is the case for lateral-current-injection architectures [27] and might be suitable for the implementation of *p*- and *n*-regions for contacting and carrier injection or extraction.



Integration	Wafer-scale	Single device	Wafer-scale	Wafer-scale
Shape	By design	Nanowire	Fin-like	By design
Growth direction	Vertical	Lateral (axial) or radial	Vertical	Lateral

Figure 1. Schematic comparison for several integration methods for III-Vs (red) on Si (blue) and SiO_2 (grey). Color shading symbolizes the growth direction and thereby natural orientation of heterostructures or doping profiles.

In this work, we will discuss the local integration of III-Vs self-aligned with silicon features using template-assisted selective epitaxy (TASE) [28,29]. This technique was originally developed for electronic applications [30] and has more recently been extended to photonics [29,31–33], where it enables the growth of complex nanostructures. We have explored several embodiments depending on the desired device geometry and applications.

The in-plane TASE epitaxial growth extends along the surface of the wafer and may include in situ doping profiles or hetero-junctions [34,35] oriented along the growth direction, perpendicular to the wafer surface (see Figure 1). This represents a fundamental difference to bonded devices which rely on the planar growth of different layers with composition and doping profiles in the vertical direction. Another distinguishing feature is that the III-V materials are grown such that they replace a silicon feature. This makes it self-aligned through a one-step lithographic process. This high degree of control allows us to place contacts accurately on the scaled devices and to create hybrid structures with silicon and III-V features.

Here, we present our latest work on in-plane TASE growth on an SOI wafer, as this is most suitable for applications targeting the direct coupling to silicon waveguides and other passive silicon photonic features, and therefore highly promising for the realization of photonic integrated circuits (PICs). We will review and discuss the method as applied to these structures and additionally show previously unpublished work relating to InP-based hybrid III-V/Si photonic crystal emitters which highlight the benefits of locally placing gain material.

2. Template-Assisted Selective Epitaxy

A simplified schematic of TASE is shown exemplarily for a nanorod structure in Figure 2. The process is indeed not limited to this simple shape but has, amongst others, been applied to achieve micro-disks [31] or crossbar structures [28,36]. The starting point of TASE is a Si structure patterned by standard Si processing techniques—i.e., in our case, e-beam lithography and HBr dry etching. Here, we use a standard SOI wafer, as it provides the ideal optical isolation of the photonic devices in the top layer from the Si substrate and allows for seamless integration with Si passive structures in the same layer. The etched Si structure is encapsulated in ~200 nm SiO_2 by a combination of atomic layer deposition (ALD) and plasma-enhanced chemical vapor deposition (PECVD). Subsequently, a window is etched into this oxide layer at one or more locations of the patterned Si, whereby the Si is locally exposed again, as shown in Figure 2b. This allows us to partially remove the Si from one side with a well-controlled tetramethylammonium hydroxide (TMAH) wet etch. The resulting hollow oxide template with a remaining Si seed is depicted in Figure 2c. During the MOCVD growth step, the III-V material will nucleate on this Si seed and then continue to fill the SiO_2 template (d), adapting to its shape. By changing the precursor flow during growth or adding doping species, one may change the composition and/or the background doping either abruptly or gradually in situ during growth. This allows for the creation of in-plane heterojunctions or quantum wells orthogonal to the substrate orientation with a high-quality material interface, which is generally challenging in other techniques.

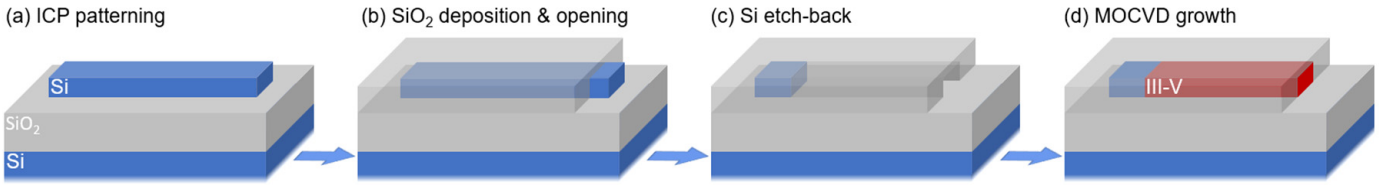


Figure 2. Schematic of TASE process flow. (**a**) Patterning of a SOI wafer by standard lithographic methods and Si patterning processes. (**b**) Deposition of an oxide layer (SiO_2) which covers the Si structure. A window is etched into the SiO_2 layer to expose one end of the underlying Si. (**c**) The Si structure is partially etched back using TMAH, leaving a hollow template behind and exposing a small Si nucleation seed at one extremity. (**d**) MOCVD growth of the III-V material into this template, nucleating on the Si seed.

In the following, two different devices will be used to illustrate the specific advantages of in-plane TASE growth for integrated photonics. Firstly, we will discuss its application to III-V/Si hybrid photonic crystal cavities, focusing on different device optimization steps;

secondly, we will illustrate the extension to electrically actuated devices with the example of an in-plane monolithic photodetector.

3. Hybrid III-V/Si Photonic Crystal Cavity Lasers

Photonic crystal (PhC) cavities have been explored extensively, as they have proven to be ideal candidates for the realization of high modulation rates and low-threshold laser operation [37–39]. This is mainly due to their very high quality (Q)-factors (>10^6) and small modal volume, where cavity mode volumes approaching the diffraction limit have been widely reported [3,40]. In a 2D cavity, this mode volume is significantly smaller than the entire structure. Thus, it was proven to be beneficial to also confine the gain region to the central cavity and thereby achieve a high overlap with the cavity mode, additionally avoiding undesired absorption outside of the main cavity region. In references [37,41], the local placement of gain in a 2D PhC cavity was realized with the use of buried heterostructures. Similarly, in Ref. [20] a 2D Si PhC structure is used with the active material in the form of a III-V nanowire placed in the central cavity.

Recently, our group demonstrated a novel concept for a one-dimensional hybrid III-V/Si PhC cavity, where we exploit TASE to replace the central parts of a Si PhC structure fabricated on SOI with III-V active materials [33]. This has several advantages: (1) it optimizes the overlap of the optical mode with the active gain material; (2) optical losses are reduced due to a lower absorption in Si; and (3) unlike the other approaches [20,37,41], it is self-aligned to the silicon mirror features.

In the following, we present first the design and fabrication of such hybrid III-V/Si PhC cavities. Then, we explore the impact of the hybrid nature of the cavity, as it is made up of two different materials: silicon and the III-V gain material.

3.1. Design and Fabrication

The 1D PhC structure consists of evenly spaced nanorods made from a high refractive index material such as Si or III-Vs and embedded in SiO_2. The length of the nanorods w_y is quadratically tapered towards the center of the device to form the cavity according to $w_y(i) = w_y(0) + i^2\ (w_y(i_{max}) - w_y(0))/{i_{max}}^2$, where i is the nanorod position. This design is adapted from Ref. [42] and thus highlights how TASE is able to leverage existing and well-optimized PhC cavity designs from the Si photonics community. Additionally, it is well suited for in-plane coupling to SOI waveguides, as required for future integration within PICs.

As each rod is individually addressable, it is possible to replace any number of rods with III-V materials, just as it is also possible to replace non-neighboring rods, while leaving the remaining rods in the original silicon. We choose the central rods here in order to achieve a high overlap between the first cavity mode field profile, which is localized in the center of the device, and the gain material.

The device resulting from replacing the central Si rods with III-V material is shown in the top-view scanning electron microscopy (SEM) image in Figure 3a, where the III-Vs appear in a brighter color than Si. Two other features can be observed in this SEM as a result of the TASE process: first, the oxide opening from where the Si was etched back; second, the remaining Si seeds at which the III-V growth nucleated. The remaining part of the PhC cavity is untouched by the process, benefitting from the high side-wall quality of the Si processing. A different refractive index of the two materials can be compensated for by adjusting the III-V rod width. Indeed, finite difference time domain (FDTD) simulations show that Q factors and resonance wavelengths comparable to the Si-only design can be achieved [33].

The $|E_y|^2$ field intensity profile of the fundamental cavity mode obtained from 3D FDTD simulations (Lumerical) is shown in Figure 3b. Comparing this mode profile with the position of the III-V rods in the SEM above showcases the high overlap between cavity mode and gain material as intended.

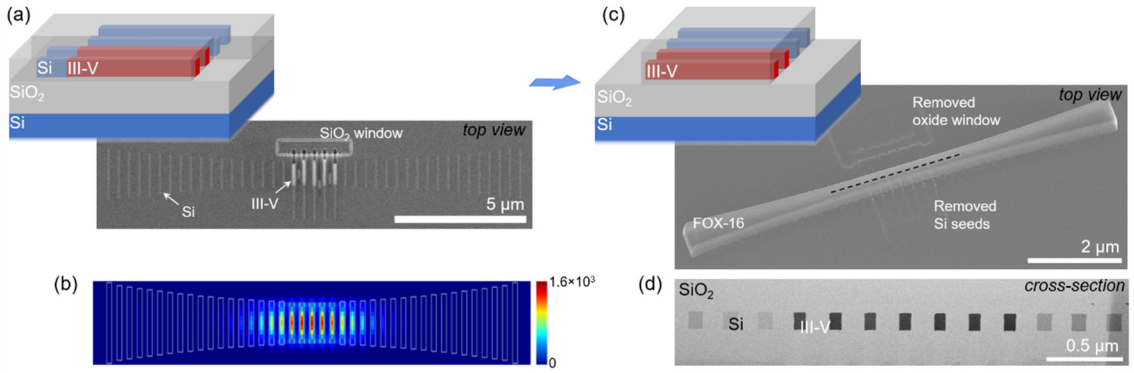


Figure 3. Fabrication of the hybrid III-V/Si photonic crystal cavities. (**a**) Schematic of the device center where some Si rods were replaced with active material. This is visible in the SEM top view (top), where the III-V material appears in a brighter color. (**b**) 3D FDTD simulated $|E_y|^2$ field profile of the fundamental mode. A comparison with (**a**) emphasizes the high gain overlap of the selected five rods with the cavity mode. (**c**) In an additional step, a symmetric cavity is achieved by defining the device outline with FOX-16 resist and removing the surrounding oxide. The resulting structure is visible in the SEM image with the cavity hidden underneath. (**d**) A STEM cross-section along the dashed line shows that the III-V rods directly inherit the Si shape. (**a**,**b**) are reprinted (adapted) with permission from [33] © 2020 American Chemical Society.

The cavity center with the oxide windows and non-uniform III-V rods on one side and the Si seed on the other side disturbs the symmetry needed for a high-Q PhC cavity. The fact that we very consistently observe cavity modes at expected peak positions and featuring similar experimental Q-factors on the order of 1000 is encouraging. This can also partially be attributed to the lateral heterojunctions implemented in [33], which help to confine the carriers in the nanorod center and thus away from the Si seed.

In order to further optimize this, a symmetric device can be achieved by removing the absorbing Si seed nanowires which extend beyond the structures. We realize this by patterning a 500 nm-thick FOX-16 resist to cover a hybrid III-V/Si PhC structure. By electron beam lithography, the resist is cured and it obtains a composition and refractive index similar to silicon oxide. A non-selective Ar-ion milling etch then removes both the Si seed and the slightly irregularly grown III-V rods in a single step, resulting in the symmetric device sketched in Figure 3c. In the corresponding SEM image, the individual rods of the PhC cavity are not visible underneath the oxide bar, but the outline of the cavity is clear. The shapes from the Si seeds and the oxide window are still recognizable but smoothed out, as they are transferred into the BOX layer below the cavity level, in the former case because of the slower etch rate of Si in the ion milling process.

The scanning transmission electron microscope (STEM) cross-sectional image in Figure 3d highlights the self-aligned position of the embedded III-V rods within the hybrid PhC cavity. The smooth and straight side walls of both the III-V and Si rods are due to the mature Si processing technology using HBr, whereas the etching of III-V stacks, especially when it includes different compositions, generally results in greater surface roughness, which impacts the final device performance.

3.2. Characterization of Hybrid III-V/Si PhC Cavities

The PhC cavities are characterized by micro-photoluminescence (µ-PL) spectroscopy at 100, 130, and 150 K for indium phosphide (InP)-based and room temperature for indium gallium arsenide (InGaAs)-based devices. A picosecond-pulsed supercontinuum laser at a pump wavelength of 750 nm (InP) or 850 nm (InGaAs) is focused onto the device by a 100× objective (NA = 0.6). The emission is collected with the same objective and analyzed by a spectrometer with a cooled InGaAs detector, using a filter which removes the pump signal.

First, we characterize hybrid III-V/Si PhC cavities with InGaAs as a gain material. Figure 4a shows the measured PL spectra for cavities with different PhC lattice constants. By tailoring this PhC parameter (lattice constant a = 325–390 nm, height h = 220 nm, rod width $w_x = 0.3a$, outer rod length $w_y = 5a$), we control the resonant wavelength which in

total covers the entire telecom bands. The measured wavelength of the modes fits well with simulated values, also depicted by the shaded area. An uncertainty when comparing simulated and experimental results arises from the refractive index of our grown III-V materials, which we estimate to lie in the range of n = 3.2–3.5, whereas the Si refractive index ranges from n = 3.46 to n = 3.61 for wavelengths of 1550 nm and 900 nm, respectively [43].

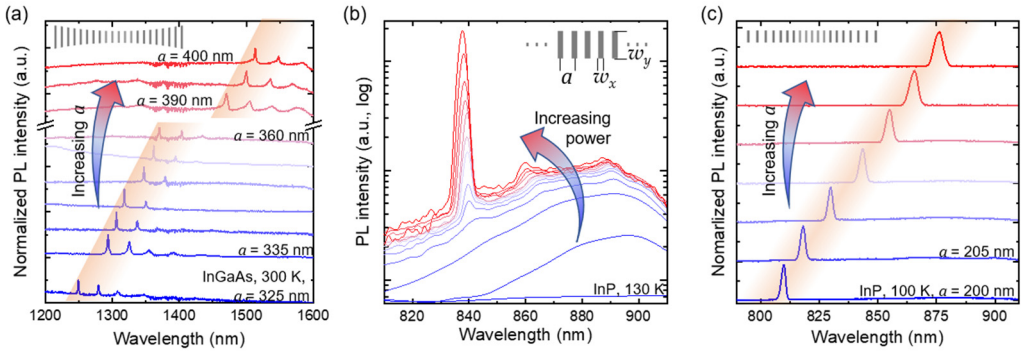


Figure 4. (**a**) Emission spectra for hybrid InGaAs/Si PhC cavities with different lattices measured at room temperature. The cavity design is displayed in the inset. Simulated emission wavelengths for each PhC cavity are marked by a shaded area due to an uncertainty on the refractive index of III-Vs. Reprinted and adapted with permission from [33] © 2020 American Chemical Society. (**b**) PL intensity for a hybrid InP/Si PhC cavity under increased optical pumping at 130 K in logarithmic scale, showing the emergence of a resonant mode at higher pump powers. (**c**) Emission wavelength dependency of InP-based cavities with a slightly different cavity design and for regularly increasing lattice constant, measured at 100 K.

It is remarkable that all the measured devices behave similarly despite the non-uniform length of the grown InGaAs rods, as seen in Figure 3a. We believe this further proves the benefit from introducing III-V material locally in the center of the device. This region where the symmetry of the PhC is disturbed only takes up a small part of the entire device, whereas a large part remains Si. Here, is it appropriate to mention that the non-uniform length of the III-V rods in the PhC structures is not intrinsic to TASE technology, past work on electronic devices showed uniform lengths of III-V features also when grown in large arrays. Recently, oxygen contamination of our reactor has led to some variation in the nucleation efficiency, which translates into a variation of total length. This affected those works, but has since been remedied.

A similar study is performed on devices with InP as the gain material [33], as shown in Figure 4b,c. The PhC parameters for this material was adjusted for resonant emission within the InP gain bandwidth. Additionally, these PhC cavities possess a slightly different geometry since the adiabatic tapering is realized by quadratically modulating the lattice constant outwards from the cavity center according to $a(i) = a(0) + i^2\,(a(i_{\max}) - a(0))/{i_{\max}}^2$.

Figure 4b shows the PL intensity under increasing pump power for a PhC cavity (a = 215 nm, h = 120 nm, $w_x = 0.5a$, $w_y = 2.5a$) with seven InP rods in the center measured at 130 K. At low pump intensity, the spontaneous emission from InP, centered around 900 nm, is visible. Upon increasing pump power, a peak appears at 835 nm and continues to increase in intensity. This peak corresponds to the fundamental cavity mode. Additionally, higher order modes are faintly visible in the spectra taken with high pump power.

The emission spectra for hybrid devices with InP as the gain material are plotted in Figure 4c for increasing lattice constant. Resonant modes are visible in each of these spectra as well, shifting to longer wavelengths with increasing lattice constant in good agreement with simulations. Here, the different cavities also cover the entire gain bandwidth between 800 nm and 900 nm.

While the combination of InGaAs with an emission wavelength in the telecom range together with the low Si absorption is desirable, we can still learn from hybrid devices with InP as gain material, especially because of the additional absorption from Si rods outside of the central cavity. InP provides material gain centered around a wavelength of 900 nm, which corresponds to an energy greater than the Si bandgap. The Si part of the PhC cavity

then not only does not provide material gain but also absorbs light as it is reflected in the PhC mirror.

A quantitative comparison of light absorption can be found in Figure 5a, where the wavelength dependence of the absorption coefficient is displayed (data taken from [44]). Considering an emission wavelength of 900 nm, the absorption coefficient of Si is two orders of magnitude lower than for InP. The emission of InGaAs predominantly lies above the Si absorption edge, i.e., in the wavelength range where Si is transparent.

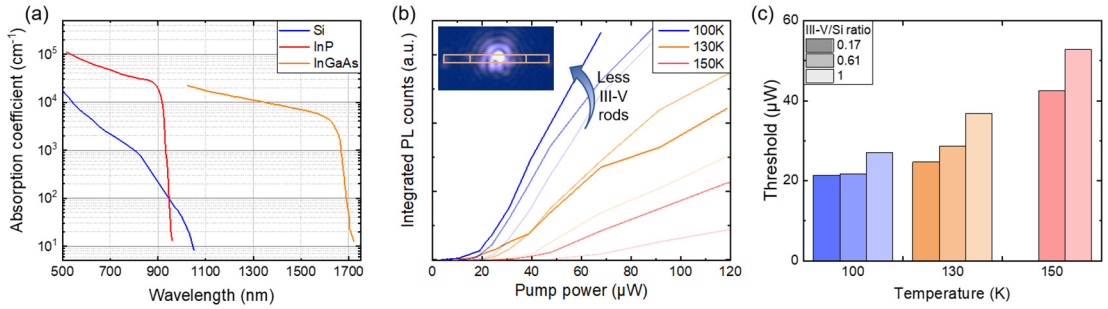


Figure 5. (**a**) Absorption coefficient of Si, InP, and InGaAs [44]. At 900 nm, the absorption coefficient of InP is two orders of magnitude larger than for Si. (**b**) Light in-light out curves for hybrid InP/Si cavities measured at different temperatures (line color) and for different numbers of Si rods in the PhC mirror (color intensity). The inset shows the far-field emission pattern above threshold. (**c**) Lasing threshold of typical devices with increasing ratio of III-V/Si rods, where 0 corresponds to all Si and 1 to all InP; in all cases, the total number of rods is 41. The threshold increases with the temperature and III-V/Si ratio.

In our setup, only the central part of the PhC cavity is pumped, and the spot-size of the pump source is about 1 μm in width. The pump-light might also be reflected within the PhC cavity, but for regions increasingly removed from the center of the structure, the III-V material is expected to contribute more loss than gain.

We investigate whether there is a correlation between device performance, in terms of emission peak intensity versus input power, and the number of III-V rods in the cavity center. For the same number of total rods (n = 41) in the cavity, an increase in the number of III-V rods relates to a larger proportion of III-V compared to Si rods. This ratio between III-V and Si rods will be used as metric in the following. While the cavity resonance wavelength and Q factor can be recovered for a different III-V/Si ratio by adjusting the rod width, the device properties directly depend on the amount of light absorption. This allows us to compare different devices with a varying number of III-V rods in the cavity center.

In Figure 5b, hybrid InP/Si devices which possess an emission wavelength of 840 nm are optically excited with increasing power and the integrated PL intensity is displayed. These light in-light out (LL) curves are measured at different temperatures and with different InP/Si rods ratio. The kink visible in the LL curve corresponds to the onset of stimulated emission in the cavity mode. However, we note that this alone is not sufficient proof of lasing, but we use it here as a basis for comparing different devices. As expected, the efficiency decreases with a higher temperature, as the slopes of the curves indicate. Additionally, a trend is visible for the three different InP/Si ratios, where the curve is shifted to lower pump power for the cavity with fewer InP rods. Figure 5c emphasizes this behavior by considering only the lasing threshold, which we extract from the LL curves at the x-axis intersection of the linear slope. A higher temperature leads to a larger threshold, as marked by the different colors. Additionally, the threshold increases with the fraction of InP rods to Si rods in the cavity. The absorption of light in the PhC mirror part of the cavity evidently plays an important role and the threshold is lower since Si is less absorptive than InP, even though it does not contribute to the gain. Thus, we benefit from being able to place the gain material only in the part of the cavity with a large overlap to the desired resonant mode, and which can be efficiently pumped.

We show these results for three different temperatures, but cannot achieve lasing in the InP-based devices above a temperature of 150 K. Going to room temperature operation,

a different material with emission above the Si band edge is necessary to eliminate the contribution of absorption losses in the mirrors. A natural choice is $In_{0.5}Ga_{0.5}As$ as it is lattice matched to InP. The InGaAs of course will also absorb, but we only keep it in the cavity center where it can be efficiently pumped.

Indeed, we already saw this effect on devices with InGaAs as a gain material in Figure 4c, as these measurements were performed at room temperature, for which the spectra of similar InP devices did not show any cavity modes. A direct comparison between the devices with different gain material is not possible because of their different design and different emission wavelength, for which also the pump laser wavelength was adjusted.

The lack of absorption from the mirrors might not fully explain the gain in performance. The InGaAs-based devices do not contain a uniform $In_{0.5}Ga_{0.5}As$ profile, but it is sandwiched between two InP regions which possess a larger bandgap energy. Together with the in situ *p*- and *n*-type doping of the two InP regions, respectively, a wide potential-well like structure is formed which might improve the carrier confinement. Additionally, a *p*-type doped InGaAs is added to the *p*-type InP to reduce the contact resistance in future design, but this should not impact the performance of the present devices.

Whereas the PhC structures are currently based on optical pumping, we are investigating a path towards electrical actuation. For this, the aforementioned *n*-InP/*i*-InGaAs/*p*-InP/*p*-InGaAs nanorods already contain an appropriate materials profile.

4. Monolithic Detectors

TASE is equally well suited to realize efficient III-V-based detectors which lie in-plane with Si waveguides. Together with emitters, these are the main components needed to obtain a full optical link. Recently, electrical functionality for monolithic $In_{50}Ga_{50}As$ detectors [34] was demonstrated using the same TASE technique, which is shown in Figure 6. In this work the focus was on small form-factor devices for low-capacitance high-speed performance. We grew the III-V active region using the same method as for the emitters, but this time the height was only 60 nm. This means that, although the devices are coupled directly to a silicon nanowire, it is too thin to support a propagating mode and the metal contacts on top will induce absorption losses. In future designs, interfacing the *i*-region of the photodetector directly with a Si waveguide perpendicular to it might prove beneficial. Here, the responsivity and bandwidth measurements were performed through free space coupling from an optical fiber.

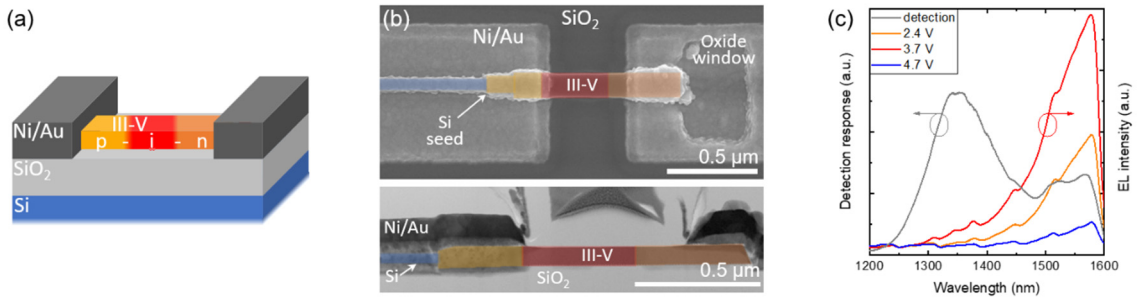


Figure 6. (**a**) The last step in addition to the process flow in Figure 1 consists of depositing Ni/Au contacts. The grown III-V material for this device is a *p*-*i*-*n* heterostructure, as indicated in (**b**) by the false-colored top-view SEM and cross-sectional TEM. The Si seed for growth nucleation is clearly visible underneath the deposited contact. (**c**) Spectral response of the monolithic InGaAs photodetector in reverse bias (detection) and forward bias (emission), on different scales. (**b**,**c**) are adapted with permission from [34].

The 1 µm-long devices contain an in situ *p*-*i*-*n*-doping profile with an intrinsic absorption region of roughly 300 nm length, as pointed out in the SEM and STEM in Figure 6b. If we consider that only the *i*-region contributes to the absorption, we calculate a responsivity up to 0.65 A/W (2 V reverse bias) depending on the operating conditions. This is the ideal case and should be considered as an upper limit. The devices show relatively low dark

currents in the range of a few A/cm^2 and a strong RF response, whereby the measured f3dB > 25 GHz is limited by our setup.

We observed a rather non-linear spectral response with peaks in the O- and C-band, as shown in Figure 6c. In particular, the strong peak in absorption at 1350 nm is somewhat surprising based on the 50% In content. Extensive simulations carried out in Synopsys Sentaurus by collaborators at the Swiss Federal Institute of Technology (ETH) in Zurich showed this to be a result of the scaled geometry and device architecture. This results in the reflections at the various film interfaces as well as at the contact edges and illustrates an important point about nanoscale photonic devices—namely, that such effects might dominate device performance in minute geometries, as compared to conventional bulk-like devices. Thus, nanoscale effects need to be considered in the device design so that it might be turned to an advantage. This is the case here, where these reflections cause an amplification of the response in the important region for datacom around 1350 nm.

We also evaluated the operation of those devices under forward bias for light emission. The electroluminescence is further in the near-IR spectral region, so we are only able to observe the tails around 1600 nm in our setup.

5. Conclusions

In this work, we first provided a brief introduction to different monolithic III-V on Si integration techniques, with a focus on the TASE technique developed by our group. We presented in-plane integrated photonic devices which make use of the benefits of the innovative TASE platform. This represents an extension to our electronic devices for which we originally developed these techniques, but we exploit the same underlying technique for the integration of in-plane homo- and heterojunctions. We believe that this opens up new opportunities for co-integration between active and passive elements. In particular, the ability to integrate III-Vs locally on silicon and within silicon features in a self-aligned manner enables novel paradigms for device design. In this way, we can exploit silicon for what it does best—ease of processing and low optical losses in the NIR for transmission and passives—while adding the III-V only and exactly where we need it.

For an integrated platform, electrical and not optical actuation should be the goal. We have demonstrated electroluminescence for the forward-biased *p-i-n* detectors, which contain the same materials as the so far optically pumped PhC cavities. In fact, both emitters and detectors can be fabricated in the same step with TASE. With the added gain material within a PhC cavity, we show a path towards efficient and tailorable light emitters, covering the entire telecom bands. Additionally, the ability to play around with optical loss and gain at will as well as mixing different III-Vs on the same wafer will also allow for making more exotic devices—for example, exploiting topological effects [45,46].

Author Contributions: All the authors created the device concepts, where H.S. and K.E.M. have led the initial development of TASE. M.S., N.V.T., S.M., P.T. fabricated the samples supported by H.S. for MOCVD growth. M.S. and N.V.T. performed FDTD simulations. M.S., N.V.T., S.M., P.T. characterized the samples and analyzed data. N.V.T. and K.E.M. led the projects. M.S. and K.E.M. prepared the original draft, all the authors contributed to this manuscript. All authors have read and agreed to the published version of the manuscript.

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