

Article

All-Optical Non-Inverted Parity Generator and Checker Based on Semiconductor Optical Amplifiers

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Abstract: An all-optical non-inverted parity generator and checker based on semiconductor optical amplifiers (SOAs) are proposed with four-wave mixing (FWM) and cross-gain modulation (XGM) non-linear effects. A 2-bit parity generator and checker using by exclusive NOR (XNOR) and exclusive OR (XOR) gates are implemented by first SOA and second SOA with 10 Gb/s return-to-zero (RZ) code, respectively. The parity and check bits are provided by adjusting the center wavelength of the tunable optical bandpass filter (TOBPF). A saturable absorber (SA) is used to reduce the negative effect of small signal clock (Clk) probe light to improve extinction ratio (ER) and optical signal-to-noise ratio (OSNR). For Pe and Ce (even parity bit and even check bit) without Clk probe light, ER and OSNR still maintain good performance because of the amplified effect of SOA. For Po (odd parity bit), ER and OSNR are improved to 1 dB difference for the original value. For Co (odd check bit), ER is deteriorated by 4 dB without SA, while OSNR is deteriorated by 12 dB. ER and OSNR are improved by about 2 dB for the original value with the SA. This design has the advantages of simple structure and great integration capability and low cost.

Keywords: all-optical parity generator; all-optical parity checker; semiconductor optical amplifier; all-optical signal processing; all-optical XOR logic; all-optical XNOR logic



Citation: Han, B.; Xu, J.; Chen, P.; Guo, R.; Gu, Y.; Ning, Y.; Liu, Y. All-Optical Non-Inverted Parity Generator and Checker Based on Semiconductor Optical Amplifiers. *Appl. Sci.* **2021**, *11*, 1499. <https://doi.org/10.3390/app11041499>

Academic Editor: Kyriakos E. Zoiros

Received: 29 December 2020

Accepted: 3 February 2021

Published: 7 February 2021

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1. Introduction

To solve the problem of data transmission in the future communication network, all-optical signal processing (AOSP) [1] technology with larger capacity, better flexibility, and good scalability has attracted more and more attention. Due to the invention of low-loss optical fiber [2] and Erbium-doped fiber amplifier (EDFA) [3], it has good progress in data transmission over long distances (thousands of kilometers). As the data transmission capacity, speed, and distance requirements of optical fiber networks increase, there has been an increasing interest in all-optical signal codes, and it has become a key technology for optical communications and optical networks in the future. However, long-distance transmission would cause data added, deleted, and flipped errors. If the error is not discovered and handled in time, it will lead to the wrong transmission of information and cause various negative effects. In order to detect coding errors, the most common solution is parity. In the parity checker circuit, the integrity of the data is verified by successive operations on the binary data. The parity bits are added before data transmission by the

parity generator, and the parity checker is used at the receiving end to check whether there are errors and noise during the data transmission.

The principle of the parity checker circuit is to check the total number of “1” codes in the data, so the summation properties of the XNOR gate and XOR can be used. If it does not match the initial setting (the number of “1” codes in the even parity checker is odd, the number of “1” codes in the odd parity checker is even), the parity check circuit will output an error signal. In recent studies, people have implemented the all-optical parity generator and checker circuit in various ways; for example, parity checker based on terahertz optical asymmetric demultiplexer interferometers [4], the parity generator and checker using semiconductor optical amplifiers (SOAs) based on Mach–Zehnder interference [5–10], parity generator and checker based on the microring cavity, parity generator and checker using an SOA-assisted optical tree architecture [11], parity generator and checker based on SOA-assisted Sagnac switches [12]. Due to the integration of potential and good non-linear characteristics of semiconductor optical amplifiers, people have a strong research interest. There are extensive studies in all-optical signal processing and all-optical calculations, such as switches, clocked flip-flops [13], logic gates [14–18], subtractor and adder [19–22], decoder/encoder [20,23], and comparator [23,24]. It can be seen from the research of various all-optical technologies that semiconductor optical amplifiers have broad application prospects in future optical communication systems.

In this paper, we present an all-optical non-inverted 2-bits parity generator based on a single SOA and checker based on dual SOAs. It can check 2-bit data errors occur during the 2-bits (A and B) optical signal transmission. The device utilizes the cross-gain modulation (XGM) effect and the four-wave mixing (FWM) effect of the SOA. By adjusting the center wavelength of the tunable optical band-pass filter (TOBPF) to realize different logic gates, which provide parity and check bits for the all-optical parity generator and checker. It can check whether there are errors in the data during the signal light transmission process and completes the operation in the 10 Gb/s pseudo-random return-to-zero (RZ) codes. A saturable absorber (SA) is configured to reduce extinction ratio (ER) and optical signal-to-noise ratio (OSNR) deterioration because of “0” codes noise and amplified noise of small signal Clk probe light. In this article, the experimental principles of the parity generator and parity checker are discussed in Section 2. In Section 3, the experiment results of parity bit penetrator and checker are discussed. The conclusion is given in Section 4.

2. Principle

The all-optical non-inverted parity generator and checker based on SOAs is shown in Figure 1. From the principle of the optical generator and checker circuit, we found that it can be composed of XOR [14–16] and XNOR [17,18] gate, the dotted line section, and the entire working in Figure 1 correspond to the parity generator and checker, respectively.

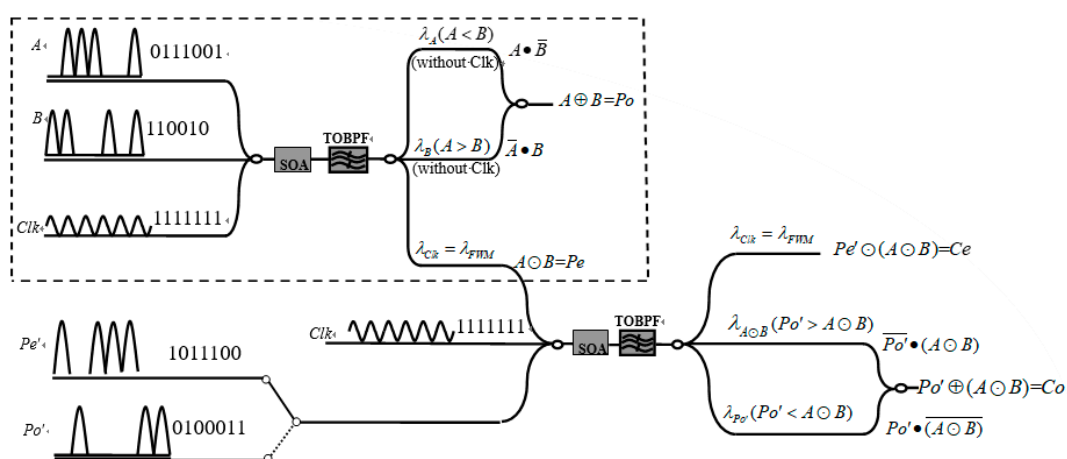


Figure 1. Principle of the all-optical non-inverted parity generator and checker based on semiconductor optical amplifiers (SOAs) (\oplus and \odot are the symbolic representation of exclusive OR (XOR) and exclusive NOR (XNOR), respectively).

To verify whether there are errors or noise interference during the binary data transmitted from the sending end to the receiving end, the parity checker is applied to the sending end and receiving end of the data transmission to detect whether an error occurs (0 changed 1, 1 changed 0). On the one hand, the parity bit (0 or 1) is added to the data bit at the sending end so that total number of “1” codes is odd or even in the added data bit. On the other hand, the receiving end counts the number of “1” codes in the received data. If the total number of “1” codes is odd, it is called odd parity. On the contrary, it is called even parity. In odd or even parity, if the number of “1” codes are even or odd in the received data, it means that error has occurred.

2.1. Parity Generator

As shown parity generator in Figure 1, to generator an odd/even parity bit, the two data bits are added using XOR and XNOR gate, the parity bits Pe and Po are obtained, where Pe is the even parity bit, Po is the odd parity bit, and the expressions are, respectively,

$$Pe = A \oplus B \quad (1)$$

$$Po = \overline{A \oplus B} \quad (2)$$

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The 2-bit parity generator circuit can simultaneously generate parity bits Pe and Po using a single SOA. Compared with the scheme with a control circuit (control the parity generator to be odd or even), we achieve the expected purpose and make the circuit structure more compact, easier to integrate.

As shown in Table 1, for all the truth of A , B , and Pe in each row and the total number of “1” codes is even when the even parity generator is working. Similarly, for all the truth of A , B , and Po in each row and the total number of “1” codes is odd when the odd parity generator is working. Parity bits Pe and Po of parity generator for the inputs $A = [0111001]$ and $B = [1100101]$ are shown in Table 1.

Table 1. Truth table of parity generator.

A	B	Pe	Po
0	1	1	0
1	1	0	1
1	0	1	0
1	0	1	0
0	1	1	0
0	0	0	1
1	1	0	1

2.2. Parity Checker

As shown in parity checker in Figure 1, 2-bit parity checker is implemented with SOAs and the outputs are parity check bits. In order to realize a 2-bit parity checker, the redesign formula is as follows:

$$Ce = Pe' \oplus (A \oplus B) = Pe' \odot (A \odot B) \quad (3)$$

$$Co = \overline{Po' \oplus (A \oplus B)} = Po' \oplus (A \odot B) \quad (4)$$

where the even check bit is C_e which is generated using the XOR gate of the second SOA. The odd check bit is C_o which is generated using the XNOR gate of the second SOA. This formula can also achieve the expected purpose by checking the truth table. At the same time, it avoids the instability caused by too many lights of different wavelengths under the XGM effect in the XOR logic. This solution can make the design more compact, more stable, and easier to implement into integrated circuits.

The Pe' and Po' (same as Pe and Po in the parity generator) are applied to the parity checker. When the optical switch (OSW) selects Pe' , the even parity check bit output will be obtained. When the optical switch selects Po' , it gets an odd parity check bit. According to the properties of XOR or XNOR summation of the number of "1" codes, the conclusion can be clearly shown: if the parity checker output result is 0, it means that the received data is completely correct; if the parity checker output result is "1", it means that the data has an error or noise during transmission. The truth table of the parity checker has been given in Tables 2 and 3, we consider all possible logical combinations of A and B .

Table 2. Truth table of even parity checker.

A	B	Pe'	C_e	Result
0	1	1	0	Error
1	1	0	0	
0	0	1	1	
1	1	1	1	
0	1	1	0	Error
0	0	0	0	
1	1	0	0	

Table 3. Truth table of odd parity checker.

A	B	Po'	C_o	Result
0	1	0	0	Error
1	1	1	0	
0	0	0	1	
1	1	0	1	
0	1	0	0	Error
0	0	1	0	
1	1	1	0	

The Principles of XOR and XNOR gates based on SOA implementation:

A and B are two signal lights which wavelengths are λ_A and λ_B , while the Clk light is the wavelength of λ_{clk} with 50 ps RZ pulse. When signal light A and B are injected in SOA, gain, and phase modulation of Clk light is performed. All-optical logic gates are obtained by switching the center wavelength of TOBPF. Table 1 is the corresponding logical truth value.

The realization principle of different logic function are as follows:

XNOR: Due to the FWM and XGM effects, the output is different under different code type combinations. When data A and B both are "1" code, the output is "1" code due to FWM in the SOA. Meanwhile, the relationship between the wavelength of idle light generated by FWM and the wavelength of the clock detection light is $\lambda_{clk} = \lambda_{FWM}$. Due to the XGM, when data A and B both are 0 and 1 codes (1 and 0 codes), the output is 0 (1) code when small signal probe light is magnified, respectively. When data A and B both are "0" code, the output is "1" code due to small probe light is magnified.

XOR: When the peak powers of the two wavelengths are different, the low-power wavelength is modulated by the XGM effect of the high-power wavelength. A is modulated to achieve $A \bullet \bar{B}$ when the center wavelength of the TOBPF is λ_A . Conversely, B is modulated to achieve $\bar{A} \bullet B$ when the center wavelength of TOBPF is λ_B . $A \bullet \bar{B}$ and $\bar{A} \bullet B$ are output together to realize XOR logic gate.

To realize the logic gate $Co (Po' \oplus (A \odot B))$ in the parity checker, it is necessary to reconfigure the power and wavelength, EVOA1 and EVOA2 are used to control the power and optical delay line (ODL) (after the EDFA7) is used to control the timing of the output of logic gates $\overline{Po'} \bullet (A \odot B)$ and $Po' \bullet (A \odot B)$ to realize the logic gate $Po' \oplus (A \odot B)$. EVOA1, EVOA2, and ODL are controlled by the personal computer to adjust their parameters.

3. Experimental Result and Discussion

The experimental scheme of all-optical non-inverted parity generator and checker are presented in Figure 2.

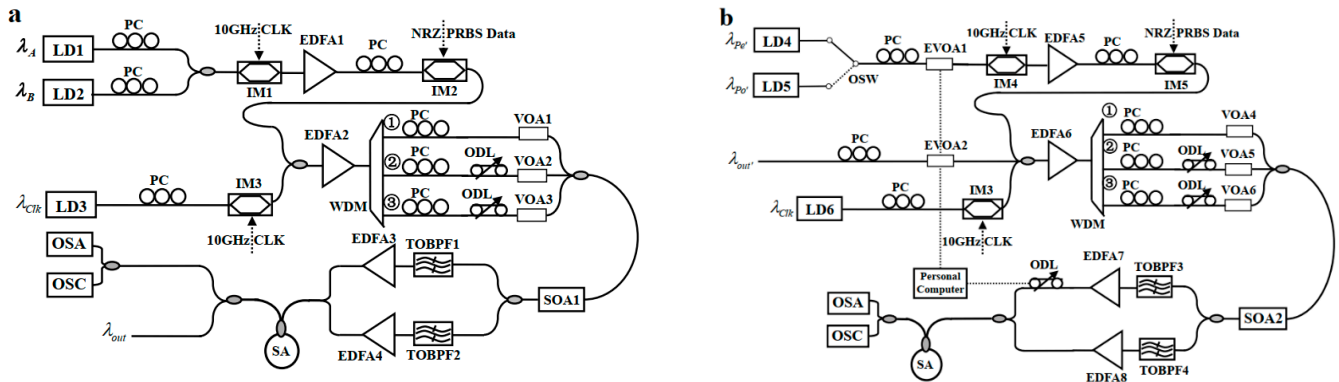


Figure 2. The experimental setup of all-optical non-inverted parity generator (a) and checker (b) (PC polarization controller, EVOA electrical variable optical attenuator, IM intensity modulator, CLK electronic clock, ODL optical delay line, VOA variable optical attenuator, TOBPF tunable optical band pass filter, WDM wavelength division multiplexer, SMF single-mode fiber, EDFA erbium-doped fiber amplifier, OSW optical switch, SA saturable absorber).

The parity generator is shown in Figure 2a, the three inputs include signal light A , B , and probe light Clk . The polarization state is adjusted by polarization controller (PC). The 10 GHz optical Clk pulse modulated by the intensity modulator 1 (IM1) and amplified by erbium-doped fiber amplifier (EDFA), then it modulated as 10 Gbit/s pseudo-random code sequence (PRBS) of 27-1 length by IM2. In the same way, the probe light Clk enters the wave-decomposition multiplexer (WDM) together with PRBS light after PC and IM2 through a 50:50 optical coupler. It is divided into 3 channels for modulation respectively. Among them, PC controls the polarization state, ODL controls the relative delay, and variable optical attenuator (VOA) adjusts the optical power. The three light waves include (1) light A , 1550.9 nm wavelength with data code “0111001”, (2) light B , 1551.7 nm wavelength with data code “1100101”, and (3) the probe light with data code “1111111”. After, they are injected into SOA1, using the FWM effect and XGM effect of SOA1 and the center wavelength through the tunable optical band pass filter (TOBPF) with 0.26 nm narrow band is selected, the output results Pe and Po are obtained, as shown in Figure 2b the parity checker is used as a parity bit for verification.

The circuit of the parity checker is shown in Figure 2b. The input λ_{out} is connected with the output $\lambda_{out'}$ of the parity generator, so the parity generator can be realized by the extension of the parity generator. Pe' and Po' is the output of the parity generator. Use an optical switch as a selector to control the output of the parity checker (Ce or Co). The OSC (oscilloscope: Agilent-86100A) and OSA (optical spectrum analyzer: Agilent-86142B) are used to observe the signal waveform and spectra of the output of the logic gate, respectively. The main device parameters are given: the bias current of SOA is 300 mA. The maximum power of EDFA is 20 dBm. The bandwidth of TOBPF is 0.26 nm. The adjustable attenuation range of VOA is from 1.5 dB to 25 dB. The maximum delay of the optical delay line is 660 ps. The SA consists of a 3 dB coupler and a 5 m erbium-doped fiber. The experimental parameter settings of all logic gates are shown in Table 4.

Table 4. Experimental parameters with logic gates (P: power with dBm unit; W: wavelength with nm unit; ER: extinction ratio with dB unit; OSNR: optical signal to noise ratio with dB unit).

Signal	A			B			CLK		TOBPF	Result
Logic	P	W	ER/OSNR	P	W	ER/OSNR	P	W	W	ER/OSNR
\bar{A}	−2.5	1550.9	11.92/14.95	×	×	×	−27	1552.5	1552.5	11.75/14.02
\bar{B}	×	×	×	−2.5	1551.7	11.82/12.53	−27	1552.5	1552.5	11.52/11.83
$A \odot B$	2	1550.9	12.96/13.82	0	1551.7	12.04/12.98	−27	1552.5	1552.5	11.02/11.88
$\bar{A} \bullet B$	−2.7	1550.9	11.34/15.6	−9	1551.7	5.17/6.81	×	×	1551.7	11.24/6.47
$A \bullet \bar{B}$	−9	1550.9	5.17/6.81	−2.7	1551.7	11.34/15.6	×	×	1550.9	11.21/6.43
$Pe' \odot (A \odot B)$	2	1550.9	12.96/13.82	0	1551.7	12.04/12.98	−27	1552.5	1552.5	8.03/9.46
$\bar{Po}' \bullet (A \odot B)$	−2.7	1550.9	11.34/15.6	−9	1551.7	5.17/6.81	×	×	1551.7	8.36/4.67
$Po' \bullet (\bar{A} \odot \bar{B})$	−9	1550.9	5.17/6.81	−2.7	1551.7	11.34/15.6	×	×	1550.9	8.31/4.59

The inputs, odd, and even parity bits are shown in Figure 3. The outputs are verified with the truth table shown in Table 1. For Po and Co , XGM and FWM are used in the parity checker which are shown in Figure 3c.

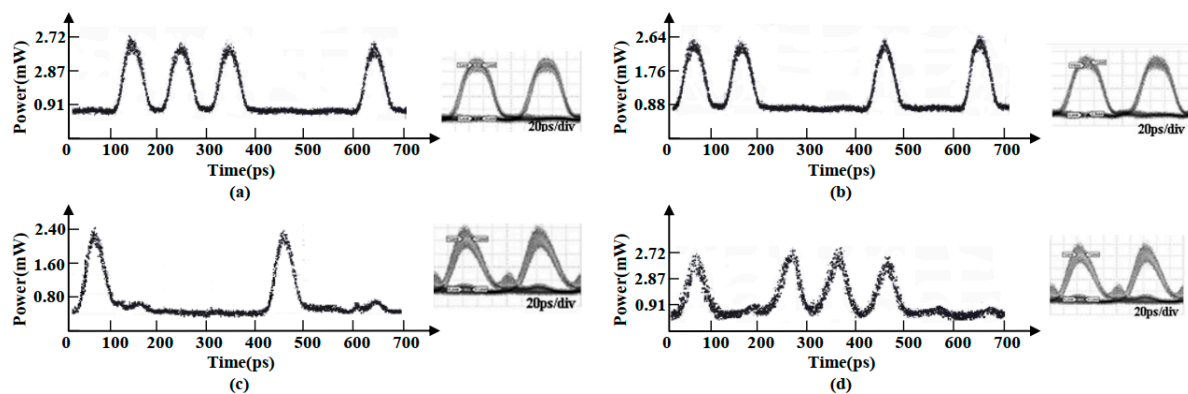


Figure 3. Wave from all-optical non-inverted parity generator (a) optical signal pulse train A, (b) optical signal pulse train B, (c) the odd parity bit output, (d) the even parity bit output.

When errors have occurred in the data received by the parity checker, suppose $A = [0101001]$ and $B = [1101101]$, the experimental results of the parity checker are shown in the Figure 4, the check bit output is “1” to indicate that the received data is incorrect. If the received data A and B are correct, the output result of the parity checker should be “0”.

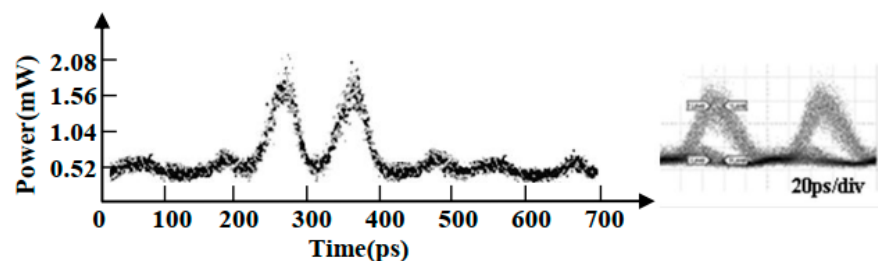


Figure 4. The output result of the all-optical parity checker with errors.

ER and OSNR are analyzed to observe the performance of the device more intuitively. We found that ER and OSNR of the parity checker are only 4–6 dB due to the application of dual SOAs. To improve the performance of the device, a SA with 5 m unpumped erbium-doped fiber is used to reduce deterioration. In realizing the Po of the parity generator, ER and OSNR are both improved to 1 dB difference for the original value with the SA. For the Co of the parity checker without the SA, ER and OSNR are both deteriorated by about 4 dB and 12 dB respectively because of amplified noise of small signal “1” code, ER and

OSNR are improved to about 2 dB difference for the original value with the SA. For the implementation of the Pe and Ce , they keep the good performance by the amplified effect of SOA.

This solution uses continuous wave (CW) as the probe light which can balance the power relationship of each light and keep the power constant, and avoid the XGM effect caused by carrier concentration changed in the active region when multiple lights incident on the SOA at the same time. Meanwhile, we need to keep the clock and signal dynamics consistent during the experiment.

4. Conclusions

A new kind of 2-bit all-optical non-inverted parity generator and parity checker is proposed with FWM and WGM effect of SOA, where the parity generator and checker are realized by SOAs, which enhances the integratability, configurability, and extensibility of the circuit. The experimental results confirm the feasibility of the scheme and measure the ER and OSNR for every output. The ER and OSNR can show the stability of the system very well in the entire transmission process. The results show that a SA is configured which has a certain improvement effect on ER and OSNR of the parity generator and checker. ER and OSNR of the parity checker are only reduced by 3 dB and 2 dB respectively which are compared with the parity generator. The scheme uses only dual SOAs to implement the parity generator and checker which have the potential to achieve more bits of parity and realize further complex logic functions.

Author Contributions: Conceptualization and methodology, B.H. and J.X.; writing—original draft preparation, P.C.; validation, R.G.; software, Y.G., and Y.N.; writing—review and editing, project administration and funding acquisition, Y.L.; All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded in part by the National Science Fund for Distinguished Young Scholars under grant number 61705157 and 61805167, in part by the National Nature Science Foundation of China grant number 61975142 and 61475112, in part by the Research Project Supported Shanxi Scholarship Council of China grant number 2017-key-2, in part by the Project funded by China Postdoctoral Science Foundation, in part by the Research Project Supported by Shanxi Scholarship Council of China grant number 2020-112, and in part by the Key Research and Development (R&D) Projects of Shanxi Province grant number 201903D121124.

Data Availability Statement: The data presented in this study are available on request from the corresponding author. The data are not publicly available due to confidentiality.

Conflicts of Interest: The authors declare no conflict of interest.

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