



# Article Switched Low-Noise Amplifier Using Gyrator-Based Matching Network for TD-LTE/LTE-U/Mid-Band 5G and WLAN Applications

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**Abstract:** This paper presents a triple-band low-noise amplifier (LNA) fabricated using a 0.18 μm Complementary Metal-Oxide-Semiconductor (CMOS) process. The LNA uses a double-peak load network with a switched component to accomplish the triple-band operation. Moreover, noise reduction using a substrate resistor to ameliorate the noise performance is presented. Noise reduction of 1.5 dB can be achieved at 2.5 GHz without additional dc power and extra manufacturing costs. An input matching technique is realized simultaneously using a gyrator-based feedback topology. The triple-band LNA can be realized by using a dual-band input network with a switched matching mechanism. The target frequencies of the triple-band LNA are 2.3–2.7 GHz, 3.4–3.8 GHz, and 5.1–5.9 GHz, covering the operating frequency bands of time-division long-term evolution (TD-LTE), mid-band Fifth-generation (5G), LTE-unlicensed (LTE-U) band, and Wireless LAN (WLAN) technology. The measured power gains and noise figures at 2.5, 3.5, and 5.2 GHz are 12.3, 15.3, and 13.1 dB and 2.3, 2.2, and 2.6 dB, respectively.

Keywords: low-noise amplifier; 5G; triple-band; noise reduction

## 1. Introduction

Fourth-generation (4G) systems, such as time division duplexing (TDD) long-term evolution (TD-LTE), for mobile telecommunication have advanced highly. At present, the major TD-LTE frequency bands are 2.3 GHz (Band 40), 2.6 GHz (Band 41), and 3.5 GHz (Bands 42 and 43) [1]. To further boost the performance of LTE and provide faster and more secure mobile services, using LTE-unlicensed (LTE-U) band in the unlicensed 5-GHz spectrum with a cost-effective method is considered a favorable solution for achieving a larger bandwidth [2]. To further increase the traffic capacity, 5G communication technology has been proposed, and the Radio Spectrum Policy Group (RSPG) adopts the 3.6 GHz band for 5G communication in Europe [3,4].

IEEE 802.11ac, with an operating frequency of 5 GHz, has been dubbed and specified as a Wi-Fi standard that is three times faster than IEEE 802.11n. Therefore, several coexistence schemes have been developed to allow efficient and fair spectrum sharing between LTE-U and WLAN [5–7]. WLAN standards [8] (IEEE 802.11a/b/g/n/ac) cover 2.4 and 5 GHz frequency bands, and different countries usually adopt different frequency bands for the limited bandwidth. Thus, highly integrated radio-frequency integrated circuits with multiple bands are becoming critical for use in TD-LTE, LTE-U, 5G, and WLAN applications. Moreover, owing to increasing demands of these new frequency bands in practical applications, compatibility with 2-, 3-, and 5-GHz bands operation has become challenging for low-noise amplifier (LNA) designers.

Conventional design strategies for multiband communication have adopted different single-band transceiver circuits in parallel for achieving different frequency bands [9,10];



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**Copyright:** © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). however, this has increased the implementation cost and current dissipation. To overcome the aforementioned drawbacks, topologies of wideband LNA have been designed and demonstrated for multiband applications [11,12]. The broadband gain response causes undesired interference, thereby impairing the linearity of the receiver. A dual-resonant transformer-based matching network was analyzed and capable of two different frequencies [13], but a dual-band operation is insufficient to cover the latest triple-band wireless standard.

Furthermore, a lossy silicon substrate lowers the quality factor of the spiral inductor, which limits the reliability of the LNA. Several papers have proposed methods for ameliorating the noise of LNAs. A flipped CMOS glass-integrated-passive-device (GIPD) package [14] and inductively coupled plasma (ICP) deep-trench technology [15] were utilized to improve the quality factor of off-chip and on-chip inductors. However, the extra processes of CMOS GIPD flip-chips and ICP created excessive costs of package and production.

To achieve a wide range of wireless communication services, with up to 400, 400, and 800 MHz bandwidths from 2.3–2.7, 3.4–3.8, and 5.1–5.9 GHz bands, respectively, which include TD-LTE Band 40–41, Band 42–43, and the unlicensed 5-GHz band operation, with miniaturized circuit size, and less than 3 dB noise targeted for each band, we proposed a triple-band LNA that employs a switched narrow-band double-peak load matching mechanism to operate on triple-band and avoid unwanted interference, and decrease power consumption for multiband transceiver application. The input matching of the LNA is adopted by gyrator-based feedback topology to minimize the circuit size. Moreover, a noise cancellation technique with additional substrate resistor is presented to enhance noise figure performance.

The rest of this paper is organized as follows. Section 2 introduces the design principle and analysis of the matching network and noise reduction technique used in this switched LNA. Section 3 details the triple-band LNA. The experimental results and conclusions are summarized in Sections 4 and 5, respectively.

#### 2. Circuit Design and Analysis

The proposed LNA was designed based on the operating frequencies of TD-LTE, midband 5G, LTE-U, and IEEE 802.11 a/b/g/n/ac standards. To achieve high compatibility, Band 40 and Band 41 range from 2.3 to 2.4 GHz and 2.5 to 2.7 GHz, respectively. Band 42 and Band 43 range from 3.4 to 3.6 GHz and 3.6 to 3.8 GHz, respectively [16]. Moreover, 3.4–3.8 GHz is also the range for mid-band 5G communications for the EU licensed band [17]. The shared 5-GHz LTE-U band ranges from 5.150 to 5.925 GHz [2]. Furthermore, WLAN (IEEE 802.11a/b/g/n/ac) covers a frequency range of 2.4–2.5 and 5.1–5.9 GHz. Therefore, the target bands are the operating frequencies covering 2.3–2.7, 3.4–3.8, and 5.1–5.9 GHz for TD-LTE/LTE-U and WLAN applications.

#### 2.1. Proposed Switched-Resonator Triple-Band Load Network

We designed an LNA that utilizes a double-peak single-notch network with a switch as the load impedance to have the same characteristics of the input network. The schematic of a load network controlled by a switched transistor  $M_{sw1}$  is shown in Figure 1a. The simplified single-band and dual-band network are shown in Figure 1b,c, respectively. The single-band load impedance  $Z_{L_{sw}(off)}$  is simplified to an LC tank operated at  $\omega_3 = 3.5$  GHz when the switch is off. Similarly, when the switch is on, the dual-band load impedance  $Z_{L_{sw}(on)}$  operated at  $\omega_1 = 2.5$  GHz and  $\omega_2 = 5.2$  GHz is chosen. The load impedance  $Z_{L_{sw}(on)}$  and  $Z_{L_{sw}(off)}$  can be expressed as shown in Equations (1) and (2), respectively:

$$Z_{L_{sw}(on)} = \frac{j\omega L_d (1 - \omega^2 L_1 C_1)}{\omega^4 L_d C_d L_1 C_1 - \omega^2 (L_d C_d + L_1 C_1 + L_d C_1) + 1},$$
(1)

$$Z_{L_{sw(off)}} = \frac{-j\omega L_d}{\omega^2 L_d C_d - 1}$$
(2)





**Figure 1.** Schematic of the load network. (**a**) The proposed triple-band load network with an additional switched component, (**b**) single-band network, (**c**) and dual-band network.

Equation (1) shows that the two poles  $\omega_1$  and  $\omega_2$  and one zero  $Z_{L_sw(on)}$  can be obtained by letting the denominator equal null.  $\omega_1$  and  $\omega_2$  can be written as

$$\omega_1^2, \omega_2^2 = \frac{L_1 C_1 + L_d C_d + L_d C_1}{2L_1 C_1 L_d C_d} \pm \frac{\sqrt{(L_1 C_1 + L_d C_d + L_d C_1)^2 - 4L_1 C_1 L_d C_d}}{2L_1 C_1 L_d C_d}$$
(3)

and  $\omega_{z_{sw(on)}}$  can be written as

$$\omega_{z\_sw(on)} = \frac{1}{\sqrt{L_1 C_1}} \tag{4}$$

From Equation (2),  $\omega_{p_{sw}(off)}$  can be written as

$$\omega_{p\_sw(off)} = \frac{1}{\sqrt{L_d C_d}} = \omega_3 \tag{5}$$

The proposed triple-band load network has three given target frequencies for the four load components, implying that there is one degree of freedom, say  $C_d$ , left for the circuit design. Figure 2 shows the load impedance versus frequency with different  $C_d$  parameters. As shown in Figure 2a, the dual-band network provides double-peak amplitudes of load impedance when the switch is on. Figure 2b shows the load impedance of a single-band network when the switch is off.

In general, the first step in the design criteria of the proposed load network is to select a lower  $C_d$  on account of the higher load impedance (i.e., the LNA gain). However, a drawback of the design is the high implementation cost due to the requirement of large inductance  $L_1$  and  $L_d$ . Therefore, the trade-off between the gain and die area should be considered [18].



**Figure 2.** Load impedance versus frequency with different  $C_d$  parameters. (a) A dual-band load network when the switch is on. (b) A single-band load network when the switch is off.

# 2.2. Conventional Gyrator-Based Active Inductor and Proposed Gyrator-Based Triple-Band Input Matching Network

The conventional gyrator-based active inductor [18] is shown in Figure 3a. Transistors  $M_1-M_3$  were employed to establish a back-to-back transconductor stage, where  $M_1$  is a common-drain stage, functioning as the feedback element, and  $M_2-M_3$  comprise a cascode stage, which is the gain element. The transistor  $M_3$  is used as a gain booster. The inductive impedance in the Smith chart and the equivalent circuit comprising an inductor, capacitor, and resistor are shown in Figure 3b,c, respectively. The gyrator-based circuit topology can be simplified as shown in Figure 3d. In the proposed input matching network, the gyrator topology comprises a feedback ( $G_{m1}$ ) and feedforward gain ( $G_{m2}$ ) element to convert the capacitive impedance into inductive impedance. The impedance can be changed from capacitive  $C_x$  to inductive  $L_{in}$  [19] and can be derived as

$$I_{in} = G_{m2} \left( G_{m1} V_{in} \times \frac{1}{sC_X} \right)$$
(6)

and

$$Z_{\rm in} = \frac{V_{\rm in}}{I_{\rm in}} = \frac{sC_X}{G_{m1} \times G_{m2}} = sL_{in} \tag{7}$$

In Equation (7),  $Z_{in}$  is with an inductive loading  $L_{in}$  with an inductance  $C_x/(G_{m1} \times G_{m2})$ . The proposed input matching network is presented with an additional switched resonator  $Z_{L_sw}$  between point X and  $V_{dd}$ . Therefore, we added a resonator  $Z_{L_sw}$  parallel to the capacitor  $C_x$  (here,  $Z_c = 1/sC_x$ ), as shown in Figure 3e. The impedance  $Z_{in}$  can be written as

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{G_{m1} \times G_{m2}(Z_c || Z_{L_sw})}$$
(8)

 $Z_{in}$  will be an inductive loading with an inductance  $C_x/(G_{m1} \times G_{m2})$  if  $Z_{L_{sw}}$  is merely an open loading.

As shown in Figure 4a, with a gyrator-based design,  $Z_{in}$  can be inductive around the resonant frequency  $\omega_o$  when the switch of  $Z_{L\_sw}$  is off. Contrarily, the impedance at the output node X is capacitive when the operating frequency is far from the resonant frequency. When the switch of  $Z_{L\_sw}$  is on,  $Z_{L\_sw}$  is changed to a dual resonator loading, as shown in Figure 4b, with dual inductive points found at the resonated frequencies  $\omega_1$  and  $\omega_2$ . By contrast, the triple-band input matching network can be accomplished when the feedback mechanism is provided with the proposed switched resonator.



**Figure 3.** Conventional and proposed gyrator-based topology. (a) Schematic of regulated cascode active inductor, (b) Smith chart, (c) equivalent circuit, (d) circuit topology and input impedance, (e) proposed gyrator-based circuit topology and its impedance with a switched resonator  $Z_{L_{SW}}$ .



(a)

Figure 4. Cont.



**Figure 4.** Principle of the input matching technique. (**a**) Smith chart when the switch is off, (**b**) Smith chart when the switch is on.

# 2.3. Noise Reduction with Large Substrate Resistance

Because the receiver sensitivity is determined by the thermal noise floor at input, the noise figure (NF) of the receiver, and the signal-to-noise ratio (SNR) requirement at the detector and NF of the receiver is dominated by the first stages of the receiver [20], a noise reduction technique with substrate resistor is applied to decrease the noise power of LNA.

As shown in Figure 5a,  $R_B$  is employed in an N-type Metal-Oxide-Semiconductor (NMOS) device to ameliorate the noise performance of the proposed CMOS LNA. The structure of a NMOS with  $R_B$  is shown in Figure 5b. The NF can be derived as [21]

$$NF = NF_{min} + \frac{G_n}{R_s} \times \left| Z_s - R_{opt} - jX_{opt} \right|^2$$
(9)

 $G_n$  and NF<sub>min</sub> can be written as

$$G_n = \frac{K_g \omega^2 C_{gs}^{\prime 2}}{g_m} \times \left(1 + \frac{R_d}{R_{ds}^{\prime} \parallel R_{sub}}\right)$$
(10)

and

$$NF_{min} = 1 + 2G_n \left( R_g + R_s + R_{opt} \right)$$
(11)



Figure 5. Cont.



**Figure 5.** Additional larger substrate resistance  $R_B$ . (a) A NMOS device with a larger substrate resistance  $R_B = 8 \text{ k}\Omega$ , (b) structure of a NMOS with  $R_B$ , (c) noise equivalent circuit of a NMOS device with  $R_B$ .

From (10) and (11), it can be observed that the increased resistance of the equivalent substrate resistor  $R_{sub}$  diminishes  $G_n$ , which in turn reduces the minimum noise figure NF<sub>min</sub>. Furthermore, the NF can also be reduced by reducing  $G_n$  and NF<sub>min</sub> in (9) [22]. Figure 6 presents the simulated noise factor *F* contributed by all MOSFET devices with and without  $R_B$ . Note that the simulated  $V_{SB}$  approaches zero, so the body-effect transconductance can be neglected [23].



**Figure 6.** Simulated RF MOSFET noise factor *F* (NF =  $10\log_{10} (1 + F)$ ) and noise reduction with and without *R*<sub>*B*</sub>.

A larger  $Z_{sub}$  by increasing the value of  $R_B$  results in the reduction of the noise factor. The noise factor *F* contributed by the MOS device is shown in Figure 6, and a considerable noise power reduction in the MOS device can be demonstrated by the additional resistance  $R_B$ . A maximum of 32% noise reduction can be achieved without requiring additional chip area and dc power because the size of the 8 k $\Omega$  High Resistance Implant (HRI) resistor is only 2 um × 15 um [22]. Figure 7 shows the simulation results of the noise figure with and without the additional resistance  $R_B$ . A decrease of 0.71/0.67/0.64 dB noise figure was achieved at 2.5/3.5/5.2 GHz due to the usage of the larger resistance  $R_B = 8$  k $\Omega$ .



**Figure 7.** Simulated noise figure with and without the additional resistance  $R_B = 8 \text{ k}\Omega$ . (a) Dual band when the switch is on, (b) single band when the switch is off.

#### 3. Proposed Switched Triple-Band LNA

To provide coverage for a wide range of wireless communication services, three spectrums will be covered with up to 400, 400, and 800 MHz from 2.3–2.7, 3.4–3.8, and 5.1–5.9 GHz, respectively, which include TD-LTE Band 40–41, Band 42–43, mid-band 5G, and the unlicensed 5-GHz band. To achieve 5 dB noise figure specifications [24], the 2 dB margin of the noise figure is appreciated when the effects of process, voltage, and temperature (PVT) variations can be estimated by simulation [25]. Consequently, the target noise figure of the proposed LNA is less than 3 dB with sufficient gain in 2-, 3-, and 5-GHz bands.

The triple-band LNA can reduce the chip area considerably by using a dual-band input network with an additional switched component. As shown in Figure 8, we designed the LNA to utilize a double-peak single-notch network with an additional switch as the load impedance to have the same characteristics of the input network. The additional resistance  $R_B$  was adopted to simultaneously accomplish noise power reduction. The transistor M<sub>5</sub> with a 50  $\Omega$  resistive load R<sub>1</sub> was employed to achieve output matching for testing purposes. A decrease of 0.71/0.67/0.64 dB in the noise figure was attained at 2.5/3.5/5.2 GHz due to the use of  $R_B$ .



**Figure 8.** The proposed triple-band low-noise amplifier (LNA) with the load network design and the noise reduction resistor, the component values  $R_{\rm B} = 8 \text{ k}\Omega$ ,  $R_{\rm g} = 5.2 \text{ k}\Omega$ ,  $R_1 = 50 \Omega$ ,  $C_1 = 588 \text{ fF}$ ,  $C_2 = 3.8 \text{ pF}$ ,  $C_3 = 3.8 \text{ pF}$ ,  $C_d = 388 \text{ fF}$ .

#### 4. Measurement Results

The LNA chip draws 7.9 mA dc core current from the 1.8 V supply voltage. The S parameters of the designed gain and input return loss are depicted in Figures 9 and 10. The measured power gains at 2.5/3.5/5.2 GHz were 12.3/15.3/13.1 dB, and the input return losses were more than 10 dB among the three operating frequencies. The noise figure was measured using Agilent N8975A noise figure analyzer with Agilent 346C noise source. The simulated and measured noise figures at the same bias condition are depicted in Figure 11. The measured noise figures at 2.5/3.5/5.2 GHz were 2.3/2.2/2.6 dB. The relation between the input third-order intercept point (IIP3) and the 1-dB compression points (P<sub>1dB</sub>) is shown as [24].

$$IIP_3 = P_{1dB} + 9.6 \, dB \tag{12}$$

The measured  $P_{1dB}$  are -15/-16/-17 dBm at 2.5/3.5/5.2 GHz, as shown in Figure 12, therefore, IIP3 could be calculated as -5.4/-6.4/-7.4 dBm.



Figure 9. Measured and simulated S-parameters (S21 and S11) of the proposed LNA.



Figure 10. Measured and simulated S-parameters (S<sub>22</sub> and S<sub>12</sub>) of the proposed LNA.



Figure 11. Measured and simulated noise figures of the proposed LNA.



**Figure 12.** The linearity  $(P_{1dB})$  of the proposed LNA.

The measurement results of the proposed LNA are summarized with recently published information in Table 1.

Ref.	Technology	Freq. (GHz)	G <sub>max</sub> (dB)	NF <sub>min</sub> (dB)	IIP <sub>3</sub> (dBm)	Power Consumption (mW)	FOM <sup>5</sup>	Area (mm <sup>2</sup> )
		2.4	14.4	3.3	-7.12			
[26]	0.18-µm	3.5	13	3.8	-6.2	7.2	1.66	0.63
		5.2 <sup>1</sup>	10	4.3	-4.34			
		2.4	22.1	2.8	-18.2			
[27]	0.13-µm	3.4	22.6	2.2	-15.3	4.6	6.01	0.49
		5.4 <sup>1</sup>	24.8	3.1	-20.4			
		2.8 <sup>2</sup>	16.1	2.4	-4			
[28]	0.13-µm	3.3	14.2	3.0	$^{-2}$	6.4	9.61	0.44
		5.65	14.9	4.8	-4.2			
		2.4			-12			
[29]	0.13-µm	3.5	15	2.7	-13.5	_ 6	_ 6	_ 6
		5.2			-13			
[30]	0.18-µm	2.4-11	14.8	4.1	-11.5	3.4	1.72	$1.1^{4}$
[22]	0.18-µm	2.3-4.8	27 <sup>3</sup>	2.7 <sup>3</sup>	$-3.2^{3}$	13.1	26	0.34
		2.5	12.3	2.3	-5.4			
This work	0.18-µm	3.5	15.3	2.2	-6.4	14.2	2.9	0.52
		5.2	13.1	2.7	-7.4			

Table 1. Performance summary of the published CMOS LNAs.

<sup>1</sup> 5 GHz band provides less than 800 MHz. <sup>2</sup> 2 GHz band lacks for time-division long-term evolution (TD-LTE) Band 40. <sup>3</sup> Simulation result. <sup>4</sup> Chip area is the largest in Table 1. <sup>5</sup> Only the best result for all operating bands is shown. <sup>6</sup> Full TRX design. IIP<sub>3</sub>: input third-order intercept point; FOM: figure of merit.

For performance comparison, the figure of merit (FOM) is defined by [31]:

$$FOM = \frac{Gain(abs) \times IIP3(mW) \times fc(GHz)}{(NF - 1)(abs) \times Powerconsumption(mW)}$$
(13)

Comparing the performance among the three operating frequencies, in terms of power gain, noise figure, and cost, the proposed switched triple-band LNA is the only one that can cover the whole target bands and provide the lowest  $NF_{min}$  with adequate power gain among 2-, 3-, and 5-GHz frequencies. The measured power consumption of the proposed design is slightly large due to the additional buffer amplifier stage for testing purposes. In this study, the circuit simulation was performed using Agilent's Advanced Design System (ADS) software with a TSMC design kit. In addition, the LNA is fabricated in an inexpensive 0.18- $\mu$ m CMOS process with a smaller chip-size, therefore, it has an advantage in terms of lower manufacturing cost.

## 5. Conclusions

The die microphotograph of the fabricated LNA and the corresponding transistors and inductor sizes are shown in Figure 13, with the die area including pads of  $0.75 \times 0.69$  mm<sup>2</sup>. The target frequencies of the proposed triple-band LNAs were 2.5, 3.5, and 5.2 GHz, which can be used in TD-LTE, mid-band 5G, LTE-U, and WLAN technology. A triple-band LNA with a switched resonator concept was fabricated using TSMC 0.18-µm CMOS technology, and a considerable die area reduction was achieved. Furthermore, an additional substrate resistance *R*<sub>B</sub> diminished the output noise power density of the MOS device, and a 0.71/0.67/0.64-dB decrease in the noise figure was attained at 2.5/3.5/5.2 GHz by using the triple-band LNA without additional chip area, dc power, and CMOS process steps. The frequency range for each band are 2.3–2.7, 3.4–3.8, and 5.1–5.9 GHz, including TD-LTE Band 40–41, Band 42–43, mid-band 5G, and the unlicensed 5-GHz band operation. The measured 10 dB return loss can be achieved to fulfil triple-band operation with moderate gain around 12 dB, and 2.2~2.7 dB noise figure. The measurement result agrees well with the simulation result.



**Figure 13.** Microphotograph of the proposed LNA with  $0.75 \times 0.69 \text{ mm}^2$  die area with transistor sizes W/L (µm) M1 = 30/0.18, M2 = 320/0.18, M3 = 320/0.18, M4 = 18/0.5, M5 = 125/0.18, Msw1 = 384/0.18, and inductor sizes width/turns/radius of spiral L<sub>1</sub> = 6 µm/3/39 µm, L<sub>2</sub> = 6 µm/3.5/61 µm.

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