Article

Analysis of Circuit Simulation Considering Total Ionizing Dose Effects on FinFET and Nanowire FET

Hyeonjae Won [1] and Myounggon Kang [1,2,*]

1   Department of Electronic Engineering, Korea National University of Transportation, Room No. 307, IT Building, 50 Daehak-ro, Chungju-si, Chungbuk 27469, Korea; whj617@ut.ac.kr
2   Department of IT Energy Convergence (BK21 FOUR), Korea National University of Transportation, Room No. 307, IT Building, 50 Daehak-ro, Chungju-si, Chungbuk 27469, Korea
*   Correspondence: mgkang@ut.ac.kr; Tel.: +82-43-841-5164

Abstract: In this study, we analyzed the total ionizing dose (TID) effect characteristics of p-type FinFET and Nanowire FET (NW-FET) according to the structural aspect through comparison of the two devices. Similar to n-type devices, p-type NW-FETs are less affected than FinFETs by the TID effect. For the inverter TID circuit simulation, both n- and p-types of FinFET and NW-FET were analyzed regarding the TID effect. The inverter operation considering the TID effect was verified using the Berkeley short-channel insulated-gate FET model (BSIM) common multi-gate (CMG) parameters. In addition, an inverter circuit composed of the NW-FET exhibited a smaller change by the TID than that of an inverter circuit composed of the FinFET. Therefore, the gate controllability of the gate-all-around (GAA) device had an excellent tolerance to not only short-channel effects (SCE) but also TID effects.

Keywords: radiation; total ionizing dose (TID); compact modeling; circuit simulation; Nanowire FET (NW-FET); FinFET; inverter

1. Introduction

Radiation hardening on semiconductor devices is a critical issue in various fields including radiation therapy, space, and nuclear reactor processes. The characteristics of devices change when they are exposed to a radiation environment. Designs, processes and shielding to reduce radiation effects are actively being studied in [1–4]. However, the research on the radiation effect in a single device is still insufficient. Single event effects (SEE), total ionizing dose (TID) effects, soft error rate (SER), displacement damage (DD), and multiple bit upsets (MBU) lead to the obstruction of the reliable operation of semiconductor devices due to radiation [5–9]. The TID effect causes the issue of changing the electrical properties of semiconductor devices due to the hole trap. When the particles pass the dielectric area, electron–hole pairs (EHP) are generated. Electrons with relatively fast mobility exit the dielectric region, but holes with low mobility have some holes trapped at the existing trap site, which increases the leakage current and causes a threshold voltage (V_T) shift [10]. Therefore, the device reliability is degraded. Nanoscale devices can be further affected by other static and dynamic parameters by the TID effect [11]. However, it is challenging to analyze the exact radiation effect due to the trap recovery of the irradiated device from the measurement [12,13]. Therefore, the TID phenomenon should be analyzed only by a simulation.

V_Ts has been used in the industry to continue the complementary metal–oxide–semiconductor (CMOS) scaling. However, critical issues such as the short-channel effect (SCE), V_T roll-off, and parasitic resistance emerge upon the FinFET scaling [14]. To alleviate these issues, Nanowire FET (NW-FET) has strong gate controllability and has been proposed to replace the FinFETs [15,16]. The better gate controllability provided by the gate-all-around (GAA) structure can overcome the SCE problem and enable a more

aggressive gate length scaling than that for the FinFETs [17–20]. Therefore, it is a promising solution for device miniaturization [21]. Thus, studies to mitigate the radiation effect of devices with this structure are required. In this study, TID simulations of a FinFET and NW-FET were carried out to analyze the element with a larger TID effect, according to the device structural part. This study was carried out by comparing the structural elements of the oxide area and gate controllability. Accurate TID simulation results were compared by calibrating the current and device sizes of the NW-FET and FinFET.

As the oxide area increases, more EHP occurs and the number of trapped holes increases. However, despite the larger oxide area of the NW-FET than the FinFET, the V_T did not change significantly, and the device appeared to be more resistant to radiation. It is shown by introducing the GAA structure, that the higher the gate controllability, the more the TID effect can be suppressed in the oxide region. In addition, the FinFET and NW-FET affected by the TID were extracted using a Berkeley short-channel insulated-gate FET (BSIM) common multi-gate (CMG) and applied to an inverter circuit to perform the simulation.

2. Methodology of TID Simulation

2.1. Device Structure Design

The TID effects of an NMOS FinFET and NW-FET have been analyzed [22]. In this study, we analyze the TID effect of PMOS devices. The PMOS NW-FET was stacked in five stages to match the current and device size to those in the NMOS device study. The FinFET and NW-FET were similarly constructed by the three-dimensional (3D) technology computer-aided design (TCAD) simulation tool. The PMOS FinFET was designed as an equal NMOS considering the International Technology Roadmap for Semiconductors (ITRS) [23]. Figure 1 shows the TCAD structures of the FinFET and NW-FET.

The devices were made with a silicon body and the n- and p-types dopant was phosphorus and boron. The device channel insulator materials were deposited SiO_2 and HfO_2. The I_D-V_G characteristics were calibrated for an accurate comparison of the TID effects. Tables 1 and 2 show each design's parameters and the initial V_T characteristics of the FinFET and NW-FET, respectively.

Table 1. Device's parameters.

Design Factor	FinFET	NW-FET
Channel length	12 nm	12 nm
FinFET's width and NW-FET's diameter	6 nm	6 nm
Height (NW-FET total height)	42 nm	30 nm
Total area	489.5 nm^2	474.9 nm^2
S/D doping	1×10^{21} cm^{-3}	1×10^{21} cm^{-3}
Channel doping	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Oxide area	237.5 nm^2	333.6 nm^2
EOT	0.812 nm	0.812 nm

Table 2. V_T data of each device.

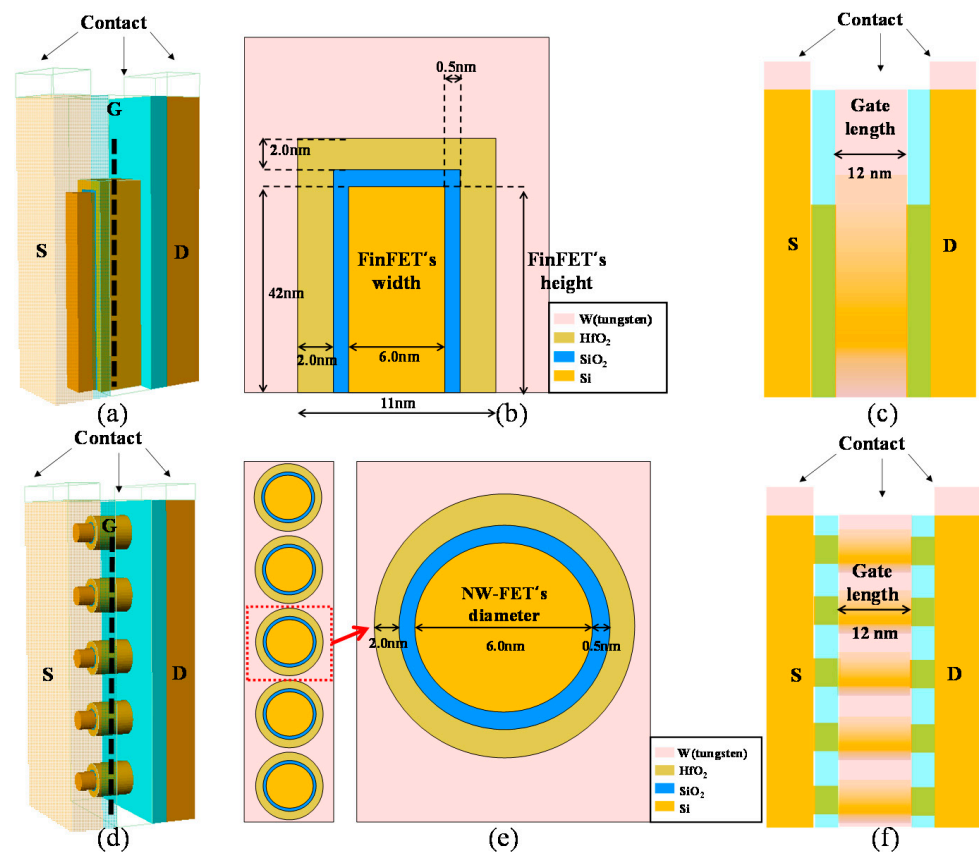| V_{DD} = 0.65 V	FinFET (V_T)	NW-FET (V_T)
NMOS	0.33 V	0.4 V
PMOS	0.3 V	0.38 V

Figure 1. Technology computer-aided design (TCAD) structures of the FinFET and Nanowire FET (NW-FET). (**a**) FinFET 3D structure; (**b**) FinFET's cross-section of gate; (**c**) FinFET's cross-section of channel length; (**d**) NW-FET 3D structure; (**e**) NW-FET's cross-section of gate; (**f**) NW-FET's cross-section of channel length.

2.2. Condition of TID Simulation

For the TID simulation, we used the Silvaco's Victory Device platform [24]. The Klaassen model was applied to the TID simulation to reflect electron and hole mobilities, trap parameters, recombination parameters, etc. [25–29]. In the TID simulation, the insulator region's trap–detrap model parameters were used as in [30]. The simulation was performed precisely, as the interface trap between SiO_2 and HfO_2 was calculated by using an interface trap parameter between the insulators. In the TID simulation, γ-ray irradiation obtained using a ^{60}Co source was used [31]. Each device was irradiated at 1 rad/s. The simulation was carried out at 100 krad, 1 Mrad, 10 Mrad, and 100 Mrad.

3. TID Simulation Results and Procedure of Compact Modeling with TID

Figure 2 shows the PMOS device's electrical characteristics according to the total dose. V_T was extracted when the drain absolute current was 0.1 μA using the constant current method, as shown in Figure 2. As the holes were trapped in the insulator region, V_T was shifted. The electrical properties further changed with the increase in the radiation dose.
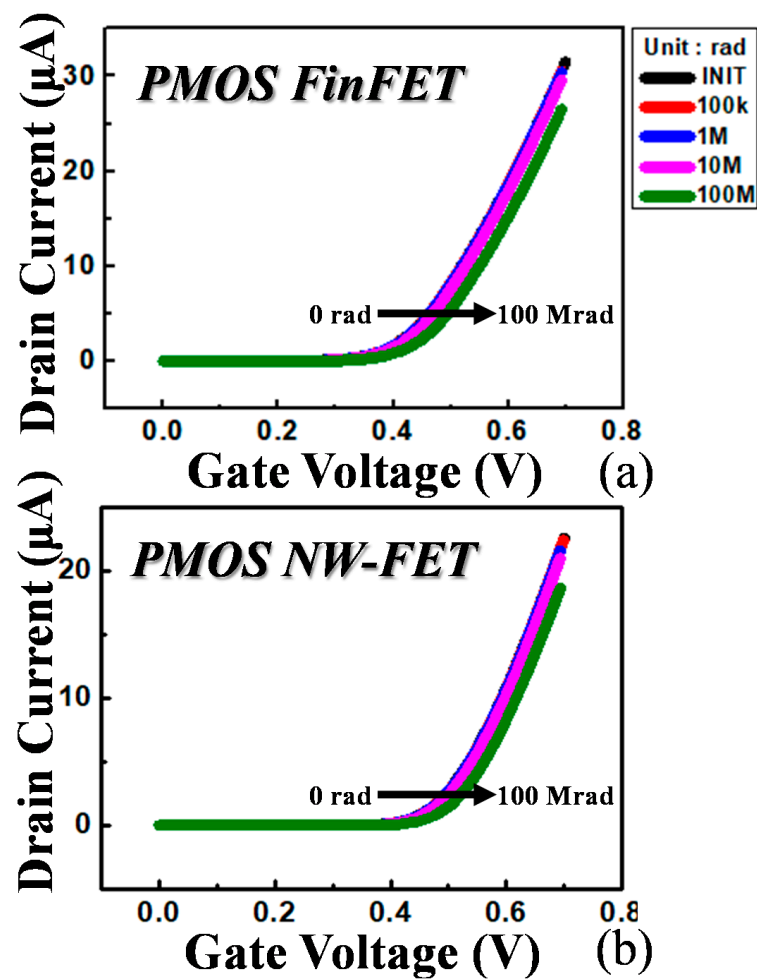
Figure 2. I_D-V_G curve shift with the increase in the radiation dose up to 100 Mrad. The simulation method sweeps V_G from 0 to 0.7 V when the total dose is reached. (**a**) PMOS FinFET; (**b**) PMOS NW-FET.

Figure 3 shows the V_T shift for each TID for both FinFET and NW-FET. The result before 10 Mrad shows a large change in the V_T of PMOS devices, but the result is reversed at 100 Mrad. Also, the V_T variation of n-type and p-type devices is about several mV. In the case of planar MOSFET, it is known that the PMOS device is affected more by the TID effect due to the interface trap. However, in the case of nanoscale 3D-structure devices, the influence of the interface trap is reduced because of the short channel length, and the V_T variation of n-type and p-type is similar. In addition, the more a device has a strong gate controllability, the less variation in the TID effect [32,33]. The NW-FET exhibits a smaller V_T shift than that of the FinFET. The NW-FET has a wider oxide area than FinFET. Thus, NW-FET had to be more affected by a TID effect and exhibit a larger V_T shift than FinFET. However, the NW-FET was less affected due to the superior gate controllability. This is suppressed not only the SCE problem, but also the TID effect issue [34]. Structurally, the NW-FET insulator area was larger (96.1 nm^2) than that in the FinFET. However, contrary to the expectations, the NW-FET had a smaller TID effect than that of FinFET. Therefore, the gate controllability is more important in the TID effect suppression than the oxide area.
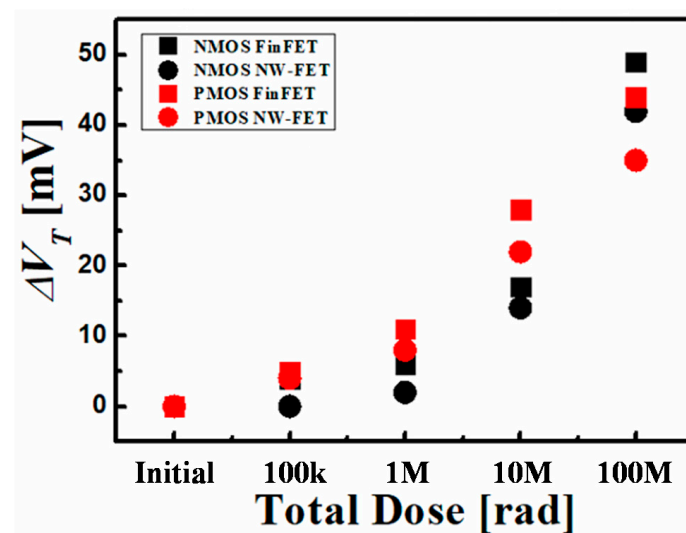
Figure 3. FinFET and NW-FET V_T shifts according to the total ionizing dose (TID).

The simulation of TID circuits requires a very long time period because of the numerous calculations. However, the spice circuit simulation method, which extracts and executes BSIM parameters, can check results faster than the conventional TCAD circuit simulation. Thus, for the circuit simulation, parameters of the BSIM, widely used in the industry as a standard compact model, were extracted. Figure 4 shows a flow chart of parameter extraction considering the TID characteristics. TID simulation data from the Victory Device platform were extracted using various BSIM CMG parameters. The extracted data were applied to the circuit simulation considering the TID.
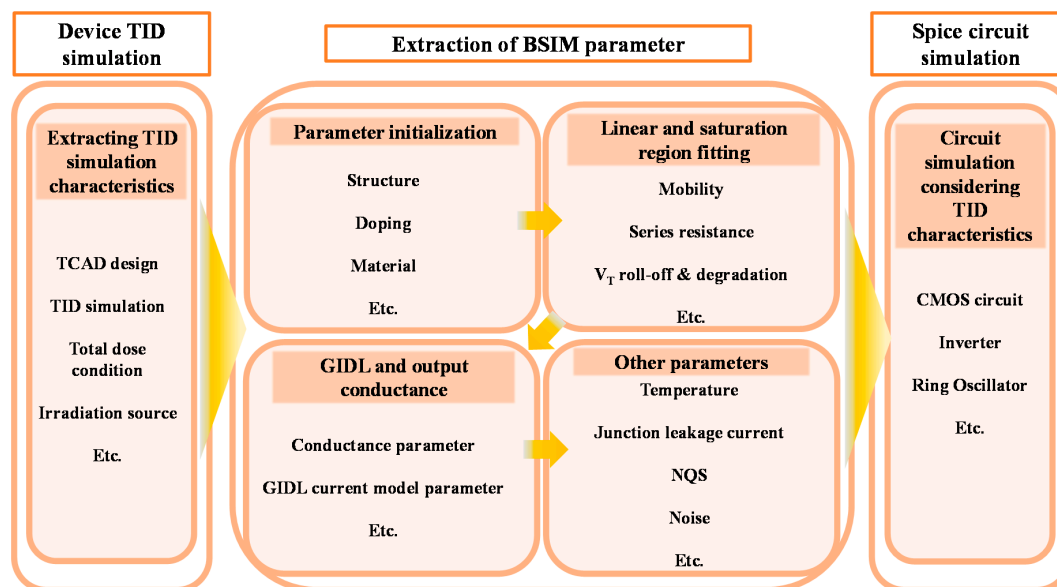

Figure 4. Flow chart of the simulations considering the TID effect.

4. Circuit Characteristics with the TID Effect

To extract the data for the inverter circuit simulation, calibration with the existing TCAD TID simulation data using BSIM CMG parameters was carried out. Figure 5 shows the results of the calibration of the electrical characteristics of the FinFET and NW-FET with the BSIM CMG parameters. The electrical properties of the FinFET and NW-FET fit well with the data extracted by the BSIM CMG parameters. In addition, the TID

simulation data in Figure 2 were extracted using the BSIM CMG parameters according to the radiation dose.

Figure 6 shows the device inverter operating characteristics according to the cumulative radiation dose. Larger switching point variations are observed with the increase in the total dose. Owing to the V_T shift of NMOS, the falling edge of the inverter operation causes a faster descent, while the V_T shift of PMOS causes a slow rise. Therefore, the TID effect changes the operating characteristics of the inverter and degrades the reliability. In addition, the FinFET inverter operation is more shifted than that of the NW-FET by the TID effect. The difference originates from the different gate controllability. The NW-FET inverter operation has a smaller variation with the TID than that of the FinFET inverter operation owing to its high gate controllability.
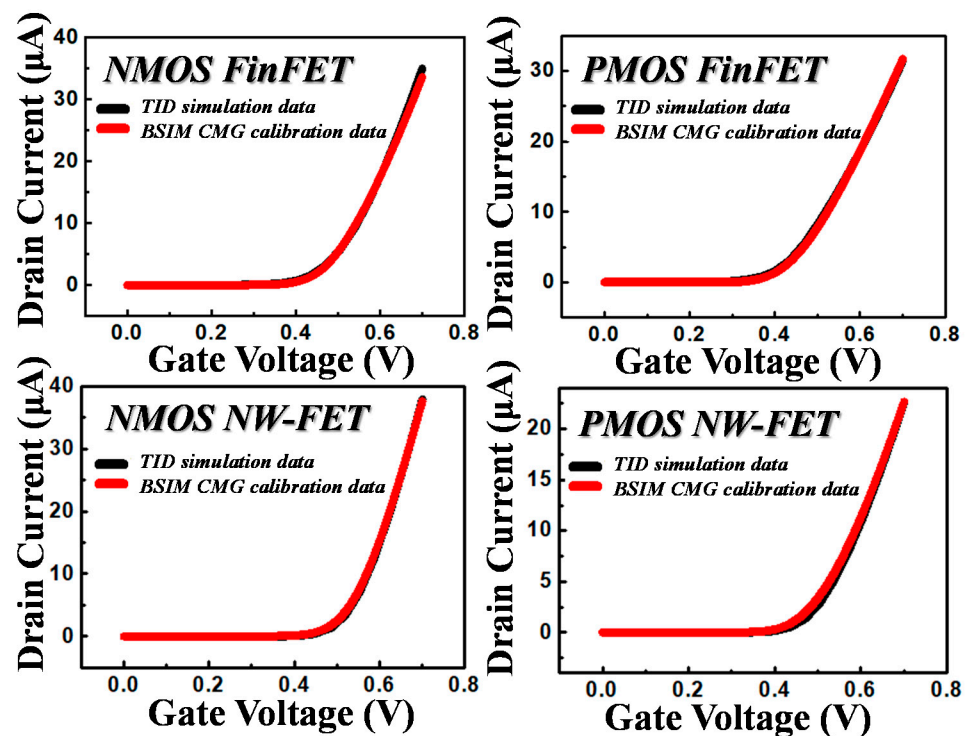

Figure 5. Calibration of the electrical characteristics of the FinFET and NW-FET with the Berkeley short-channel insulated-gate FET (BSIM) common multi-gate (CMG) parameters.
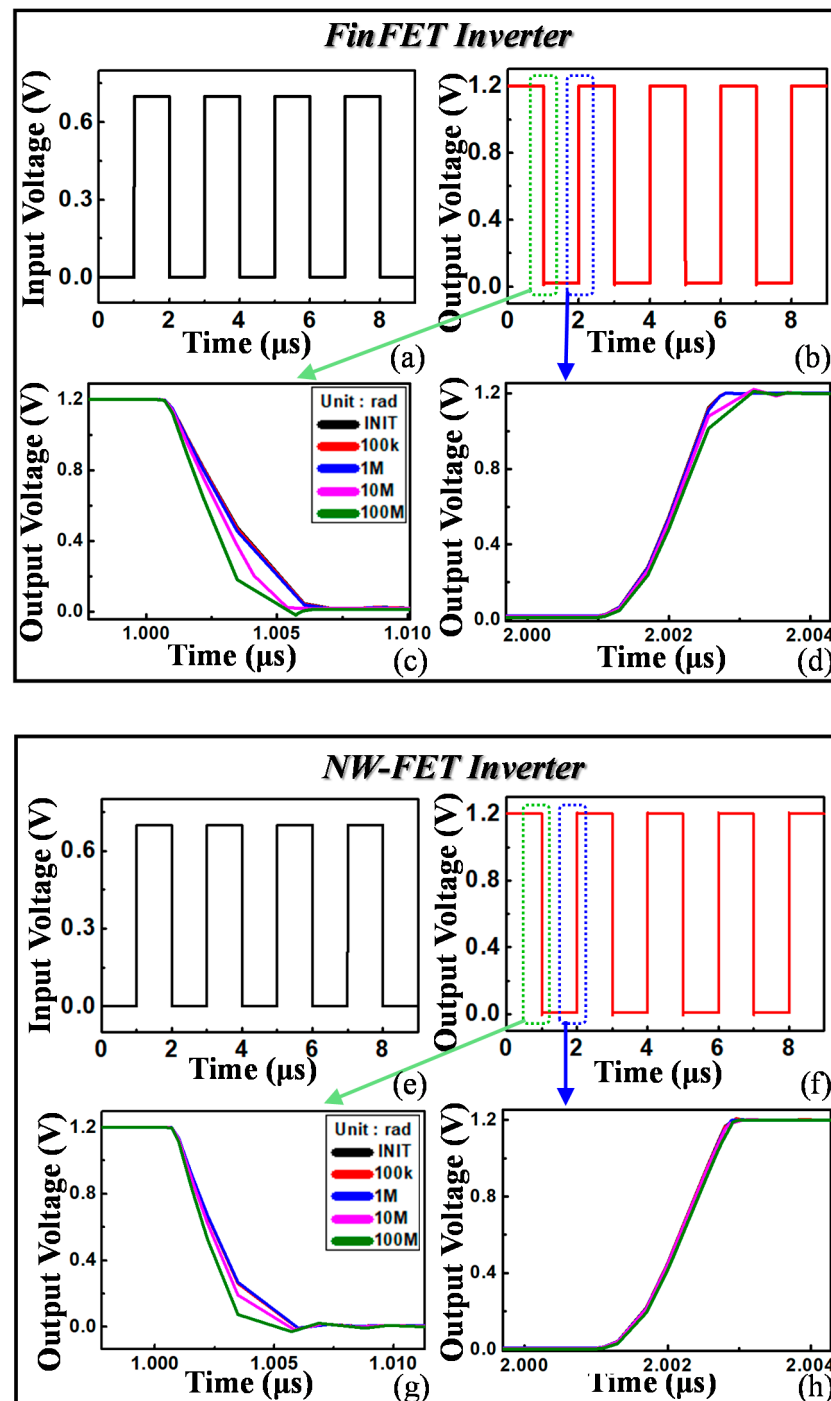
Figure 6. FinFET and NW-FET inverter operation characteristics according to the accumulated radiation dose. (**a**,**e**) inverter input pulse; (**b**) FinFET inverter output for each total dose; (**c**) FinFET inverter operation of falling edge; (**d**) FinFET inverter operation of rising edge; (**f**) NW-FET inverter output for each total dose; (**g**) NW-FET inverter operation of falling edge; (**h**) NW-FET inverter operation of rising edge.

5. Conclusions

The NW-FET device exhibited a smaller ionizing radiation sensitivity than that of the FinFET device. The NW-FET had a larger insulator area than that of the FinFET, approximately 96 nm². However, the NW-FET was less affected by the TID effect than the FinFET. The structure with a larger gate controllability confirmed that the TID effect

can be effectively overcome. To improve the gate controllability method, a GAA structure and high-*k* dielectric materials have to be introduced. In addition, we not only analyzed the effect of the TID on the device but also applied it to the inverter using the BSIM CMG parameter reflecting the TID. The TID effect changed the operating characteristics of the inverter and degraded the reliability. However, the NW-FET inverter operation had a smaller variation with the TID than that of the FinFET inverter operation because of its high gate controllability. Therefore, NW-FET devices are tolerant to the TID, which improves the circuit operation stability in radiation environments.

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