

Article

Generalized Structures for Switched-Capacitor Multilevel Inverter Topology for Energy Storage System Application

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Abstract: The apparent advantages of Multilevel Inverter (MLI) topologies in handling medium and high power with less loss in switching and lower harmonic distortion in an output voltage waveform makes it better than the conventional inverter. However, the MLI topologies utilize a large number of DC power supplies and power semiconductor devices. They also have a higher value of total standing voltage (TSV). Moreover, capacitor voltage balancing problems, self-voltage boosting inability, and complex control techniques require a relook and improvement in their structure. More recently, Switched-Capacitor Multilevel Inverter (SCMLI) topologies have been proposed to overcome the shortcomings of MLIs. In this paper, a generalized structure for a single-phase switched capacitor multilevel inverter (SCMLI) with self-voltage boosting and self-voltage balancing capability is proposed. A detailed analysis of a general structure of SCMLI is presented. The comparative analysis of the structures is carried out with recently reported topologies to demonstrate superiority. An optimized low-frequency modulation controls the output voltage waveform. The simulation and experimental results are included in the paper for single-unit symmetric (9-level voltage) and asymmetric (17-level voltage) configurations.

Keywords: energy storage; total harmonic distortion; switched-capacitor multilevel inverter (SCMLI); total standing voltage



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1. Introduction

Nowadays, the alteration of power from DC to AC is an important process and performs a vital task in modern power system network and industrial processes powered by electric drives [1]. DC to AC conversion is carried out by power electronics converters. Due to high harmonic losses in two-level inverters, multilevel inverters are used in order to have highly efficient power electronics and drive systems [2]. The main property of the Multilevel Inverter (MLI) is to generate an output voltage waveform resembling a staircase using several voltage sources at the input, which results in the low value of total harmonics distortion (THD) and minimal values of electromagnetic interference (EMI) and voltage stress across switches [3]. The three classical topologies of MLI are Cascaded H-bridge inverter (CHB), Flying Capacitor Clamped inverter (FC), and Neutral Point Clamped inverter (NPC) [4]. Due to easy control and unique characteristics, they are practically implemented as alteration technology in various applications ranging from small- to large-scale industries. In order to achieve higher voltage levels, a large number of devices are required, which enhances the size and cost of MLIs [5]. At higher voltage levels, NPC and FC show capacitor voltage unbalancing problems besides the requirement

for a significant number of clamping diodes and capacitors, respectively [6]. Cascaded H-bridge is the most feasible and flexible among the conventional topologies, utilizing less components, but the requirement of high DC power supply is a shortcoming, which makes MLI bulky and costly. Further, the classical topologies also do not have the ability to boost the output voltage [7]. Many symmetric topologies with less switches have been presented by the authors of [8–12] to overcome the problem of large switch requirements. However, as voltage levels increase considerably, DC power supplies, power semiconductor devices, gate driver circuits, and capacitors required in the topology increases. To overcome this drawback, reduced device count asymmetric topologies are used, which have DC power supplies of different magnitudes. In [13–20], various reduced device count asymmetric topologies have been presented. Both reduced device count symmetric as well as asymmetric topologies presented in [8–20] suffer from a self-voltage boosting inability and the capacitor voltage unbalancing problem due to which these topologies are not suitable for low-input DC voltage source applications. Some auxiliary circuits such as impedance network or forehead-type boost converter are used along with MLI to achieve a self-voltage boosting capability [21]. To overcome the problem of capacitor voltage unbalancing, a complex control algorithm was proposed in [22,23]. However, the cost, size, and complexity in the control mechanism are enhanced.

To overcome MLI's shortcomings, a Switched-capacitor Multilevel Inverter (SCMLI) has recently been proposed by various researchers. SCMLIs require fewer switches and driver circuits compared to other existing topologies, and they need less DC power supplies because capacitors act as alternate DC sources. The idea of SCMLIs was first proposed by O.C. Mak and A. Ioinovici in 1998 [24]. In [25], an integrated switched-capacitor MLI topology with a voltage string was presented, which needed a low number of switches, but it suffered from high voltage stress across the backend switch H-Bridge. To overcome this problem, the author of [26] presented an improved integrated switched-capacitor MLI topology. The author of [27] proposed an SCMLI topology using a series-parallel conversion, and it can be extended to generate a high number of voltage levels. However, it requires a significant number of components at high voltage levels. A novel stepup SCMLI topology developed by the author of [28] includes a switched capacitor DC/DC converter (SCC) and a full-bridge. SCC and full-bridge are used as a level generator and polarity generator, respectively. To further increase the number of output voltage levels with a reduced number of devices, the authors of [29] presented an SCMLI topology. However, the topologies presented in [28,29] have high voltage stress across H-bridge switches due to which it cannot be used in high voltage applications except medium voltage applications. Moreover, the per-unit total standing voltage (TSV) in both topologies is high. Self-balanced step-up SCMLI topologies were presented in [30,31] to overcome these problems. Thus, there is a requirement for a generalized structure of SCMLI, which can be used to obtain the desired number of voltage levels. In this paper, a generalized SCMLI topology structure was proposed with the target being reduced power electronic switches, driver circuits, capacitors and reduced TSV per unit for a higher number of voltage levels. This paper is organized as follows: Section 2 discusses the detailed analysis of the proposed generalized structure. In Section 3, the generalized SCMLI topology structures are compared with recently proposed topologies. In Section 4, an analysis of the basic unit is presented. The simulation results are discussed and its experimental validation are presented in Section 5. The paper is concluded in Section 6.

2. Proposed Generalized Structures of the Switched Capacitor Multilevel Inverter

A generalized structure of MLI (GSMLI) has been proposed in this paper. It is shown in Figure 1. It is obtained by extending the modified H-bridge inverter on the left and on both sides.

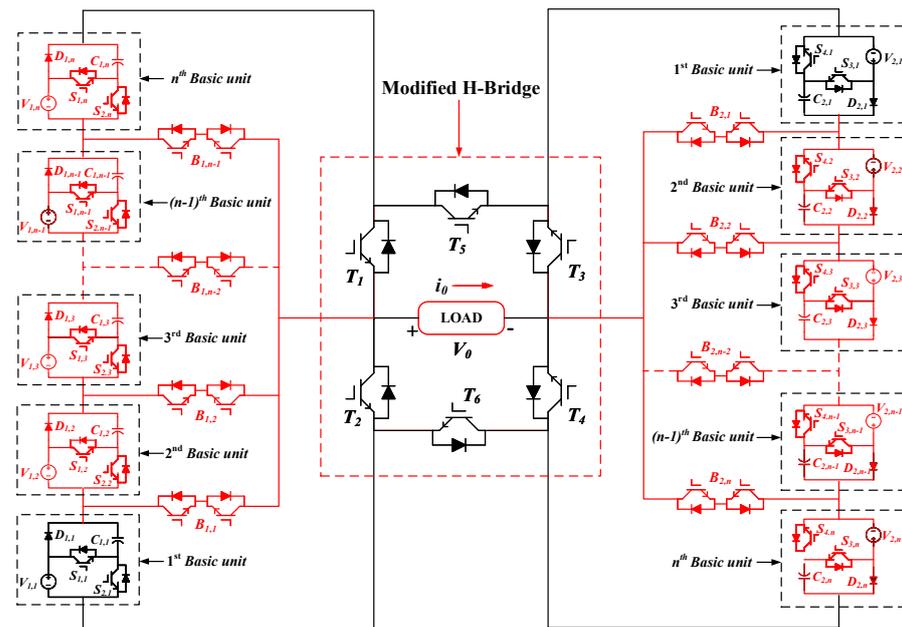


Figure 1. Circuit diagram of the Generalized Structure of the Multilevel Inverter (GSMLI).

GSMLI: The GSMLI is achieved by including $(n - 1)$ basic units and $(n - 1)$ bidirectional switches $(B_{1,1}, B_{1,2}, \dots, B_{1,n-1})$ to each side of the modified H-bridge, as shown in Figure 1 in red. Therefore, there are $2n$ total basic units from which n basic units are connected to the left side of the modified H-bridge and the remaining n basic units are on the right side of the bridge.

GSMLI can be operated in two different methods depending on the magnitude of the DC voltage sources of the left-side basic units.

(a) First method (GSMLI.1): When the basic units 1st, 2nd, 3rd, . . . , n th unit connected to the left side of the modified H-bridge have an equal magnitude of DC voltage sources and the basic units 1st, 2nd, 3rd, . . . , n th unit connected to the right side of the modified H-bridge have an equal magnitude of DC voltage sources but different from the left side basic units:

$$V_{1,1} = V_{1,2} = V_{1,3} = \dots \dots \dots V_{1,n-1} = V_{1,n} = V$$

Then, to generate the maximum possible voltage levels in this condition, the following equation must be satisfied by the voltage sources of basic units connected to the right side:

$$V_{2,1} = V_{2,2} = V_{2,3} = \dots \dots \dots V_{2,n-1} = V_{2,n} = (2n + 1)V$$

The capacitors $C_{1,1}, C_{1,2}, C_{1,3}, \dots, C_{1,n-1}, C_{1,n}$ are charged to V through switches $S_{2,1}, S_{2,2}, S_{2,3}, \dots, S_{2,n-1}, S_{2,n}$, respectively, and switches $S_{1,1}, S_{1,2}, S_{1,3}, \dots, S_{1,n-1}, S_{1,n}$ are used for discharging the capacitors. The capacitors $C_{2,1}, C_{2,2}, C_{2,3}, \dots, C_{2,n-1}, C_{2,n}$ are charged to $(2n + 1)V$ through switches $S_{4,1}, S_{4,2}, S_{4,3}, \dots, S_{4,n-1}, S_{4,n}$, respectively, and switches $S_{3,1}, S_{3,2}, S_{3,3}, \dots, S_{3,n-1}, S_{3,n}$ are used for discharging the capacitors.

The maximum value of the blocked voltage across switches excluding bidirectional switches $B_{1,1}, B_{1,2}, \dots, B_{1,n-1}$ and $B_{2,1}, B_{2,2}, \dots, B_{2,n-1}$ are given as

$$V_{S_{i,1}} = V_{S_{i,2}} = V_{S_{i,3}} = \dots \dots \dots V_{S_{i,n-1}} = V_{S_{i,n}} = V, i = 1,2$$

$$V_{S_{i,1}} = V_{S_{i,2}} = V_{S_{i,3}} = \dots \dots \dots V_{S_{i,n-1}} = V_{S_{i,n}} = (2n + 1)V, i = 3,4$$

$$V_{T1} = V_{T2} = 2nV, V_{T3} = V_{T4} = 2n(2n + 1)V$$

$$V_{T5} = V_{T6} = 4n(4n + 1)V$$

The maximum value of the blocked voltage across diodes $D_{1,1}, D_{1,2}, \dots, D_{1,n-1}$, and $D_{2,1}, D_{2,2}, \dots, D_{2,n-1}$ are given as

$$V_{D1,1} = V_{D1,2} = V_{D1,3} = \dots \dots \dots V_{D1,n-1} = V_{D1,n} = V$$

$$V_{D2,1} = V_{D2,2} = V_{D2,3} = \dots \dots \dots V_{D2,n-1} = V_{D2,n} = (2n + 1)V$$

The maximum value of the blocked voltage across bidirectional switches $B_{1,1}, B_{1,2}, \dots, B_{1,n-1}$ are given as follows:

When n is odd

$$V_{B1,i} = (2n - 2i)V \text{ for } i = 1, 2, 3, \dots, \dots, \dots, \frac{n-1}{2} \text{ for } n \geq 2$$

$$V_{B1,j} = 2jV \text{ for } j = \frac{n-1}{2} + 1, \frac{n-1}{2} + 2, \dots, \dots, n-1 \text{ for } n \geq 2$$

When n is even

$$V_{B1,i} = (2n - 2i)V \text{ for } i = 1, 2, 3, \dots, \dots, \dots, \frac{n-2}{2} \text{ for } n \geq 2$$

$$V_{B1,j} = 2jV \text{ for } j = \frac{n-2}{2} + 1, \frac{n-2}{2} + 2, \dots, \dots, n-1 \text{ for } n \geq 2$$

The maximum value of blocked voltage across bidirectional switches $B_{2,1}, B_{2,2}, \dots, B_{2,n-1}$ are given as follows:

When n is odd

$$V_{B2,i} = (2n - 2i)(2n + 1)V \text{ for } i = 1, 2, \dots, \dots, \dots, \frac{n-1}{2} \text{ for } n \geq 2$$

$$V_{B2,j} = 2(2n + 1)V \text{ for } j = \frac{n-1}{2} + 1, \frac{n-1}{2} + 2, \dots, \dots, n-1 \text{ for } n \geq 2$$

When n is even

$$V_{B2,i} = (2n - 2i)(2n + 1)V \text{ for } i = 1, 2, \dots, \dots, \dots, \frac{n-2}{2} \text{ for } n \geq 2$$

$$V_{B2,j} = 2j(2n + 1)V \text{ for } j = \frac{n-2}{2} + 1, \frac{n-2}{2} + 2, \dots, \dots, n-1 \text{ for } n \geq 2$$

TSV_{B1} of bidirectional switches $B_{1,1}, B_{1,2}, \dots, B_{1,n-1}$ is given as follows:

When n is odd

$$TSV_{B1} = \sum_{i=1}^{\frac{n-1}{2}} (2n - 2i)V + \sum_{j=\frac{n-1}{2}+1}^{n-1} (2j)V \text{ for } n \geq 2$$

$$TSV_{B1} = \left[\frac{3n^2 - 4n + 1}{2} \right] V \text{ for } n \geq 2$$

When n is even

$$TSV_{B1} = \sum_{i=1}^{\frac{n-2}{2}} (2n - 2i)V + \sum_{j=\frac{n-2}{2}+2}^{n-1} (2j)V + n \text{ for } n \geq 2$$

$$TSV_{B1} = \left[\frac{3n^2 - 6n}{2} \right] V \text{ for } n \geq 2$$

TSV_{B2} of bidirectional switches $B_{2,1}, B_{2,2}, \dots, B_{2,n-1}$ is given as follows:

When n is odd

$$TSV_{B2} = \sum_{i=1}^{\frac{n-1}{2}} (2n - 2i)(2n + 1)V + \sum_{j=\frac{n-1}{2}+1}^{n-1} (2j)(2n + 1)V \text{ for } n \geq 2$$

$$TSV_{B2} = \left[\frac{3n^2 - 4n + 1}{2} \right] (2n + 1)V \text{ for } n \geq 2$$

When n is even

$$TSV_{B2} = \sum_{i=1}^{\frac{n-1}{2}} (2n - 2i)V + \sum_{j=\frac{n-1}{2}+2}^{n-2} (2j)V + n \text{ for } n \geq 2$$

$$TSV_{B2} = \left[\frac{3n^2 - 6n}{2} \right] (2n + 1)V \text{ for } n \geq 2$$

Therefore, TSV of the proposed $GSMLL.1$ is given as

$$TSV = (\sum_{i=1}^n V_{S1,i}) + (\sum_{i=1}^n V_{S2,i}) + (\sum_{i=1}^n V_{S3,i}) + (\sum_{i=1}^n V_{S4,i}) + (\sum_{i=1}^n V_{D1,i}) + (\sum_{i=1}^n V_{D2,i}) + (\sum_{i=1}^6 V_{Ti}) + TSV_{B1} + TSV_{B2}$$

$$TSV = \left[\frac{6n^3 + 90n^2 + 38n + 2}{2} \right] V \text{ for odd values of } n \geq 2$$

$$TSV = \left[\frac{6n^3 + 82n^2 + 32n}{2} \right] V \text{ for even values of } n \geq 2$$

TSV in per unit of the proposed $GSMLL.1$ is given as

$$TSV_{p.u.} = \left[\frac{6n^3 + 90n^2 + 38n + 2}{8n^2 + 8n} \right] \text{ for odd values of } n \geq 2$$

$$TSV_{p.u.} = \left[\frac{6n^3 + 82n^2 + 32n}{8n^2 + 8n} \right] \text{ for even values of } n \geq 2$$

(b) Second method ($GSMLL.2$): When the basic units 1st, 2nd, 3rd, ..., n th unit connected to each side of the modified H-bridge have an unequal magnitude of DC voltage sources and generate the maximum possible voltage levels, the voltage magnitude of DC sources must be selected in a binary fashion as given by the following relation:

$$V_{1,j} = 2^{j-1}V \text{ for } j = 1, 2, 3, \dots, n$$

$$V_{2,j} = 2^{j-1} \cdot (2^{n+1} - 1)V \text{ for } j = 1, 2, 3, \dots, n$$

The capacitors $C_{1,1}, C_{1,2}, C_{1,3}, \dots, C_{1,n-1}, C_{1,n}$ and capacitors $C_{2,1}, C_{2,2}, C_{2,3}, \dots, C_{2,n-1}, C_{2,n}$ are charged in binary fashion. The voltage across capacitors $C_{1,1}, C_{1,2}, C_{1,3}, \dots, C_{1,n-1}, C_{1,n}$ are given by the following equation:

$$V_{C1,j} = 2^{j-1}V \text{ for } j = 1, 2, 3, \dots, n$$

The voltage across capacitors $C_{2,1}, C_{2,2}, C_{2,3}, \dots, C_{2,n-1}, C_{2,n}$ are given as

$$V_{C2,j} = 2^{j-1} \cdot (2^{n+1} - 1)V \text{ for } j = 1, 2, 3, \dots, n$$

The maximum value of the blocked voltage across switches excluding bidirectional switches $B_{1,1}, B_{1,2}, \dots, B_{1,n-1}$ are given as

$$V_{S1,j} = V_{S2,j} = 2^{j-1}V \text{ for } j = 1, 2, 3, \dots, n$$

$$V_{S3,j} = V_{S4,j} = 2^{j-1} \cdot (2^{n+1} - 1)V \text{ for } j = 1, 2, 3, \dots, n$$

$$V_{T1} = V_{T2} = (2^{n+1} - 2)V, V_{T3} = V_{T4} = (2^{n+1} - 2)(2^{n+1} - 1)V$$

$$V_{T5} = V_{T6} = (2^{n+1} - 2) (2^{n+1})V$$

The maximum value of the blocked voltage across diodes $D_{1,1}, D_{1,2}, \dots, D_{1,n-1}$, and $D_{2,1}, D_{2,2}, \dots, D_{2,n-1}$ are given as

$$V_{D1,j} = 2^{j-1}V \text{ for } j = 1, 2, 3, \dots, n$$

$$V_{D2,j} = 2^{j-1} \cdot (2^{n+1} - 1)V \text{ for } j = 1, 2, 3, \dots, n$$

The maximum value of the blocked voltage across bidirectional switches $B_{1,1}, B_{1,2}, \dots, B_{1,n-1}$ are given as

$$V_{B1,j} = (2^{n+1} - 2 - 2 \sum_{i=1}^j 2^{i-1})V \text{ for } n \geq 2$$

The maximum value of the blocked voltage across bidirectional switches $B_{2,1}, B_{2,2}, \dots, B_{2,n-1}$ are given as

$$V_{B1,j} = (2^{n+1} - 2 - 2 \sum_{i=1}^j 2^{i-1})(2^{n+1} - 1)V \text{ for } n \geq 2$$

TSV_{B1} of the bidirectional switches $B_{1,1}, B_{1,2}, \dots, B_{1,n-1}$ is given as

$$TSV_{B1} = [(n - 2)2^{n+1} + 4]V \text{ for } n \geq 2$$

TSV_{B2} of the bidirectional switches $B_{2,1}, B_{2,2}, \dots, B_{2,n-1}$ is given as

$$TSV_{B2} = [(n - 2)2^{n+1} + 4](2^{n+1} - 1)V \text{ for } n \geq 2$$

The overall TSV of the proposed GSMLI.2 is given as

$$TSV = [(2n - 9)2^n + 2^{2n+3} + 1](2^{n+1})V \text{ for } n \geq 2$$

TSV in per unit of the proposed GSMLI.2 is given as

$$TSV_{p.u} = \left[\frac{[(2n - 9)2^n + 2^{2n+3} + 1]}{2^{n+1} - 2} \right] \text{ for } n \geq 2$$

For n number of basic units connected to each side of the modified H-bridge, the numbers of levels (N_L), switches (N_{sw}), driver circuits (N_{dri}), diodes (N_{diode}), and capacitors (N_{cap}) in terms of the number of stages (n) and the number of level (N_L) for GSMLI.1 and GSMLI.2 are given by Table 1.

Table 1. Generalized formulas for different devices of GSMLI.

Parameters	n Is the Number of Stages		N_L Is the Number of Levels	
	First Method	Second Method	First Method	Second Method
N_L	$8n^2 + 8n + 1$	$2^{2n+3} - 2^{n+3} + 1$	N_L	N_L
N_{sw}	$8n + 2$	$8n + 2$	$2[-3 + \sqrt{2(N_L + 1)}]$	$8\log_2[2 + \sqrt{2(N_L + 1)}] - 14$
N_{dri}	$6n + 4$	$6n + 4$	$[-2 + \frac{3}{2}\sqrt{2(N_L + 1)}]$	$6\log_2[2 + \sqrt{2(N_L + 1)}] - 8$
N_{diode}	$2n$	$2n$	$[-2 + \frac{1}{2}\sqrt{2(N_L + 1)}]$	$2\log_2[2 + \sqrt{2(N_L + 1)}] - 4$
N_{cap}	$2n$	$2n$	$[-2 + \frac{1}{2}\sqrt{2(N_L + 1)}]$	$2\log_2[2 + \sqrt{2(N_L + 1)}] - 4$

3. Comparative Analysis of the Proposed GSMLI Topology

The proposed generalized structure was compared with other recent topologies. The performance of various parameters such as numbers of diodes (N_{diode}), switches (N_{sw}), capacitors (N_{cap}), drivers (N_{dri}), and $TSV_{p.u.}$, and cost function per level (CF/N_L), are shown in Figure 2. It may be noted that all these topologies are designed to generate seventeen levels of output voltage. Cost function per level (CF/N_L) is defined as

$$CF = (N_{sw} + N_{cap} + N_{dri} + N_{diode} + \alpha * TSV) \times N_{source}$$

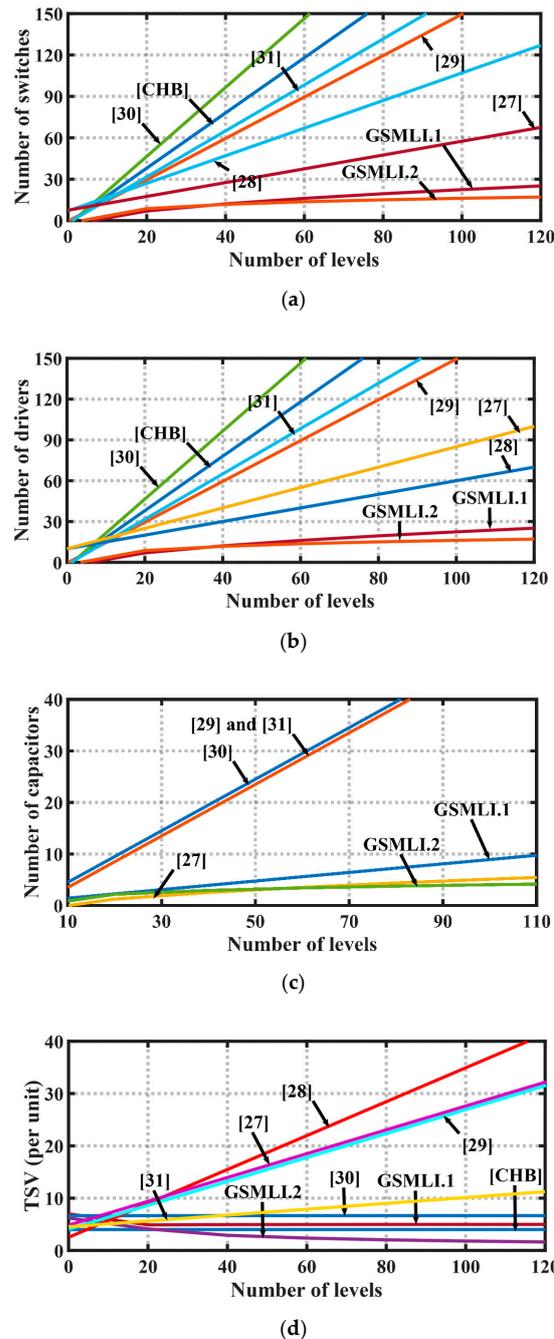


Figure 2. Comparison curves: (a) number of switches vs. number of levels, (b) number of switches vs. number of levels, (c) number of switches vs. number of levels, and (d) total standing voltage (TSV) (per unit) vs. the number of levels.

Here, α represents the contribution of TSV in the cost function

The comparisons are carried out among the levels of generalized structure of the proposed topology and other topologies. The comparison is conducted in terms of numbers of switches, drivers, capacitors, diodes, and TSV when all generated the same levels. From Figure 2a, it can be observed that the number of switches required in the generalized structure in both methods (first and second) is less than the number of switches required by other topologies for the same number of levels. It can also be seen from Figure 2a that the number of switches required in the second method generalized structure is less than the switches required by the first method of generalized structure. From Figure 2b,c, it is clear that the number of driver circuits and capacitors required in GSMLI in both methods (first and second) is less than the number of drivers and capacitors required by other topologies for the same number of levels. In [28], there is no capacitor, which is why it is not shown in Figure 2c.

From Figure 2d, it is clear that the TSV (in per unit) in GSMLI (second method) is less than the other topologies when all generated the same number of levels. TSV (in per unit) in the GSMLI (first method) is higher than the CHB and in [30] when all generated the same number of levels; however, it requires less switches, drivers, and capacitors compared to CHB and in [30].

4. Analysis of the Basic Unit of GSMLI

The generalized topology presented in this work was simulated and experimentally verified by considering one unit in symmetric and asymmetric mode. It has also been tested for TSV, and optimal capacitance was calculated in this section. The basic units act as a level generator that can produce two voltage levels from a solitary DC power supply. Figure 3 shows the conducting paths of the proposed topology for asymmetric configuration. Switches S_2 and S_4 and diodes D_1 and D_2 of the basic units are utilized for the charging purpose of capacitors C_1 and C_2 , respectively, while switches S_1 and S_3 are used for discharging capacitors C_1 and C_2 , respectively, in order to take the participation of the capacitor voltages into consideration in voltage level generation. The switches used in the modified H-Bridge are T_1, T_2, T_3, T_4, T_5 , and T_6 . Positive voltage levels are generated by utilizing switches T_1, T_4 , and T_6 , whereas negative voltage levels are generated by utilizing switches T_2, T_3 , and T_5 . Thus, the operation of switch pairs (T_1, T_2) , (T_3, T_4) , (T_5, T_6) , (T_7, T_8) , (S_1, S_2) , and (S_3, S_4) are complementary. This topology is capable of generating $0V, \pm V_1, \pm(V_1 + V_{C1}), \pm V_2, \pm(V_1 + V_2), \pm(V_1 + V_{C1} + V_2), \pm(V_2 + V_{C2}), \pm(V_1 + V_2 + V_{C2})$, and $\pm(V_1 + V_{C1} + V_2 + V_{C2})$ voltage levels. This topology is self-balancing for capacitor voltage because charging and discharging take place in an alternate manner and, if there is any voltage drop in capacitors voltage due to discharging, then it is regained during charging. This topology can damp out the disparate voltage between the capacitor and power supply, due to which it acts as a practically effective power circuit.

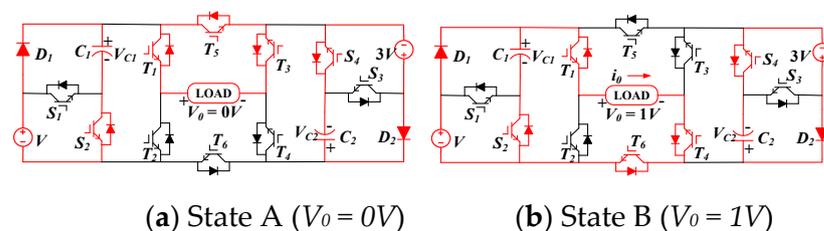


Figure 3. Cont.

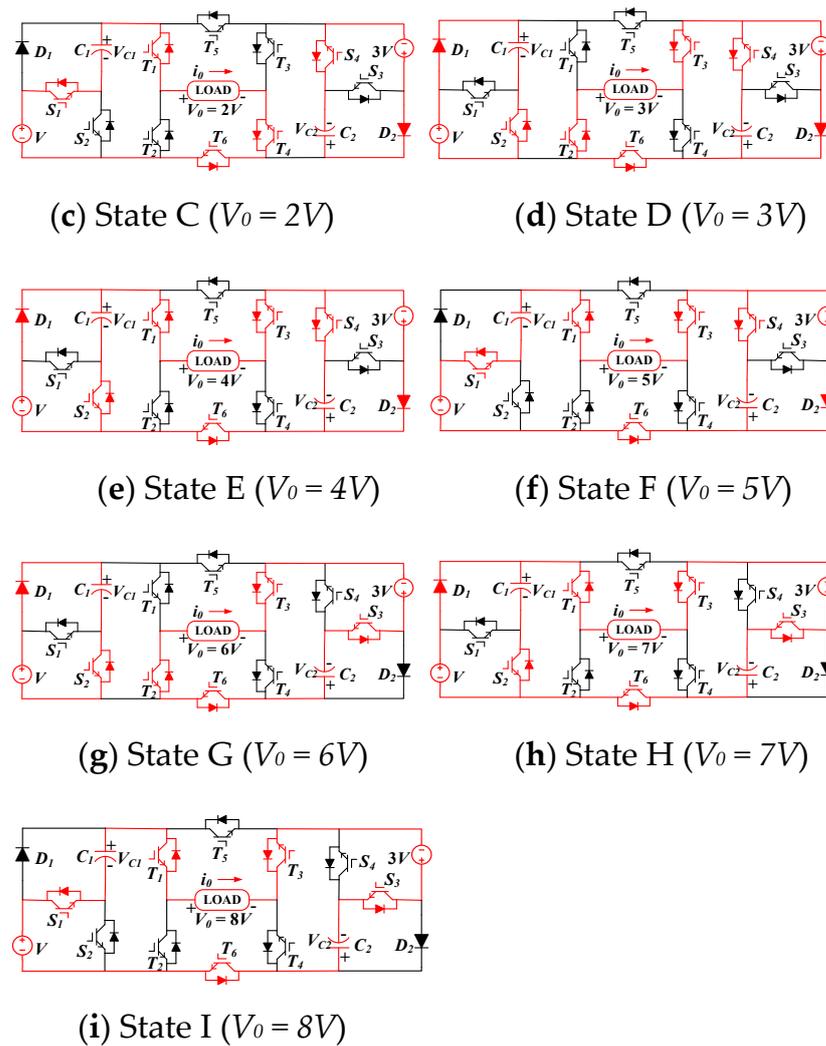


Figure 3. Conducting path for positive half-cycle modes.

4.1. Operating States

The proposed topology can be utilized in asymmetric and symmetric configurations. Table 2 illustrates the switching states of T_1 to T_6 and S_1 to S_4 , the charging and discharging states of capacitors C_1 and C_2 in a fastidious switching state. “C” and “D” indicate that the capacitor is charged and discharged, respectively. “-” indicates that there is no change in the states of the capacitors. “1” denotes the on state of switches, while “0” denotes the off state of switches.

When both DC voltage sources have the same magnitude ($V_1 = V_2$), then it is operated in symmetric configuration and produces 9 levels in $0V, \pm V_1, \pm(V_1 + V_{C1}), \pm(2V_1 + V_{C1})$, and $\pm(2V_1 + V_{C1} + V_{C2})$ output voltage waveform, which can be seen from Table 2. From Table 2, it can be observed that more levels are generated when both voltage sources have different magnitudes of voltage, i.e., asymmetric configuration.

To generate the maximum available voltage levels, it must be operated in asymmetric configuration and the magnitude of DC voltage sources V_1 and V_2 must be selected in a 1:3 ratio. When it is operated in asymmetric configuration ($3V_1 = V_2$), it produces 17 levels ($0V, \pm V_1, \pm(V_1 + V_{C1}), \pm 3V_1, \pm 4V_1, \pm(4V_1 + V_{C1}), \pm(3V_1 + V_{C2}), \pm(4V_1 + V_{C2})$, and $\pm(4V_1 + V_{C1} + V_{C2})$) in output voltage waveform, as shown in Table 2.

Table 2. States of switches and capacitors.

States	Output Voltage(V_0)	S_1 or S_2	S_3 or S_4	T_1 or T_2	T_3 or T_4	T_5 or T_6	T_7 or T_8	C_1	C_2	(V_0) Symmetric ($V_1 = V_2 = V_{C1} = V_{C2} = V$)	(V_0) Asymmetric ($V_1 = V_{C1} = V$ & $V_2 = V_{C2} = 3V$)
A	0V	0	0	0	0	0	0	c	c	0V	0V
B	V_1	0	0	1	0	0	0	-	-	$V_1 = V$	$V_1 = V$
C	$V_1 + V_{C1}$	1	0	1	0	0	0	d	-	$V_1 + V_{C1} = 2V$	$V_1 + V_{C1} = 2V$
D	V_2	0	0	0	0	1	0	c	-	$V_2 = V$	$V_2 = 3V$
E	$V_1 + V_2$	0	0	1	0	1	0	-	-	$V_1 + V_2 = 2V$	$V_1 + V_2 = 4V$
F	$V_1 + V_{C1} + V_2$	1	0	1	0	1	0	d	-	$V_1 + V_{C1} + V_2 = 3V$	$V_1 + V_{C1} + V_2 = 5V$
G	$V_2 + V_{C2}$	0	1	0	0	1	0	c	d	$V_2 + V_{C2} = 2V$	$V_2 + V_{C2} = 6V$
H	$V_1 + V_2 + V_{C2}$	0	1	1	0	1	0	-	d	$V_1 + V_2 + V_{C2} = 3V$	$V_1 + V_2 + V_{C2} = 7V$
I	$V_1 + V_{C1} + V_2 + V_{C2}$	1	1	1	0	1	0	d	d	$V_1 + V_{C1} + V_2 + V_{C2} = 4V$	$V_1 + V_{C1} + V_2 + V_{C2} = 8V$
J	$-V_1$	0	0	0	1	0	0	c	c	$-V_1 = -V$	$-V_1 = -V$
K	$-(V_1 + V_{C1})$	1	0	0	1	0	0	d	-	$-(V_1 + V_{C1}) = -2V$	$-(V_1 + V_{C1}) = -2V$
L	$-V_2$	0	0	0	0	0	1	c	-	$-V_2 = -V$	$-V_2 = -3V$
M	$-(V_1 + V_2)$	0	0	0	1	0	1	-	-	$-(V_1 + V_2) = -2V$	$-(V_1 + V_2) = -4V$
N	$-(V_1 + V_{C1} + V_2)$	1	0	0	1	0	1	d	-	$-(V_1 + V_{C1} + V_2) = -3V$	$-(V_1 + V_{C1} + V_2) = -5V$
O	$-(V_2 + V_{C2})$	0	1	0	0	0	1	c	d	$-(V_2 + V_{C2}) = -2V$	$-(V_2 + V_{C2}) = -6V$
P	$-(V_1 + V_2 + V_{C2})$	0	1	0	1	0	1	-	d	$-(V_1 + V_2 + V_{C2}) = -3V$	$-(V_1 + V_2 + V_{C2}) = -7V$
Q	$-(V_1 + V_{C1} + V_2 + V_{C2})$	1	1	0	1	0	1	d	d	$-(V_1 + V_{C1} + V_2 + V_{C2}) = -4V$	$-(V_1 + V_{C1} + V_2 + V_{C2}) = -8V$

Total standing voltage (TSV) is one of the most important parameters while designing different inverter topologies. TSV is defined as the sum of the maximum blocked voltage (stress) across the semiconductor switches and diodes when the output voltage of all possible levels is generated at the output.

The maximum value of blocked voltage across each switch in symmetric configuration ($V_1 = V_2 = V$) is given as

$$V_{T1} = V_{T2} = 2V_1 = 2V, V_{T3} = V_{T4} = 2V_2 = 2V$$

$$V_{T5} = V_{T6} = 2(V_1 + V_2) = 4V, V_{S1} = V_{S2} = V_1 = V$$

$$V_{S3} = V_{S4} = V_2 = V, V_{D1} = V_1 = V, V_{D2} = V_2 = V$$

where $V_{T1}, V_{T2}, V_{T3}, V_{T4}, V_{T5}, V_{T6}, V_{S1}, V_{S2}, V_{S3}, V_{S4}, V_{D1}$, and V_{D2} are the blocked voltages across switches $T_1, T_2, T_3, T_4, T_5, T_6, S_1, S_2, S_3$, and S_4 respectively.

$$TSV = V_{T1} + V_{T2} + V_{T3} + V_{T4} + V_{T5} + V_{T6} + V_{S1} + V_{S2} + V_{D1} + V_{S3} + V_{D2} + V_{S4} = 22V$$

TSV in per unit is defined as

$$TSV_{p.u.} = \frac{TSV}{V_{o,max}}$$

where $V_{o,max}$ is the maximum value of output voltage $TSV_{p.u}$ in symmetric configuration is given as

$$TSV_{p.u.} = \frac{22V}{4V} = 5.5$$

The maximum value of the blocked voltage across each switch in asymmetric configuration ($V_1 = V$ and $V_2 = 3V$) is given as

$$V_{T1} = V_{T2} = 2V_1 = 2V, V_{T3} = V_{T4} = 2V_2 = 6V$$

$$V_{T5} = V_{T6} = 2(V_1 + V_2) = 8V, V_{S1} = V_{S2} = V_1 = V$$

$$V_{S3} = V_{S4} = V_2 = 3V, V_{D1} = V_1 = V, V_{D2} = V_2 = 3V$$

$$TSV = 44V$$

$TSV_{p.u}$ in asymmetric configuration is given as

$$TSV_{p.u.} = \frac{44V}{8V} = 5.5$$

4.2. Capacitance Selection

The optimal value of capacitances for both switched capacitors (C_1 and C_2) is calculated based on the longest discharge time (LDT) over a complete cycle of the fundamental output voltage. The maximum quantity of charges from switched capacitors is discharged during LDT. Figure 4 shows the output voltage of this proposed topology (asymmetric) along with the LDT for both switched capacitors. The LDT for C_2 is high compared to C_1 .

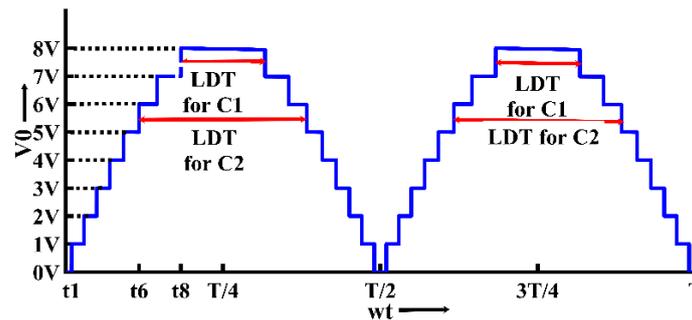


Figure 4. Waveform of output voltage (inverted negative half-cycle) along with the longest discharge time (LDT) of capacitors in asymmetric configuration.

The amount of discharge during LDT for switched capacitor C_2 can be calculated as

$$Q_{C2} = 2 \times \int_{t_6}^{T/4} i_0(t) dt \tag{1}$$

For resistive load, the output current during LDT can be expressed as

$$i_0(t) = \frac{6V}{R_L} \text{ for } t_6 < t < t_7 \quad i_0(t) = \frac{7V}{R_L} \text{ for } t_7 < t < t_8 \tag{2}$$

$$i_0(t) = \frac{8V}{R_L} \text{ for } t_8 < t < T/4$$

Due to the application of a fundamental frequency scheme, the time t_8 , t_7 , and t_6 can be given as

$$t_6 = \text{Sin}^{-1}(11/16) * \frac{1}{2\pi f} \quad t_7 = \text{Sin}^{-1}(13/16) * \frac{1}{2\pi f} \quad t_8 = \text{Sin}^{-1}(15/16) * \frac{1}{2\pi f} \tag{3}$$

From Equations (1)–(3), we get Q_{C2} as

$$Q_{C2} = \frac{12V}{2\pi f R_L} \tag{4}$$

The value of optimal capacitance for switched capacitor C_2 can be calculated as

$$C_{2opt} \geq \frac{QC1 \text{ or } QC2}{p \times V} \tag{5}$$

From Equations (4) and (5),

$$C_{2opt} \geq \frac{12}{2\pi f \times R_L \times p} \tag{6}$$

The amount of discharge during LDT for switched capacitor C_1 can be calculated as

$$Q_{C1} = 2 \times \int_{t_8}^{T/4} i_0(t) dt \tag{7}$$

From Equations (2), (3), and (7), we get Q_{C1} as

$$Q_C = \frac{6V}{2\pi f R_L} \tag{8}$$

From Equations (5) and (8), the optimal capacitance (C_{1opt}) for switched capacitor C_1 is given:

$$C_{1opt} \geq \frac{6}{2\pi f \times R_L \times p} \tag{9}$$

where p is the maximum allowable output voltage ripple in percentage, R_L is load resistance, and V is input source voltage. From Equations (6) and (9), it can be observed that the optimal value of capacitances depends on the ripple in voltage, load resistance, and operating frequency. The variation of the optimal capacitance C_{2opt} with frequency (at $R_L = 100 \Omega$) for different values of voltage ripples are shown in Figure 5a. The variation in the optimal capacitances (C_{1opt} and C_{2opt}) with load resistance for different values of voltage ripples is shown in Figure 5b,d, respectively. From Figure 5b,d, it is clear that, for a particular value of voltage ripple, the values of optimal capacitances (C_{1opt} and C_{2opt}) decrease as the load resistance increases.

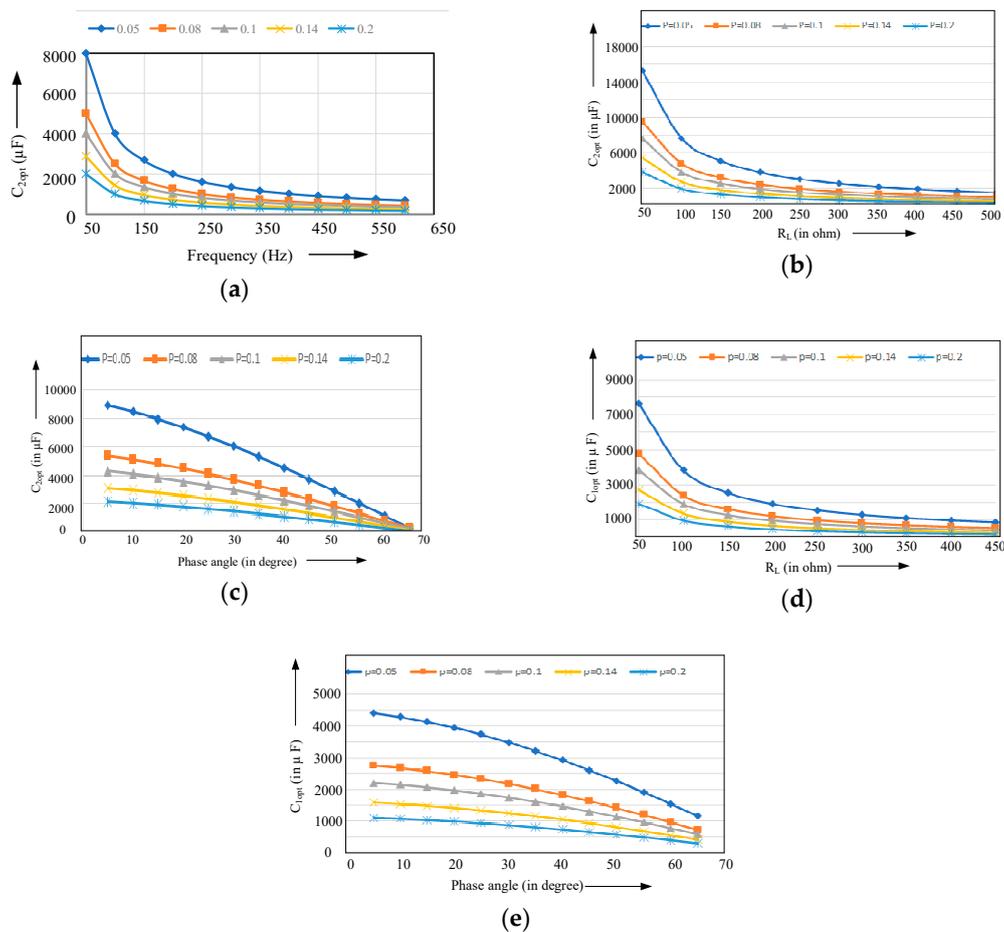


Figure 5. Variation in optimal capacitance C_{2opt} with (a) frequency (f), (b) load resistance (R_L), (c) and phase angle for different values of ripple in capacitor voltage and variation in optimal capacitance C_{1opt} with (d) load resistance (R_L) and (e) phase angle for different values of ripple in a capacitor voltage.

For R-L load, the output current can be expressed as

$$i_0(t) = I_{0max} \sin(\omega t - \varphi) \quad (10)$$

where φ is the phase angle between the fundamental output voltage and output current.

From Equations (1), (3), and (10), we get Q_{C2} as

$$\begin{aligned} Q_{C2} &= 2 \times \int_{t_{t6}}^{T/4} I_{0max} \sin(\omega t - \varphi) dt \\ Q_{C2} &= \frac{I_{0max}}{2\pi f} [\cos(0.75 - \varphi) - \sin(\varphi)] \end{aligned} \quad (11)$$

From Equations (5) and (11),

$$C_{2opt} \geq \frac{I_{0max}}{2\pi f \times V \times p} [\cos(0.75 - \varphi) - \sin(\varphi)] \quad (12)$$

From Equations (3), (7), and (10), we get Q_{C1} as

$$\begin{aligned} Q_{C1} &= 2 \times \int_{t_{t8}}^{T/4} I_{0max} \sin(\omega t - \varphi) dt \\ Q_{C1} &= \frac{I_{0max}}{2\pi f} [\cos(1.21 - \varphi) - \sin(\varphi)] \end{aligned} \quad (13)$$

From Equations (5) and (13), we get the optimal value of capacitance C_{1opt} :

$$C_{1opt} \geq \frac{I_{0max}}{2\pi f \times V \times p} [\cos(1.21 - \varphi) - \sin(\varphi)] \quad (14)$$

For plotting the graph between the optimal capacitance and phase angle for different values of voltage ripple, we take $I_{0max} = 4A$ and $V = 20$ volt. Figure 5c,e show the variation in optimal capacitances (C_{1opt} and C_{2opt}) with phase angle for different voltage ripples. From these figures, it is clear that, for a particular value of voltage ripple, the optimal capacitance decreases as the phase angle increases.

4.3. Modulation Scheme

Different modulation schemes are used for controlling the MLI output voltage. Apart from reducing THD, fundamental frequency switching schemes are also capable of minimizing the switching losses. Fundamental switching frequency schemes such as Selective Harmonic Elimination (SHE), nearest level control, and space vector control are preferred for high power applications. The main disadvantage of SHE is to solve the system of nonlinear trigonometric transcendental equations, which consume more computational time. Hence, the SHE technique is not concerned with real-time (closed-loop) applications. The nearest control techniques can eliminate this drawback of SHE. Nearest Level Control (NLC) can be classified as (1) the nearest space vector control and (2) nearest level control [26]. In this work, an optimized nearest level control is utilized for controlling the output voltage and different carrier signals are compared with a reference signal [26]. The level generation method and block scheme are shown in Figures 6 and 7, respectively, for the NLC.

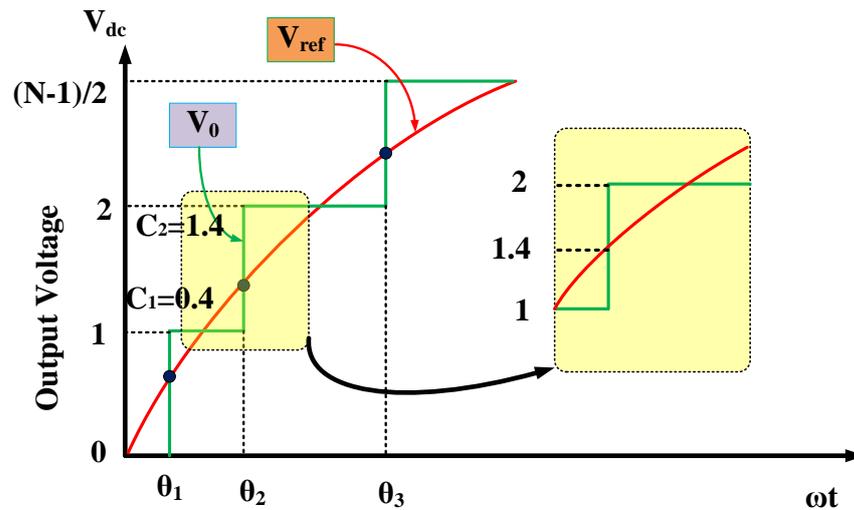


Figure 6. Level generation method of the optimized nearest level control.

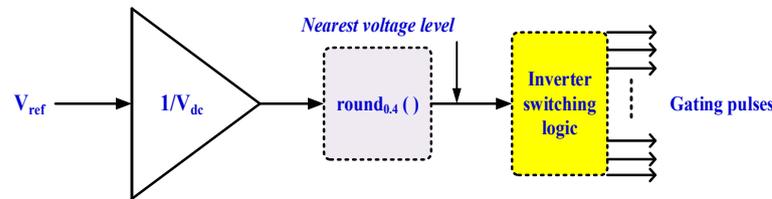


Figure 7. Block diagram of an Optimized Nearest Level Control (ONLC).

The equation for output voltage is shown below:

$$V_{out} = M * (N_{level} - 1)/2 * V_{dc} * \cos(\omega t)$$

where m is the modulation index and is expressed as

$$M = V_{ref(max)} / nV_{dc}$$

where $n = (N_{level} - 1)/2$.

5. Simulation and Hardware Realization of the Basic Unit of the Proposed GSMLI Topologies

To assert the feasibility of the topologies, a MATLAB®/Simulink-based simulation was carried out. For the simulation of this topology in symmetric configuration, V_1 and V_2 were taken equal to 12 volts and the other parameters were taken according to Table 3. For simulation of the proposed topology in asymmetric configuration, V_1 and V_2 were taken equal to 12 and 36 volts, respectively, and the other parameters were taken according to Table 3.

Table 3. Parameters used in the simulation of the symmetrical and asymmetrical configurations.

Parameters	Attributes
Switches (T_1 to S_4)	IGBT/Diode
Switching frequency (f_s)	50 Hz
Load (purely resistive)	100 Ω ,
Capacitors C_1, C_2	2200 μ F, 4300 μ F

Figure 8 shows the output voltage waveform and load current for the symmetric configuration (9 levels) of the proposed topology under R load for M at unity. Figure 9a

shows the output voltage and current for dynamic change in modulation index and Figure 9b shows the total harmonics distortion (THD) in output voltage for symmetric configuration. Figure 10 show the voltage across capacitor C_1 (2.5% ripple) and capacitor C_2 (2.5% ripple) under the symmetric configuration. Figure 11 shows the waveforms of load current and output voltage for the asymmetric configuration (17 levels) of this topology at $M = 1.0$ with a purely resistive load. From these figures, it is confirmed that the proposed topology has the capability to generate all positive and negative voltage levels. A gain factor of 40 was taken to multiply the load current in order to have its scale be the same as that of the output voltage. While Figure 12a shows the voltage and current during dynamic change in the load from resistive to resistive-inductive, Figure 12b shows the voltage and current for the asymmetric case for a varying modulation index. THD in output voltage is 9.06% and 4.63% under the symmetric (9 levels) and asymmetric (17 levels) configurations, respectively. Due to the resistive load, the current harmonic spectrum is the same as the load voltage. Figure 13 show the voltage across capacitor C_1 (2.5% ripple) and capacitor C_2 (2.5% ripple) under the asymmetric configuration.

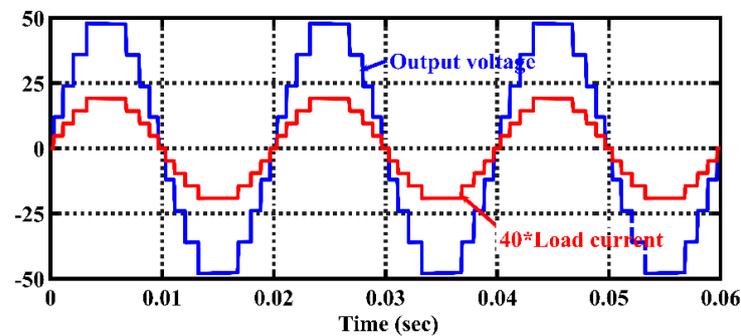
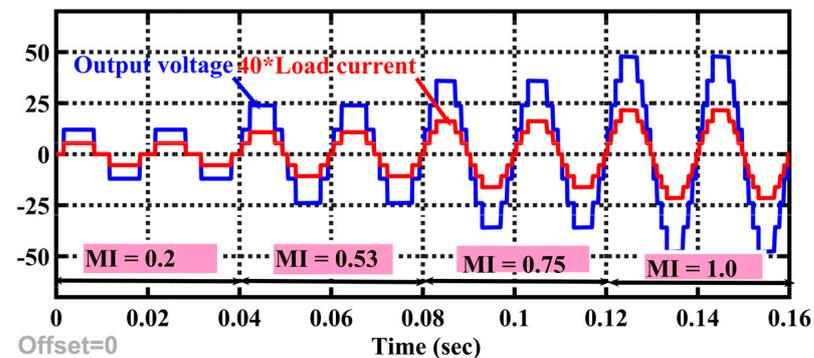
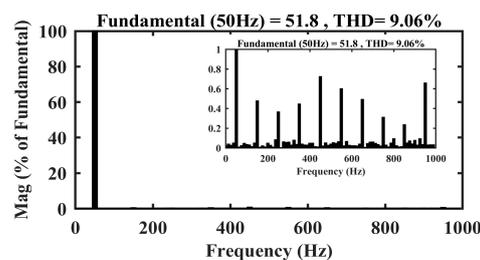


Figure 8. Output voltage and load current for symmetric configuration.



(a)



(b)

Figure 9. (a) Output voltage and current for dynamic change in modulation index and (b) total harmonics distortion (THD) in output voltage for symmetric configuration.

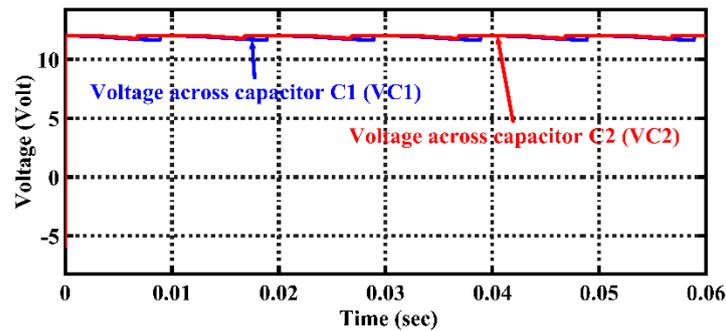


Figure 10. Voltage across capacitors C_1 and C_2 for symmetric configuration.

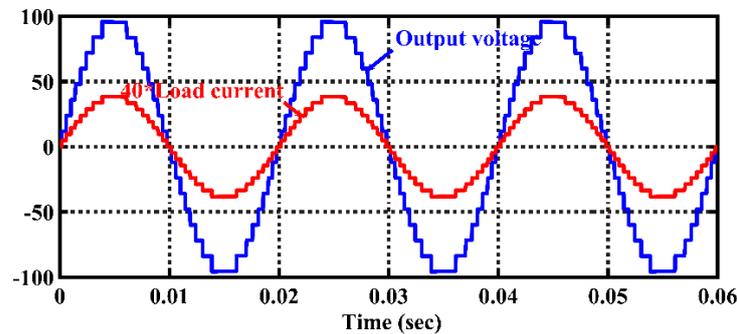


Figure 11. Output voltage and load current for asymmetric configuration.

A laboratory prototype was developed in order to verify the simulation results and performance of the proposed SCMLI topology. Figure 14 shows the setup of the laboratory prototype for the proposed topology. In this experimental work, an Insulated Gate Bipolar Transistor (IGBT) (FGA25N120AND) with rating 1200 V/25 A was utilized as the power electronic switch signals to the switches by interfacing with SIMULINK.

Diode BEC0141 with a rating of 10A was used as the power diodes, an electrolyte capacitor with a rating of 4700 $\mu\text{F}/63\text{V}$ was utilized as the switched capacitors, and TMS320 F28335 (Texas Instruments) was used as a controller for the generation of the gating prototype and controller isolated by using the TLP 250 (TOSHIBA) optocoupler. A Digital Storage Oscilloscope (TPS2024B TEKTRONIX) was employed for the measurement of the waveforms of voltage and current. For the experimental results of the symmetric configuration, voltage sources V_1 and V_2 were taken equal to 12 volts each. This resulted in a 9-level staircase output voltage with a 48-volt peak value, as shown in Figure 15a. Figure 15a also shows the load current when a purely resistive load of 100 Ω was connected at the output. Figure 15b shows the waveform of output voltage and load current when the DC voltage sources were connected across capacitors C_1 and C_2 in the symmetric configuration. Figure 15c,d show the waveform of voltage across capacitors C_1 and C_2 and the waveform of the blocked voltage across switches S_1 and T_1 , respectively, in the symmetric configuration. The peak values of voltage across capacitors C_1 and C_2 are 12 volts. The peak value of the blocked voltage across switches S_1 and T_1 are 12 and 24 volts, respectively, which verify the equations for maximum blocked voltage by switches. For the experimental results of asymmetric configuration, voltage sources V_1 and V_2 were taken 12 volts and 36 volts, respectively. This resulted in a 17-level staircase output voltage with a 96-volt peak value, as shown in Figure 15e under the no-load condition. Figure 15f shows the output voltage and load current waveform when a purely resistive load of 100 Ω was connected at the output. Figure 15g shows the waveform of output voltage (17 levels) and load current to observe the levels clearly. Figure 15h–j show the waveform of the voltage across capacitors C_1 and C_2 , the waveform of blocked voltage across switches S_1 and S_3 , and the waveform of blocked voltage across switches T_1 and T_3 , respectively, in an asymmetric configuration. The peak values of voltage across capacitors C_1 and C_2 are 12

and 36 volts. The peak values of the blocked voltage across switches S1, S3, T1, and T3 are 12, 12, 24, and 72 volts, respectively, which verify the equations for maximum blocked voltage by switches. It is clear that the experimental results have a close agreement with the simulation results.

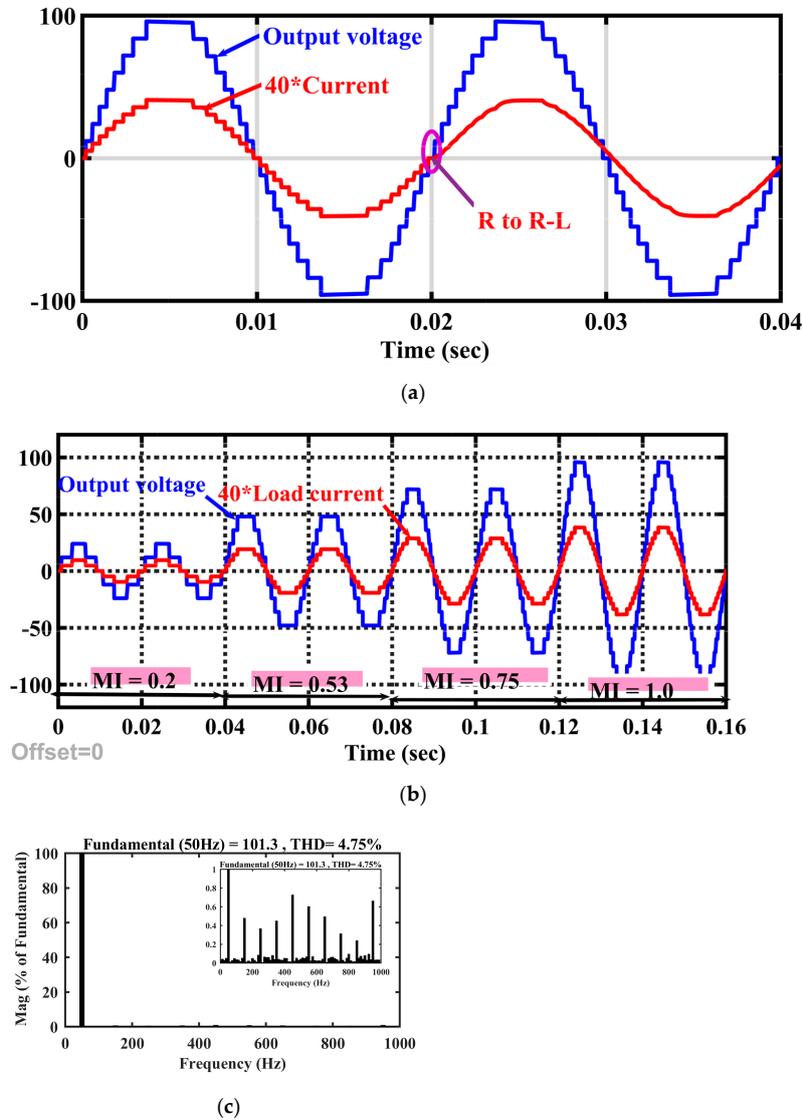


Figure 12. (a) Output voltage and current for change in load from resistive to resistive-inductive, (b) output voltage and current for dynamic change in modulation index, and (c) THD in output voltage for asymmetric configuration.

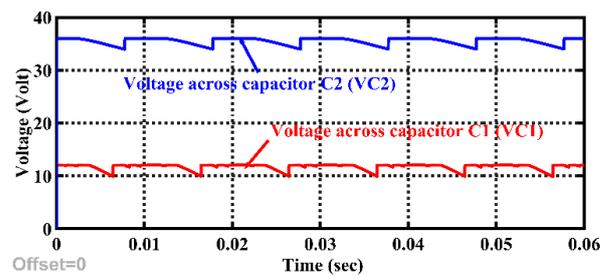


Figure 13. Voltage across capacitors C₁ and C₂ for asymmetric configuration.

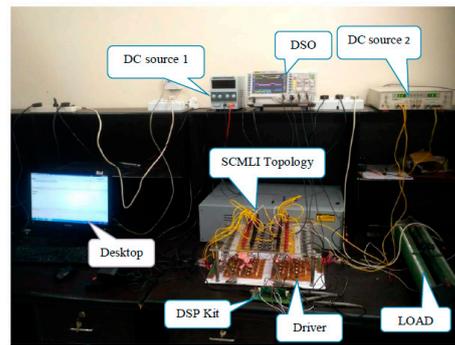


Figure 14. Experimental setup.

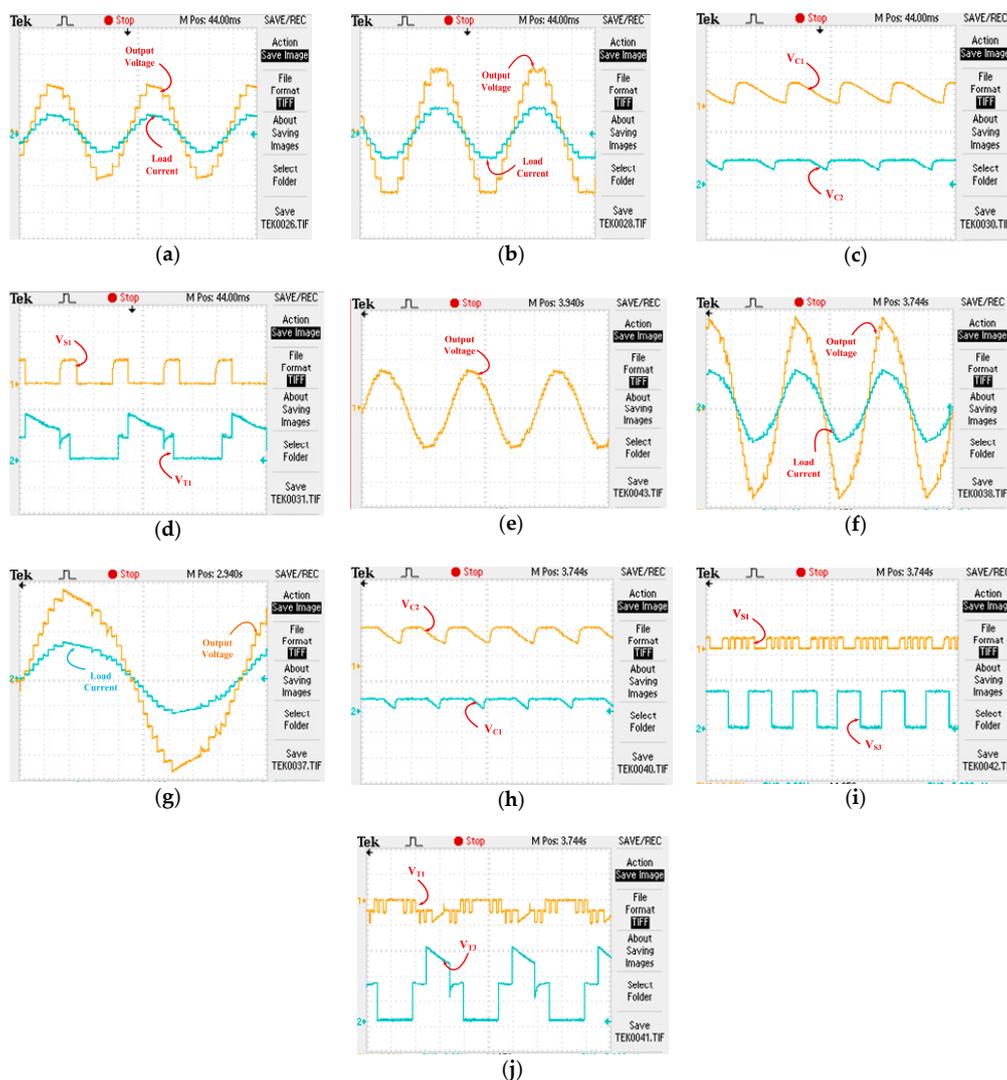


Figure 15. Waveform of (a) output voltage (25 V/div) and load current (1.5 A/div). (b) Output voltage (20 V/div) and load current (0.5 A/div) when the voltage supply of 12 V was connected across both capacitors. (c) Voltage across capacitors C₁ and C₂ (12 V/div). (d) Blocked voltage across switches S₁ and T₁ (12 V/div) in symmetric configuration. Waveform of (e) output voltage (60 V/div) under the no-load condition. (f) Output voltage (20 V/div) and load current (0.75 A/div). (g) Output voltage (20 V/div) and load current (0.75 A/div) for showing one complete cycle (h). Voltage across capacitors C₁ and C₂ (25 V/div). (i) Blocked voltage across switches S₁ and S₃ (25 V/div). (j) Blocked voltage across switches T₁ and T₃ (24 V/div) in asymmetric configuration.

6. Conclusions

In this paper, a generalized structure for the MLI topology was presented. The generalized structures including various basic units and bidirectional switches, and a detailed analysis of this structure for two different methods depending on the selection of voltage sources are also presented. In the topology, capacitor voltages are self-balanced, due to which no voltage balancing algorithm is needed. The comparative study of the generalized structure was performed, and the results show superior performance under various performance parameters. The generalized structure needs less switches, capacitors, drivers, and TSV (in per unit) for a higher level of voltage output. Finally, to validate the performance, the simulation and experimental results were presented for symmetric (9-level voltage) and asymmetric (17-level voltage) configurations for a basic unit. The experimental results validate the performance obtained by simulation. The proposed modular structure is suitable for solar PV application. Moreover, the 9 levels can find application in electric vehicle driven applications. The number of DC power sources becomes higher for a higher level of operation. Future research should focus on the replacement of the DC power supplies with capacitors for a cost-effective solution for high power applications.

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