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Constant-Current, Constant-Voltage Operation of a Dual-Bridge Resonant Converter: Modulation, Design and Experimental Results

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Abstract: To meet the requirements of charging the mainstream rechargeable batteries, in this work, a dual-bridge resonant converter (DBRC) is operated as a battery charger. Thanks to the features of this topology, the required high efficiency can be achieved with a wide range of battery voltage and current by using different modulation variables. Firstly, a typical charging process including constant-voltage stage and constant-current stage is indicated. Then, two different modulation methods of the DBRC are proposed, both of which can realize constant-voltage charging and constant-current charging. Method I adopts phase-shift modulation with constant switching frequency while Method II adopts varying frequency modulation. Furthermore, as guidance for practical application, the design principles and detailed design procedures of the DBRC are customized for the two modulation methods respectively in order to reduce the switching loss and conduction loss. Consequently, the full soft-switching operation with low rms tank current is achieved under the two modulation methods, which contributes to the high efficiency of the whole charging process. At last extensive simulation and experimental tests on a lab prototype converter are performed, which prove the feasibility and effectiveness of the proposed modulation strategies.

Keywords: DC–DC converter; resonant converter; battery charger; constant-current operation; constant-voltage operation

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1. Introduction

Being eco-friendly and energy-saving, transportation electrification has been a rapidly developing technical field in recent years thanks to advanced control technology and new generation high-frequency power semiconductor switches. As an indispensable part of transportation systems, a battery charger plays an important part in electric vehicles (EV), more electric aircraft (MEA) and electric vessel applications. To charge mainstream batteries, the general charging process contains both constant current (CC) charging stage and constant voltage (CV) charging stage in addition to the pre-charge stage and trickle charge stage. The initial CC stage should be applied when the battery voltage is near its minimum value, in which a constant charging current is required to boost the battery voltage. The battery voltage increases continuously in the CC stage until it reaches the rated voltage. In the following CV stage, the output voltage of the battery charger is fixed while the charging current declines gradually. The CV stage will last until the battery is almost charged to its full capacity. In the whole charging process, the battery charger output voltage has a 30–40% variation while the output current ranges from 10% to 100% rated current value. To meet such requirements, the design and control of the charger converter should be carefully planned and implemented.

Many researches about battery charging systems have been reported in the literature. The achievements to improve charging efficiency are attributed to novel topologies, optimal design and control strategies [1–4]. Non-isolated battery charging topologies are able to achieve high performance like the Cockcraft–Walton multiplier and switched inductors-capacitors [5–7]. However, they are not recommended for high power application owing to high switch stress and lack of galvanic isolation. Among isolated battery charging topologies, many converters adopt the full bridge (FB) structure and its variants [8]. A hybrid FB converter integrated with a half-bridge (HB) structure or another FB structure on the primary side is presented in [9,10] where the reduction of conduction loss is realized due to the reduction of circulating current. In order to overcome the narrow zero-voltage switching (ZVS) range of the conventional FB converter at light load, an additional output inductor or clamping capacitor is adopted in [11,12]. However, these solutions increase the manufacturing cost and control complexity.

Because of attractive features such as wide ZVS range of primary switches, zero-current switching (ZCS) of secondary diodes, and good voltage regulation capabilities, the FB resonant converters have attracted lots of attention [13–15]. The typical topology is the LLC-type (inductor-inductor-capacitor) FB resonant converter [16,17], which is generally controlled by frequency modulation. However, due to the wide range variation of output voltage for the battery charger, the switching frequency may have to be away from the resonant frequency. This will cause a series of problems, such as high circulation current, increasing transformer loss and lower efficiency. Therefore, the LLC-type FB resonant converter with frequency modulation is not suitable for the battery charger with wide variation of voltage and current.

In order to avoid the above problems, modified topologies and modulation strategies of FB resonant converters are presented in [18–20]. In [21,22], a phase-shifted modulation method is used to increase the efficiency of FB resonant converter under a light load condition. However, these methods increase the control complexity. In [20,23,24], higher order resonant tanks are used in the FB resonant converters. Nevertheless, complex topologies create difficulties in terms of optimum design, which will increase the cost of the system as well.

This paper focuses on the dual-bridge resonant converter (DBRC) introduced firstly in [25,26]. A DBRC has two FB structures with eight active switches that are implemented on the two sides of a high-frequency (HF) isolated transformer, which provides flexible control options. Two different modulation methods are then proposed for the DBRC with full soft-switching capability and low resonant current, both of which can realize CV and CC charging. The design principles and procedures customized for the two modulation methods are also presented. Verifications of two modulation methods are exemplified through both simulation and actual experimental tests on a 600 W prototype converter.

2. Materials and Methods

A typical charging process with CC stage and CV stage is illustrated in Figure 1. The variations of output current I_o, output voltage V_o and output power P_o during the procedure can be viewed. The resistance $R_L = V_o/I_o$ is the equivalent load resistance, which is used to reflect the instantaneous charging power. In the CC stage, the output current is constant, and the output voltage increases continuously, which indicates an increasing equivalent load resistance. The output power increases in this stage too. In the CV stage, the output current decreases continuously and the output voltage is constant, which means that the equivalent load resistance keeps increasing in the stage. The output power is decreasing in this stage. At the boundary point C, the converter has maximum output power, voltage and current.

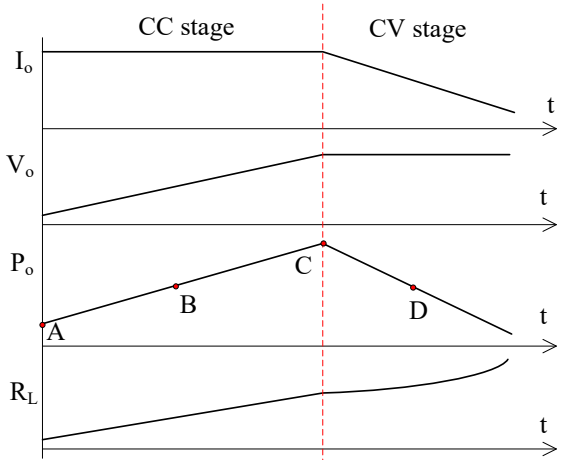


Figure 1. Variations of voltage, current, and power in a typical charging process.

To achieve the required CC and CV charging operation, a DBRC is adopted in this work. Shown in Figure 2, the DBRC has two active full bridges isolated by a HF transformer and a series resonant tank including L_s and C_s. Each full bridge is implemented by four power switches ($S_1 \sim S_4$ on the primary side and $S_a \sim S_d$ on the secondary side) with their anti-parallel body diodes. V_i is the input dc voltage, and V_o is the output dc voltage. C_1 and C_o are filter capacitors on two sides respectively. n_t : 1 is the turns ratio of the HF transformer. Half-bridge, push-pull or three-phase bridge topology can also be used to implement the two bridge-type inverters for different applications. Thanks to the structure, there are multiple control options available for power manipulation, including varying switching frequency, phase-shift and pulse-width modulation, etc. In the following parts, two modulation strategies with related design procedure would be proposed to achieve both CC and CV charing stages with the considerations of low conduction and switching losses.

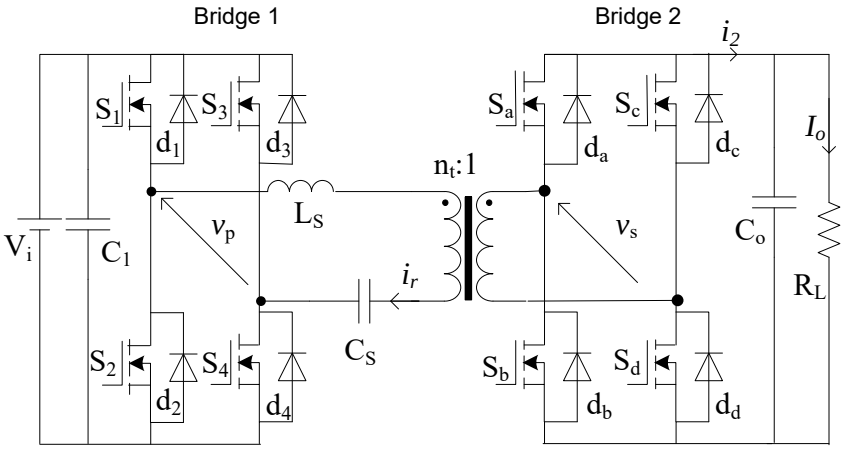


Figure 2. The circuit diagram of a DBRC converter.

2.1. Method I with Constant Frequency Varying Phase-Shift Modulation

Method I is based on phase-shifted modulation with a fixed switching frequency. Generally, the two bridges are operated actively with a phase-shift between them with the typical steady-state waveforms shown in Figure 3. The two voltage sources v_p and v_s are HF ac voltages generated by the two full-bridge converters, respectively. It is assumed

that those two voltages are square-wave voltages with 50% duty cycle, and they can be expressed as

$$\begin{aligned} v_p &= \sum_{n=1,3.}^{\infty} \frac{4V_i}{n\pi} \sin(n\omega_s t) \\ v_s &= \sum_{n=1,3.}^{\infty} \frac{4V_o}{n\pi} \sin(n\omega_s t - n\phi) \end{aligned}$$

where $\omega_s = 2\pi f_s$ is the switching angular frequency (f_s is the switching frequency), ϕ is the phase-shift angle by which v_p leads v_s. v_T is the resonant tank voltage, which is the difference between v_p, $n_t v_s$.

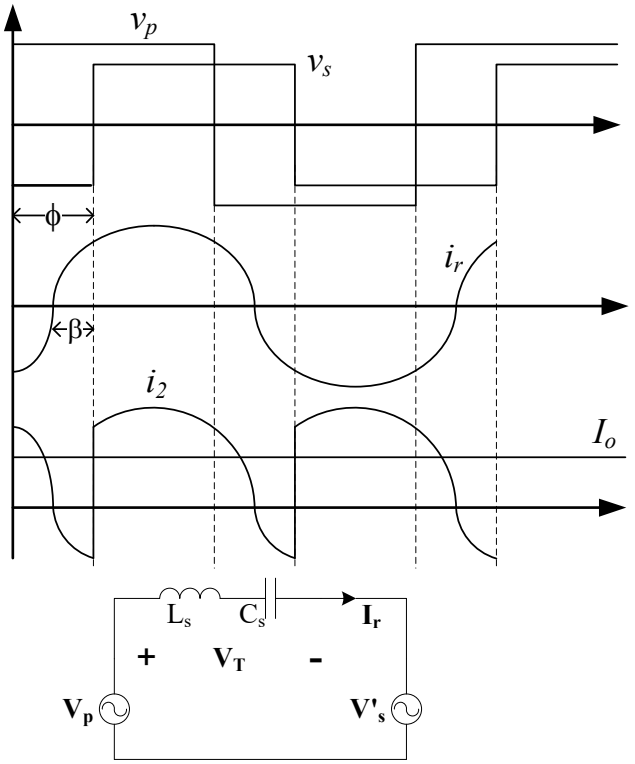


Figure 3. The typical steady-state waveforms of Method I.

Using FHA(fundamental harmonics approximation), the steady-state analysis of the resonant converter can be performed easily with consideration of the fundament harmonics of voltages/currents only. According to [25,26], the active power of the converter can be expressed as

$$P = \frac{8V_i n_t V_o \sin\phi}{\pi^2 X_t} \tag{1}$$

where $X_t = \omega_s L_s - (\omega_s C_s)^{-1}$ is the resonant tank impedance. Therefore, the output current and voltage can be derived respectively as

$$I_o = \frac{8n_t V_i \sin\phi}{\pi^2 X_t} \tag{2}$$

$$V_o = \frac{8n_t V_i R_L \sin\phi}{\pi^2 X_t} \tag{3}$$

It is known that the output current I_o is the average value of the sinusoidal resonant current i_r after active rectification of the secondary bridge.

$$I_o = \frac{1}{\pi}\int_0^{\pi} n_t i_r(\omega_s t) d\omega_s t = \frac{2}{\pi} n_t I_{rP} \cos\beta \tag{4}$$

where β is the phase angle by which v_s lags i_r. Therefore, the peak resonant current is calculated as

$$I_{rp} = \frac{\pi I_o}{2 n_t \cos\beta} \tag{5}$$

In addition, the peak resonant capacitor voltage is evaluated as

$$V_{cp} = I_{rP} \cdot \frac{1}{\omega_s C_s} \tag{6}$$

These two equations can be used to find voltage/current stresses of resonant tank components and switches.

Seen from (2), the output current I_o is related to the input voltage V_i, switching frequency ω_s and the phase-shift ϕ while it is independent of the equivalent load resistance R_L. Regardless of variation of R_L, I_o can be maintained constant as long as V_i, f_s, ϕ are fixed. Meanwhile the output voltage naturally rises from V_{omin} to V_{omax} with the increasing equivalent load resistance R_L according to (3). In other words, the DBRC is able to act as a current source. Therefore, it can be concluded that the CC charging stage can be easily realized without active control measurement due to the inherent feature of the converter itself.

To achieve CV operation, the variation of output resistance in (3) should be compensated by other variables. The controllable parameters include ω_s and ϕ. For the sake of simplicity, the phase-shift ϕ is used as the sole control parameter in this strategy. Apparently, the term $\sin\phi$ should be reduced to compensate for the increase of R_L in the CV stage to regulate output voltage. On the other hand, the declination of $\sin\phi$ will decrease the output current I_o as expected according to (2).

2.2. Design Consideration of Method I

In Figure 4, the phasor diagram of the converter using Method I at different operation points is illustrated, which includes the three voltage phasors $\mathbf{V}_p$, $\mathbf{V'}_s$ and $\mathbf{V}_T$ and one current phasor $\mathbf{I}_r$. According to Kirchhoff Voltage Law, it is seen that

$$\mathbf{V}_p - \mathbf{V'}_s = \mathbf{V}_T = \mathbf{I}_r \cdot jX_t \tag{7}$$

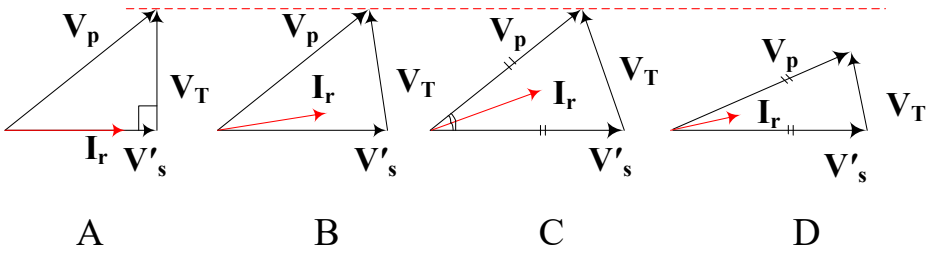


Figure 4. Phasor diagram of the converter of Method I.

In the CC stage (from A to C), the phase angle ϕ is fixed as discussed before, and the length of $\mathbf{V'}_s$ increases continuously. Geometrically, the resonant current phasor $\mathbf{I}_r$ will rotate anti-clockwise with the expanding $\mathbf{V'}_s$. Meanwhile, the length of $\mathbf{I}_r$ increases because of a constant I_o and an increasing β according to (5). $\mathbf{V}_T$ becomes longer too with a constant X_t according to (7). It is known that the necessary ZVS condition for both bridges is that

the current i_r lags v_p and leads v_s. As the operation point moves from A to C, the ZVS margin of the secondary switches becomes larger. To satisfy the ZVS condition in the whole CC stage, this is designed so that the secondary switches work at the boundary of the ZVS range at the beginning of the charging process (point A). As a result, the resonant current $\mathbf{I}_r$ is in phase with $\mathbf{V'}_s$ at the minimum load of the CC stage (point A), at which the voltage phasor triangle is a right-angle triangle.

In the CV stage (from C to D), the converter output current is expected to vary between 100% and 10% of the rated current, which is equivalent to between a full load to 10% of a load. It is well proved in the literature that a DBRC can maintain full ZVS operation of all switches from a full load to zero load only at unity gain theoretically when using phase-shift modulation [26]. Therefore, in order to achieve ZVS operation in the CV stage, the converter voltage gain is fixed at unity, which is also the maximum gain in the whole charging procedure. At the point C which is the boundary between CC and CV stage, the converter is working at maximum output power and voltage. The phasor diagram is an isosceles triangle as $\mathbf{I}_r$ is right between two voltage phasors with same length, i.e., $G_v = 1$ as expected, and β reaches its maximum as $\beta_{max} = \phi_{max}/2$. In the CV stage, the load level decreases with a fixed output voltage. The phasor diagram remains an isosceles triangle with a decreasing ϕ. The resonant current phasor is always between the two voltage phasors $\mathbf{V}_p$ and $\mathbf{V'}_s$, which satisfies the necessary ZVS condition.

2.3. Design Procedure of Method I

The maximum converter gain is calculated as

$$G_{max} = 1 = n_t V_{omax}/V_i \tag{8}$$

The HF transformer turns ratio is calculated as

$$n_t = V_i G_{max}/V_{omax} \tag{9}$$

The minimum gain is found as

$$G_{min} = n_t V_{omin}/V_i \tag{10}$$

The maximum phase-shift in the whole charging process is the same as the phase-shift in the CC stage, which can be calculated geometrically at point A as

$$\phi_{max} = \arccos G_{min} \tag{11}$$

The resonant tank impedance can be evaluated with the help of (2) and (11):

$$X_t = \frac{8 n_t V_i \sqrt{1 - G_{min}^2}}{\pi^2 I_{omax}} \tag{12}$$

In the design, the resonant capacitor peak voltage is selected as a constrain, which is supposed to have an up-limit V_{cp}^* at the maximum power point (point C), and the angle β happens to be half of ϕ_{max} at point C. With the help of (5) and (6), the resonant capacitance C_s is obtained as

$$C_s = \frac{\pi I_{omax}}{2 n_t \omega_s V_{cp}^* \cos\frac{\phi_{max}}{2}} \tag{13}$$

Then, the resonant inductance can be calculated:

$$L_s = \frac{X_t}{\omega_s} + \frac{1}{\omega_s^2 C_s} \tag{14}$$

The variation of phase-shift ϕ in the CV stage can be evaluated by

$$\phi = \arcsin \frac{V_{omax} \sin \phi_{max}}{I_{omax} R_L} \tag{15}$$

2.4. Method II with Varying Frequency Modulation (VF)

The second modulation strategy would adopt switching frequency as the sole variable to manipulate power, and the converter would be operated as a regular series resonant converter (SRC). Therefore, the secondary bridge will act as a diode rectifier or a synchronous rectifier for further low conduction loss. The typical steady-state waveforms can be seen in Figure 5. According to FHA, the secondary side can be regarded as an equivalent resistance

$$R_{ac} = \frac{8 n_t^2 R_L}{\pi^2} \tag{16}$$

and the converter gain is

$$G = \left| \frac{R_{ac}}{R_{ac} + jX_t} \right| = \frac{8}{\sqrt{64 + \pi^4 Q^2 (F - 1/F)^2}} \tag{17}$$

where the quality factor Q and the normalized switching frequency F are defined as

$$Q = \frac{\omega_r L_s}{n_t^2 R_L}; \quad F = \omega_s / \omega_r \tag{18}$$

$\omega_r = \frac{1}{\sqrt{L_s C_s}}$ is the resonant angular frequency.

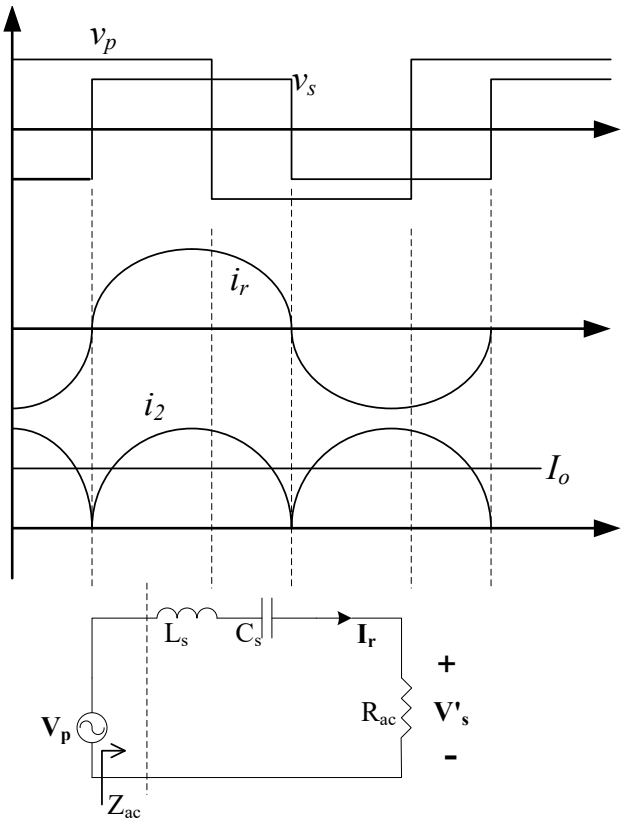


Figure 5. The typical steady-state waveforms of Method II.

According to (17), the converter voltage gain G is unity and is independent of the load at the resonant frequency, i.e., $F = 1$. In other words, the converter acts as an independent voltage source. Doubtlessly, this feature perfectly meets the requirement of CV operation. Therefore, the whole CV stage can be realized by letting the converter work at resonance state.

Referring to the equivalent circuit in Figure 5, the input impedance $Z_{ac} = R_{ac} + jX_t$ should be constant in order to keep a constant output current in the CC stage. Thus, the reactance X_t should be adjusted to compensate for the variation of R_{ac}. Apparently, switching frequency or F has to be reduced when the operation point moves from A to C.

2.5. Design Consideration of Method II

In Figure 6, the phasor diagram of the DBRC at different operation points using method II is illustrated. Starting from point A in the CC stage, the length of phasor $\overline{\mathbf{V}'_\mathbf{s}}$ tends to increase. Since that $\overline{\mathbf{V}'_\mathbf{s}}$ and $\overline{\mathbf{I}_\mathbf{r}}$ will always be in phase, the primary voltage phasor $\overline{\mathbf{V}_\mathbf{p}}$ has to rotate clockwise naturally. As a result, the switching frequency should be reduced to decrease the resonant tank impedance so as to have a shorter $\overline{\mathbf{V}_\mathbf{T}}$ since the resonant current is constant. Viewed from another angle, the term $\sin\phi/X_t$ in (2) should be maintained constant during CC stage. At point C, the switching frequency reaches its minimum—the resonant frequency and $\overline{\mathbf{V}_\mathbf{T}}$ become zero. In the CV stage, $\overline{\mathbf{V}_\mathbf{p}}$ is always equal to $\overline{\mathbf{V}'_\mathbf{s}}$ because of $X_t = 0$. The converter acts as an ideal voltage source, and the output current changes following the reduction of load level or the increasing load resistance. The phasor diagram remains as all phasors are in alignment as indicated at point D of Figure 6.

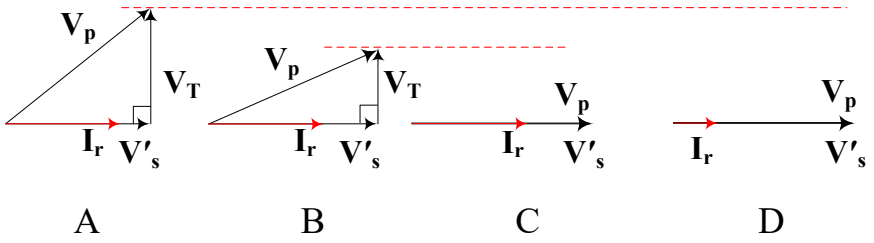


Figure 6. Phasor diagram of Method II.

2.6. Design Procedure of Method II

As mentioned before, the following parameters in the CV stage are selected as $G = G_{max} = 1$ and $F = F_{min} = 1$. Then, the HF transformer turns ratio can be decided as (8) and (9).

A proper value of the minimum switching frequency f_s, i.e., the resonant frequency f_r, can be selected directly now. As a result, the variation of switching frequency in the CC stage should be in a reasonable range.

The maximum capacitor voltage V^*_{cp} is also introduced as a design constraint here. With a selected resonance frequency or minimum switching frequency, the resonant tank can be determined as

$$C_s = \frac{\pi I_{omax}}{2n_t\omega_r V^*_{cp}} \tag{19}$$

$$L_s = \frac{1}{\omega_r^2 C_s} \tag{20}$$

In addition, the normalized switching frequency in the CC stage can be calculated as

$$F = \frac{K + \sqrt{K^2 + 4}}{2} \tag{21}$$

and K is obtained as

$$K = \frac{8\sqrt{1-G^2}}{Q_C} \quad \text{where } G = G_{min} \sim 1 \tag{22}$$

where Q_C is the quality factor at point C.

3. Results

To verify the theoretical analysis above, the two modulation methods will be exemplified through a converter in the same application, whose specifications are listed in Table 1. It is a 600 W charger converter with an input of 120 V. The rated output voltage is 120 V, and the minimum output voltage is 84 V (70% of the rated value). The range of current in the CV stage is 0.5∼5 A (10% to 100% rated current).

Table 1. Specifications of the charger converter.

Rated power	600 W
Input voltage	120 V
ine Output voltage	84∼120 V
ine Output current	0.5 A ∼5 A

Using the design procedures in the previous section, the converter is designed following the two methods, respectively. To be fair, the maximum capacitor voltage V_{cp}^* is selected at 1.5 times of input dc voltage, i.e., 180 V for both cases. The designed parameters are shown in Tables 2 and 3. For Method I, the switching frequency is selected at 100 kHz. Then, the resonant capacitance and inductance can be calculated by using (13) and (14), which in turn result in the resonance frequency of 77.68 kHz. The range of phase-shift angle ϕ is 4.1∼45.57°. For Method II, the resonance frequency is selected at 80 kHz, and the maximum switching frequency is 108 kHz.

Table 2. The design parameters using CFVP.

Transformer turns ratio	1:1
Switching Frequency	100 kHz
ine $M_{min} \sim M_{max}$	0.7 ∼ 1
ine Resonant inductance L_s	55.74 µH
ine Resonant capacitance C_s	75.32 nF
ine Maximum phase-shift ϕ_{max}	45.57°
ine Minimum phase-shift ϕ_{min}	4.1°

Table 3. The design parameters using VF.

Transformer turns ratio	1:1
$M_{min} \sim M_{max}$	0.7∼ 1
ine Resonant inductance L_s	45.60 µH
ine Resonant capacitance C_s	86.81 nF
ine Maximum switching frequency	108 kHz
ine Minimum switching frequency	80 kHz

For the sake of verification, the designed converter with proposed modulation was simulated in PSIM firstly. To approximate the actual implementation, non-ideal parameters are included in the simulation setup purposely. A dead-band of 2° is inserted into the gating signals. The on-state resistance of MOSFET is set at 50 mΩ, and the built-in barrier of anti-parallel diode is assumed to be 0.5 V.

As shown in Figure 7, a simulation block diagram and two prototype converters with the two sets of designed parameters are also built and tested. IPP60R099P7 is used for all

MOSFET switches in the two bridges. The transformers are made with ETD49 ferrites core. The two inductors are made with PQ35 ferrites core.

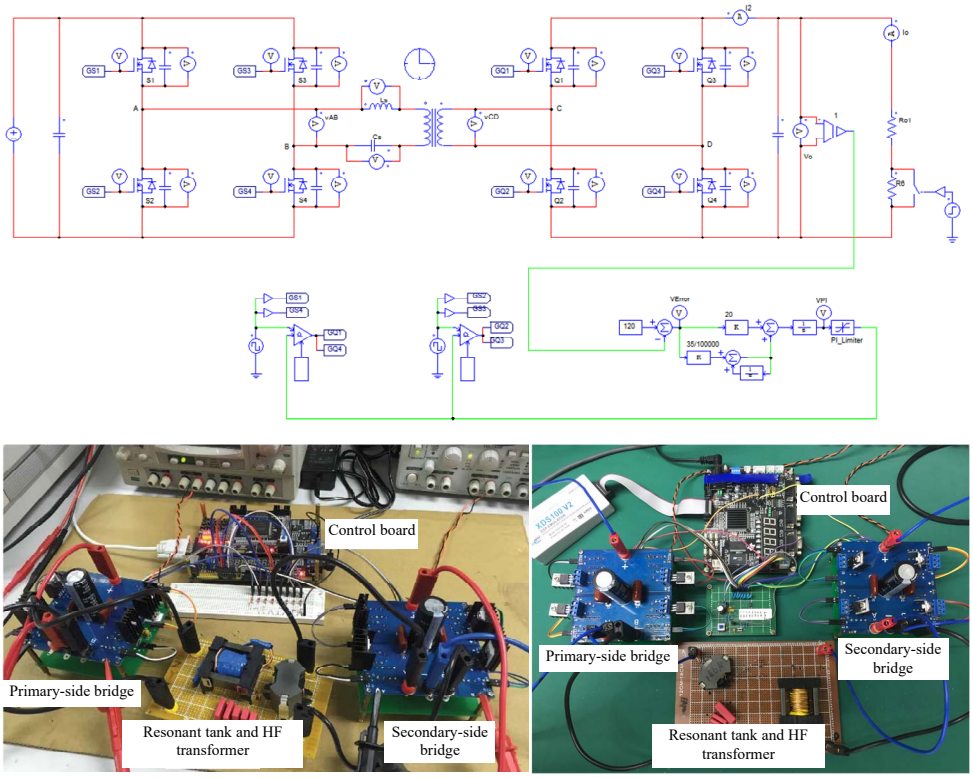


Figure 7. Simulation block diagram and experimental prototype

In Figures 8 and 9, waveforms of five cases obtained from simulation (left part) and experiment (right part) are illustrated for two modulation methods, respectively. The five cases are 70% rated voltage, 90% voltage in the CC stage, the rated/peak power case, 80% rated current, and 50% rated current in the CV stage. In each case, waveforms of v_p, v_s, v_c, i_r (from top to bottom) are captured and shown together.

Generally, the shape of those simulation waveforms has a close match with that of experimental ones in all cases. The first three cases correspond to points A, B and C in the CC stage. The output voltage rises from 84 V to 108 and 120 V, respectively, while the output current is always 5 A. It can be seen that the phase-shift ϕ and switching frequency are kept constant in Figure 8a–c for Method I. For Method II, in Figure 9a–c, it is seen that the secondary side voltage is always synchronous with the resonant current, and the switching frequency is varied in this procedure. In cases 4 and 5, the converter is in the CV stage with V_o regulated at 120 V, and the output current is around 4 A (80% load) and 2.5 A (50% load). For Method I in Figure 8d,e, the phase-shift ϕ is kept to be reduced, and the amplitudes of v_p and v_s are always the same with unity gain. For Method II in Figure 9d,e, v_p and v_s are always the same, and the resonant current is in phase with both voltages due to the resonance operation. Moreover, it is a fixed frequency and free-of-control CV stage.

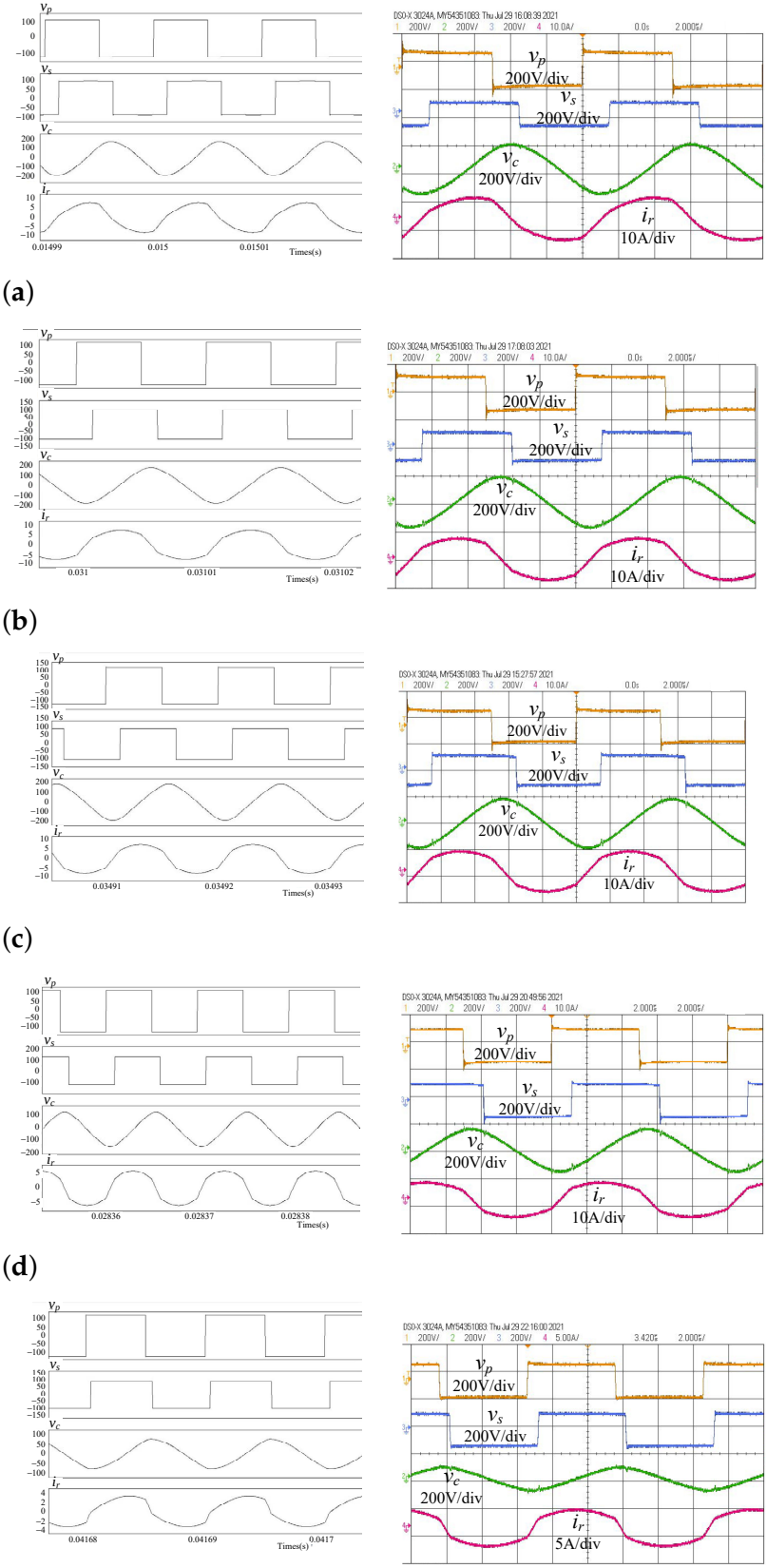
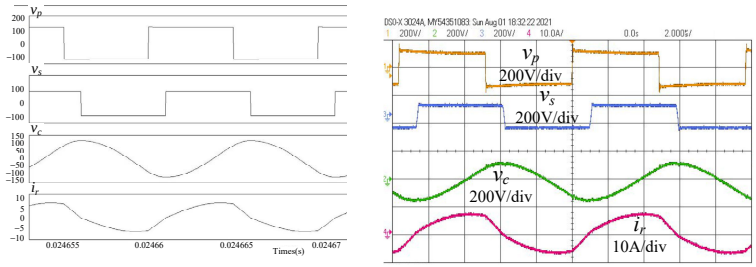
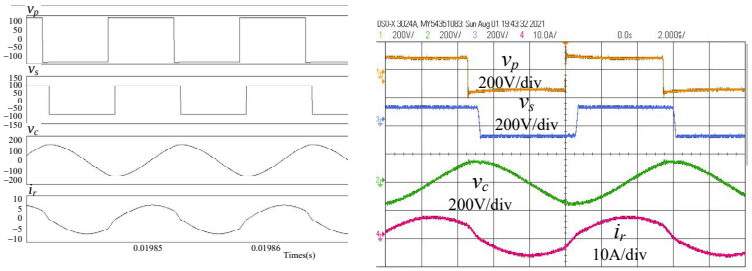


Figure 8. Simulated (left) and experimental (right) waveforms of v_p, v_s, v_c, i_r with Method I: (**a**) V_o = 84 V, CC; (**b**) V_o = 108 V, CC; (**c**) V_o = 120 V, I_o = 5 A; (**d**) I_o = 4 A, CV; (**e**) I_o = 2.5 A, CV.



(**a**)



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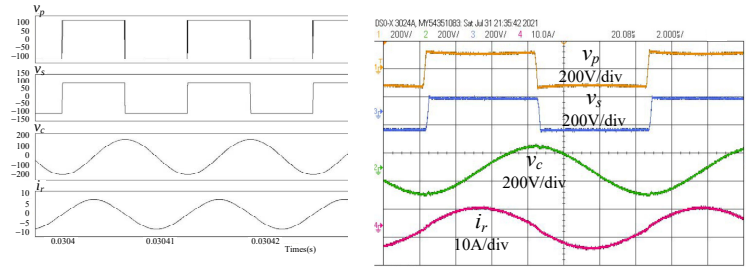

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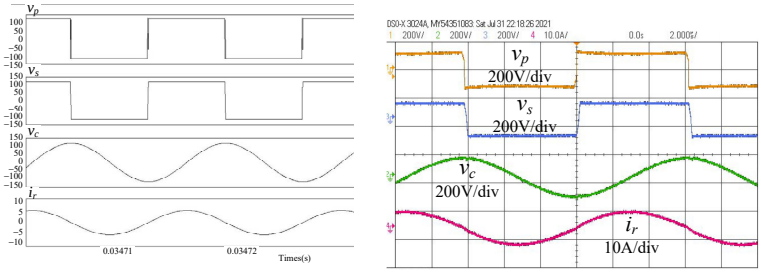

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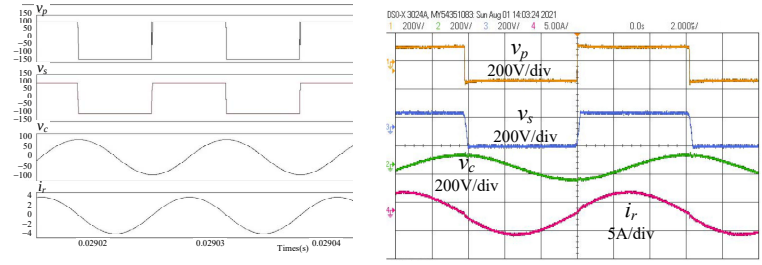

(**e**)

Figure 9. Simulated (left) and experimental (right) waveforms of v_p, v_s, v_c, i_r with Method II: (**a**) V_o = 84 V, CC; (**b**) V_o = 108 V, CC; (**c**) V_o = 120 V, I_o = 5 A; (**d**) I_o = 4 A, CV; (**e**) I_o = 2.5 A, CV.

In Figure 10, the drain-to-source voltage of switches in both bridges (S_1 and S_a) and the resonant current are put together to show the soft-switching behavior. The necessary condition of ZVS operation can be confirmed if the turn-on drain-to-source current of the switch is negative. In Method I, all switches can work in the ZVS operation except for the secondary switch at rated output power case working at the boundary of ZVS. In Method II, the primary switches can always maintain ZVS in the CC range and work with ZCS in the CV stage. The secondary bridge actually works as a synchronous rectifier so that all secondary switches work at ZCS in both CC and CV stages.

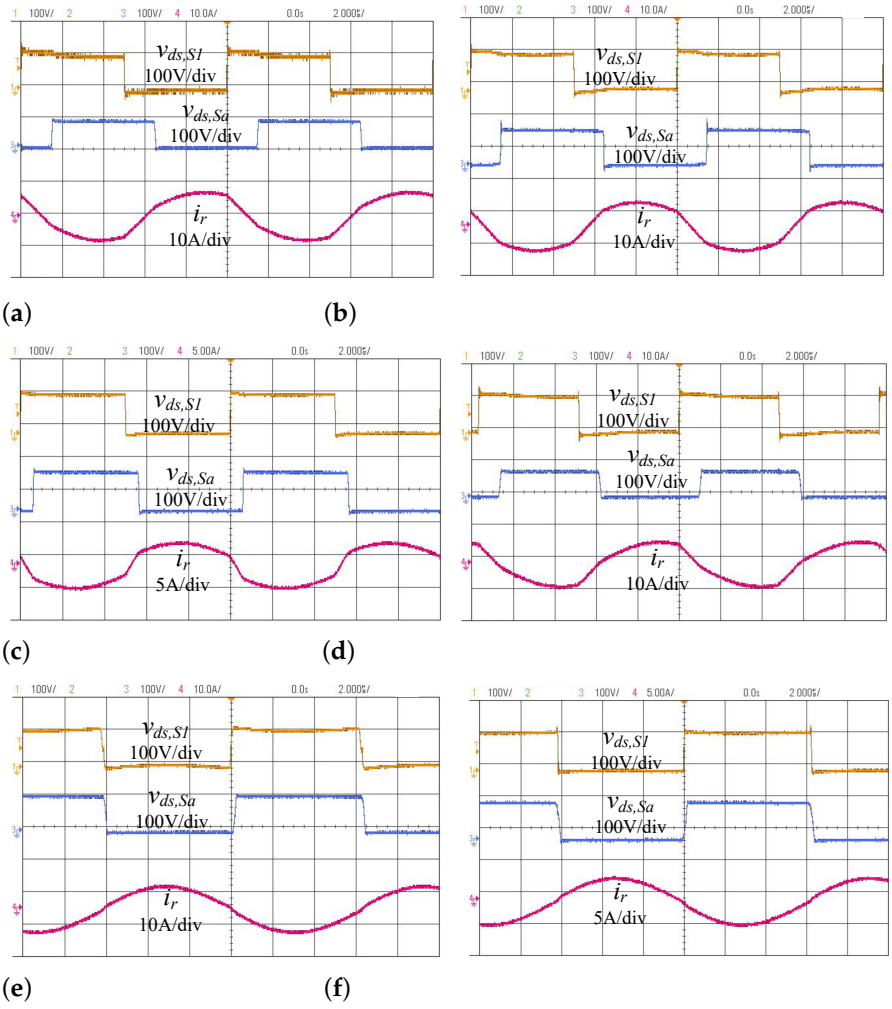

Figure 10. Switch voltages of S_1, S_a and resonant current i_r: (**a**) V_o = 84 V, CC, Method I; (**b**) V_o = 120 V, I_o = 5 A, Method I; (**c**) I_o = 2.5 A, CV, Method I; (**d**) V_o = 84 V, CC, Method II; (**e**) V_o = 120 V, I_o = 5 A, Method II; (**f**) I_o = 2.5 A, CV, Method II.

4. Discussion

In Tables 4 and 5, theoretically calculated, simulated and experimental values of important parameters are collected and listed together for comparison. Generally, values from simulation and experiment are quite close and those also match the theoretical calculations with acceptable deviation. The mismatch can be attributed to two reasons: non-ideal values in simulation setup and parasitic parameters in experimental implementation, and the inherent errors from FHA. For example, the existence of necessary dead-band is the main reason of the deviation of phase-shift ϕ, while the on-state resistance of switches and threshold voltage of diodes have impacts on actual phase-shift and switching frequency too. In addition, to cope with the wide variation of output voltage and load level, the switching frequency is not quite close to resonant frequency in some operation range. Under such

a scenario, the resonant current does not resemble a sinusoidal shape well, which can be easily identified in Figures 8a,b and 9a,b. Therefore, the peak current values from the three sources have relatively large deviations. Comparatively, the rms current values have smaller deviations, and their variation in experiment coincides with that of load level, which implies better partial load efficiency. The peak capacitor voltage in the experiment is clamped below 187 V, which is close to the designed value.

Table 4. Comparisons of parameters using Method I.

Load		70% (CC)	90% (CC)	100%	80% (CV)	50% (CV)
V_{cp}(V)	cal.	165.96	172.34	180.0	139.16	84.38
	sim.	167.3	177.67	187	144.25	88.55
	exp.	171.75	178.88	187.5	144.75	88.75
I_{rp}(A)	cal.	7.85	8.16	8.52	6.59	3.99
	sim.	7.47	7.52	7.76	5.90	3.56
	exp.	7.48	7.63	7.81	6.19	3.48
I_{rs}(A)	cal.	5.55	5.77	6.03	4.66	2.82
	sim.	5.54	5.73	6.04	4.62	2.80
	exp.	5.69	5.74	5.95	4.71	2.50
$\phi(^\circ)$	cal.	45.6	45.6	45.6	34.9	20.9
	sim.	45.4	45.4	45.4	34.2	20.5
	exp.	52.4	52.4	52.4	41.4	22.0

Table 5. Comparisons of parameters using Method II.

Load		70% (CC)	90% (CC)	100%	80% (CV)	50% (CV)
V_{cp}(V)	cal.	133.55	149.77	180.02	144.01	90.01
	sim.	139.58	157.05	179.04	143.39	89.76
	exp.	137.5	155	184.25	142.5	91.25
I_{rp}(A)	cal.	7.85	7.85	7.85	6.28	3.93
	sim.	7.63	7.35	7.81	6.26	3.86
	exp.	7.5	7.39	7.53	6.19	3.75
I_{rs}(A)	cal.	5.55	5.55	5.55	4.44	2.78
	sim.	5.54	5.46	5.53	4.42	2.73
	exp.	5.18	5.13	5.12	4.18	2.69
f_s(kHz)	cal.	107.84	96.15	80	80	80
	sim.	103.33	91.80	80	80	80
	exp.	103.32	91.92	80.65	80.65	80.65

The measured efficiency of the two designed converters in the whole charging process is presented in Figure 11. It is seen that the efficiency of Method I is higher than that of Method II in the whole charging process in a range of 0.1∼4.29 percentage. The highest efficiency and lowest efficiency of Method I are 93.32% and 77.73%, respectively, while those values of Method II are 92.8% and 72.9%. For both of methods, the highest efficiency is measured at the rated peak power (120 V/5 A), and the lowest efficiency is measured at 70% output voltage in the CC stage (84 V/5 A). The efficiency can be further improved, especially in the CC stage at light load condition. One possible approach is to use more

modulation variables and the trade-off will be higher control complexity, which are to be addressed in separated works.

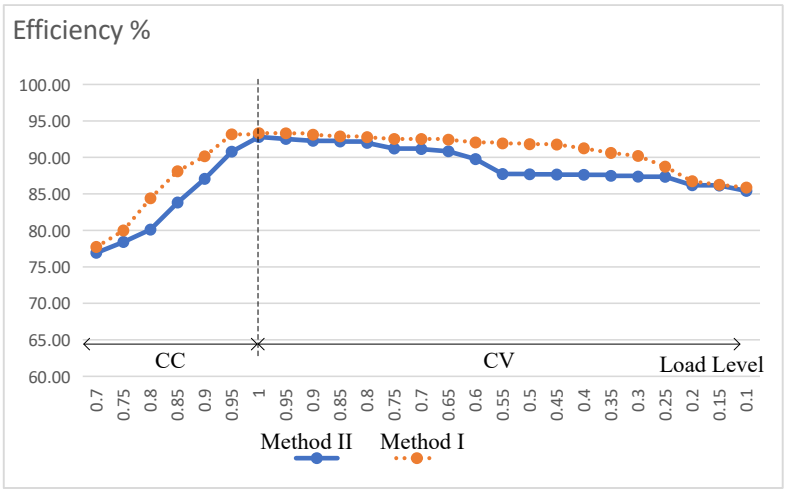

Figure 11. Measured efficiency of two proposed modulation methods.

5. Conclusions

In this paper, a DBRC is operated for battery charging application. Taking advantage of the flexible control options associated with the converter itself, two modulation methods are analyzed, designed, simulated and tested experimentally. The major contributions include: (1) Constant-current and constant-voltage operation can be achieved through proper modulation strategies. Both of them can be realized with full soft-switching and low rms tank current as well. (2) The operating characteristics of the converter with two modulation methods are comprehensively analyzed, which is universal for related researches. (3) The design procedures are extensive and representative, which provides guidance for industrial design and operation. The measured efficiency of the phase-shift based method (Method I) is higher than that of another frequency-based method. The main loss source is the conduction loss, which may be further reduced using a new generation silicon-carbide power transistor. Moreover, the two methods can be extended by adding more modulation variables to achieve different optimization objectives.

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