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A Modified Multi-Winding DC–DC Flyback Converter for Photovoltaic Applications

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Featured Application: This topology is applied to photovoltaic generation conversion using multiple panels and a single magnetic core, using MPPT and obtaining an efficiency over 96%.

Abstract: DC–DC power converters have generated much interest, as they can be used in a wide range of applications. In micro-inverter applications, flyback topologies are a relevant research topic due to their efficiency and simplicity. On the other hand, solar photovoltaic (PV) systems are one of the fastest growing and most promising renewable energy sources in the world. A power electronic converter (either DC/DC or DC/AC) is needed to interface the PV array with the load/grid. In this paper, a modified interleaved-type step-up DC–DC flyback converter is presented for a PV application. The topology is based on a multi-winding flyback converter with N parallel connected inputs and a single output. Each input is supplied by an independent PV module, and a maximum power point tracking algorithm is implemented in each module to maximize solar energy harvesting. A single flyback transformer is used, and it manages only 1/N of the converter rated power, reducing the size of the magnetic core compared to other similar topologies. The design of the magnetic core is also presented in this work. Moreover, the proposed converter includes active snubber networks to increase the efficiency, consisting of a capacitor connected in series with a power switch, to protect the main switches from damaging dv/dt when returning part of the commutation energy back to the source. In this work, the operating principle of the topology is fully described on a mathematical basis, and an efficiency analysis is also included. The converter is simulated and experimentally validated with a 1 kW prototype considering three PV panels. The experimental results are in agreement with the simulations, verifying the feasibility of the proposal.

Keywords: DC–DC power conversion; solar energy; energy conversion; multi-winding flyback transformer

Citation: Pesce, C.; Riedemann, J.; Peña, R.; Degano, M.; Pereda, J.; Villalobos, R.; Maury, C.; Young, H.; Andrade, I. A Modified Multi-Winding DC–DC Flyback Converter for Photovoltaic Applications. *Appl. Sci.* **2021**, *11*, 11999. https://doi.org/10.3390/app112411999

Academic Editor: Katarzyna Antosz

Received: 16 November 2021
Accepted: 14 December 2021
Published: 16 December 2021

1. Introduction

Renewable energy is becoming increasingly important for future sustainability. Nowadays, photovoltaic (PV) systems are growing, with an estimated worldwide installed capacity of about 871 GW in 2022 [1,2]. A photovoltaic module converts solar irradiation into DC electrical energy. To connect a PV system to a load/grid, the DC voltage needs to be processed by means of a DC/DC or DC/AC power electronics converter. Different

circuit configurations can be employed to connect PV panels to power converters, such as central or string arrangements [3]. However, it has been verified that module-level power conversion, i.e., each PV module with an individual power converter, provides the best solar energy harvesting capability and the best tracking of the global maximum power point [3,4]. Regarding the converter topologies currently employed in the field of module-level power conversion, the flyback converter [5,6] is gaining popularity since it provides important benefits such as galvanic isolation, high power density, easy voltage step-up, and low number of components [4]. Moreover, paralleling flyback units is a straightforward way to deal with the harmful mismatch effects among PV modules. However, for the flyback topology to be competitive with other circuit configurations, challenges related to the conversion efficiency and system reliability must be met [7].

Several articles in the literature report the application of flyback converters to PV systems [8–16]. Most of these works are based on an interleaved topology that consists of splitting a full converter into several standard flyback cells, each managing a part of the converter overall power [15,16].

An input-parallel output-parallel (IPOP) interleaved flyback converter is presented in [8], where two flyback cells are considered, and a single-phase inverter is connected between the DC/DC stage and the grid. The reduction of the current ripple as well as the reduction of the size of the passive elements are mentioned as a contribution.

For the same IPOP interleaved flyback topology, in [9], a control scheme based on selecting the operating mode of the flyback cells (discontinuous conduction mode (DCM), boundary conduction mode, or a combination of both) is proposed to optimize the efficiency. These operating modes are further investigated in [10] for a grid-tied interleaved flyback microinverter, aiming to optimize the efficiency in a wide load range.

In [11], an IPOP interleaved converter based on three flyback cells is presented. In this case, as the number of parallel DC/DC cells increases, the current ripple is reduced, as well as the size of the passive filtering element. An input-parallel output-series (IPOS) interleaved flyback converter is described in [12]. This circuit configuration can achieve a higher output voltage compared to the IPOP topology; however, the output diodes' current rating is rather high.

The integration of harmonic injection capability into an interleaved flyback inverter is thoroughly investigated in [13]. This method is studied for the implementation of an active anti-islanding scheme. Moreover, a mathematical model is proposed to accurately predict the steady-state behavior of the converter, either in grid-tied or in islanding operation.

To obtain soft switching on the converter, an active clamp circuit is introduced in [14], allowing a considerable reduction of the switching losses of the topology.

Regarding the application of DC-DC converters based on a single input and multiple outputs, different approaches can be found in the literature [17–22]. There are also approaches that use multiple winding transformers [23–25], although those with a single input and multiple outputs are the most frequent uses.

The aims could be to supply several cascade-connected H-bridges to generate a multilevel AC output [17,18], to connect the output in series to obtain a high DC voltage [19], or to supply independent loads with different voltage levels (depending on the number of turns of the secondary windings) [20–22].

For converters with multiple inputs and a single output, in [23], a two-input buck-boost converter is presented. One input receives power from the grid, whereas the other is connected to a PV array. The power of both inputs is combined to supply a resistive load. In [24], a DC–DC topology that can be supplied by independent DC sources is shown. The DC input voltages are converted into AC voltages by means of half-bridge inverters, then a multi-winding transformer transfers the power from all the primary inputs to the secondary output where another half-bridge converter transforms the AC voltage into DC voltage to finally supply a load. A disadvantage is that the transformer should manage the total converter power, and the number of bulky capacitors will be two times the number of inputs. Finally, a multi-input DC–DC topology for renewable energy applications with

battery backup is proposed in [25]. The converter is based on the standard flyback topology, but additional diodes and an auxiliary switch are included to allow a safe switch between the renewable energy inputs and the batteries.

In this paper, a N-modules flyback interleaved power converter with parallel connected inputs and a single output is proposed for a PV generation system. The circuit configuration is built by using a single transformer (one core) with N primary windings and one secondary winding. This represents an advantage in terms of cost and volume compared to the conventional interleaved IPOS topology [12], where the number of individual transformers (individual cores) equals the number of flyback modules. With this structure, the output diode operates N times more in a cycle (than conventional interleaved converters), and the output capacitor can therefore be smaller. For the classical problems of flyback topologies (leakage inductance) [15], active snubber circuits are added to provide protection to the main switches against dv/dt during commutation. The snubber circuits return the energy of the leakage inductance to the input capacitor of the PV, then increasing the efficiency of the topology. The proposed power converter is depicted in Figure 1 (with N = 3). More than three PV panels can be implemented in applications where it is required to increase the system power. The proposed converter is intended for applications with low input voltage and high current; the DC output voltage can be used to supply single-phase grid-tied inverters or hydrogen production with photovoltaic cells [26–29]. On the other hand, a maximum power point tracking (MPPT) algorithm is implemented to extract the maximum power available in the PV modules [30].

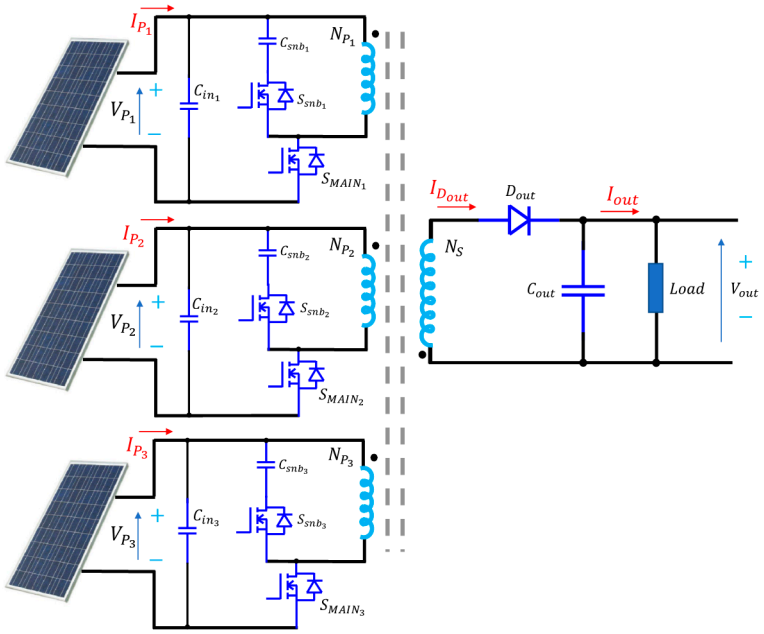


Figure 1. Topology proposed, with $N = 3$ PV panels.

The rest of the work is organized as follows. Section 2 thoroughly describes the operating principle of the converter. Section 3 presents the implemented MPPT scheme. In Section 4, guidelines about the transformer's core design are presented, whereas in Section 5 a description of the converter input capacitor design is reported. Simulations results are shown in Section 6, and Section 7 presents the obtained experimental results. In Section 8, efficiency results are show. The conclusions of the work are stated in Section 9.

2. Operating Principle

The analysis of the converter and its different operating modes was done under the following assumptions: semiconductor devices are ideal, single-core ferrite coupled inductors (flyback transformer) have unitary coupling coefficient and unity turns ratio ($N_{P,n} : N_S = 1$, where n refers to the n-th primary windings); the resistances are neglected, and the leakage

inductance is L_{l_N}; the converter operates in current discontinuous conduction mode (DCM) and steady state. Two duty cycles are defined: d_1 for main switches (S_{MAIN}) and d_2 for the snubber switches (S_{snb}). The magnetizing inductance is L_m, the switching frequency is f_s, and the commutation period is T_s. The general aspects of the operation of this topology were based on extracting the energy from the PV panels connected to the converter in a single switching period T_s. The flyback transformer was designed to manage the power from a single PV panel and not from all the panels together; this made it possible to reduce the size of the magnetic core. The switching period was divided in segments depending on the number of primary windings; hence, in this work, T_s was divided in three sections. The purpose of the snubber network was to recover the energy stored in the flyback transformer leakage inductance and limit the main switches dv/dt. The leakage inductance current charged the snubber capacitor, and then that current was returned to the input capacitor C_{in} through the antiparallel diode of the main switch. This process improved the efficiency of the topology. The operating principle consisted in six stages for each PV panel used. Since in this paper $N = 3$ is considered, the total number of stages per switching period was 18. Figures 2–7 shows the first six stages per period, for the first PV panel. The main equation will be described for each state.

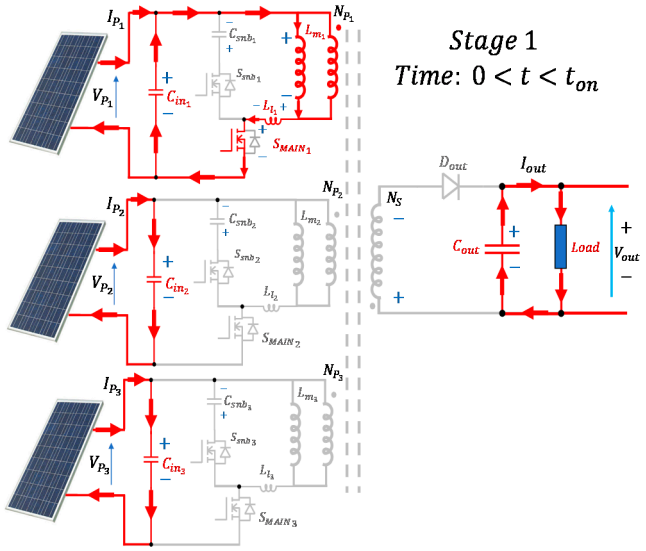


Figure 2. Stage 1, time: $0 < t < t_{on}$.

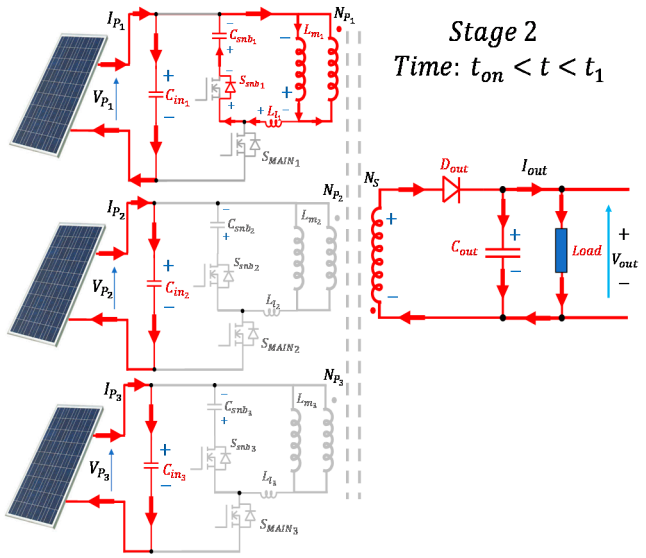


Figure 3. Stage 2, time: $t_{on} < t < t_1$.

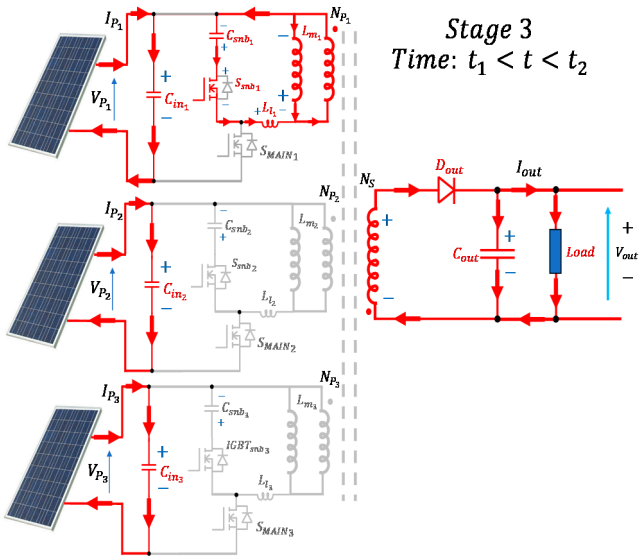


Figure 4. Stage 3, time: $t_1 < t < t_2$.

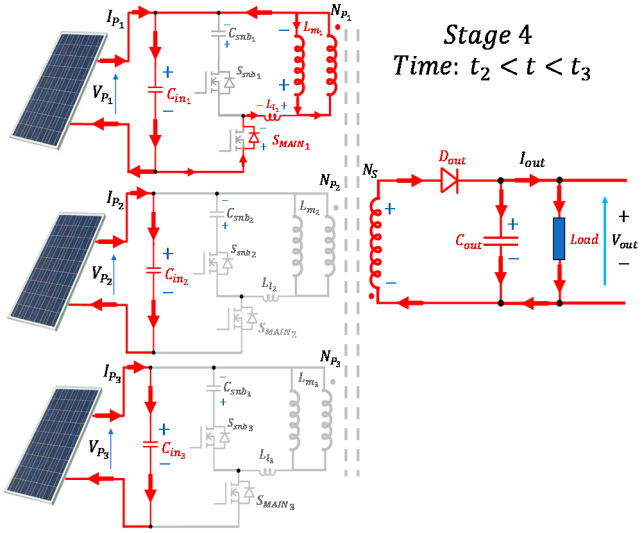


Figure 5. Stage 4, time: $t_2 < t < t_3$.

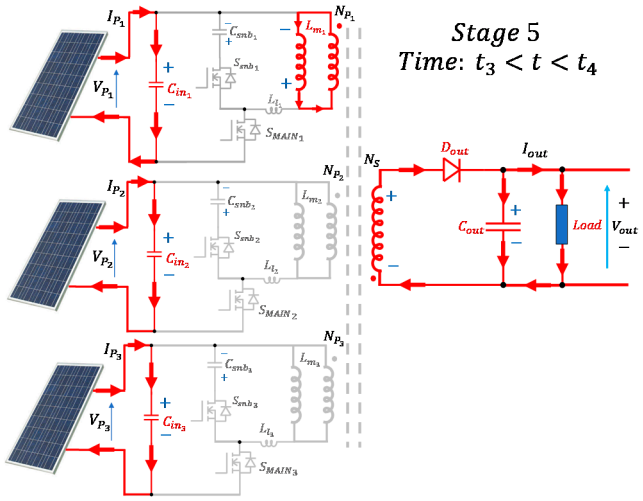


Figure 6. Stage 5, time: $t_3 < t < t_4$.

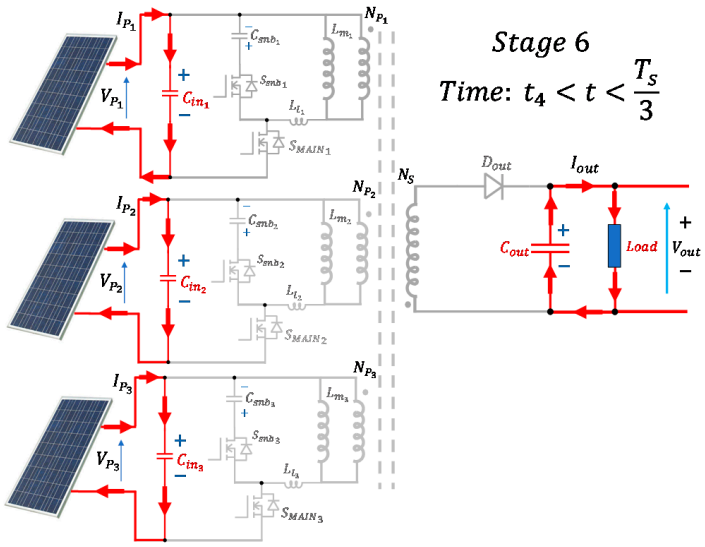


Figure 7. Stage 6, time: $t_4 < t < T_s/3$.

2.1. Stage 1: $0 < t \leq t_{on}$

As can be seen in Figure 2, at this stage only S_{MAIN_1} is activated. The energy extracted from PV panel 1 is stored in the magnetizing inductance L_m of the flyback transformer. The maximum and average currents in the switch are defined by (1) and (2), respectively. On the other hand, the snubber capacitor C_{snb_1} is charged (from the previous cycle) to a voltage defined by Equation (3)

$$I_{S_{MAIN_{MAX}}} = \frac{V_{P1}\, d_1}{(L_m + L_{l1}) f_s} \tag{1}$$

$$I_{S_{MAIN_{AVG}}} = \frac{V_{P1}\, d_1^2}{2(L_m + L_{l_1}) f_s} \tag{2}$$

$$V_{C_{snb1}}(0) = \frac{\left(\frac{V_{P1}\, d_1}{(L_m + L_l) f_s}\right) L_l}{\tan\left(\frac{d_2\, T_s}{2\sqrt{L_l\, C_{snb1}}}\right)} + V_{out} \tag{3}$$

The average current of S_{snb1} and the C_{snb1} are zero for energy balance of the snubber circuit that absorbs energy from L_{l_1} and delivers energy to C_{in_1}. The output diode D_{out} is turned off and does not transfer energy to the output capacitor C_{out}.

2.2. Stage 2: $t_{on} < t \leq t_1$

Figure 3 shows the S_{MAIN_1} turned off. The magnetizing current (defined by (4)) decreases and flows through the output diode D_{out} (defined in (5)) and the diode of the snubber switch S_{snb1}. The S_{snb1} diode conducts current from L_m to C_{snb1} through the leakage inductance L_{l1}; this current is defined by Equation (6). The voltage in C_{snb1} increases and it is defined by Equation (7). On the other side, the diode D_{out} will be forward biased by the secondary winding, and a current will flow, charging the output capacitor C_{out}; this current is defined by Equation (5). Part of the magnetizing current is stored in the leakage inductor and flows into the snubber circuit. The voltage in the leakage inductance (Equation (7)) allows to define the snubber capacitor voltage expression in Equation (8). At $t = t_1$, the current in the snubber capacitor decreases to zero. In this stage, the magnetizing inductance voltage is $V_{L_m} = -V_{out}$.

2.3. Stage 3: $t_1 < t \leq t_2$

In Figure 4, only the device S_{snb1} is activated. The energy delivered by the leakage inductance L_{l1} to the snubber capacitor C_{snb1} is now returned to the leakage inductance L_{l1}. For energy balance, the average current in the snubber capacitor C_{snb1} is zero.

$$i_{L_m}(t) = -\frac{\frac{V_{P1}\, d_1}{(L_m+L_{l1})}\, V_{out}}{V_{P1}\, d_1}\, t + \frac{V_{P1}\, d_1}{(L_m + L_{l1}) f_s} + i_{L_{l1}}(t) \tag{4}$$

$$I_{D_{out}} = i_{L_m}(t) - i_{L_{l1}}(t) \tag{5}$$

$$\begin{aligned} i_{L_{l1}}(t) &= i_{C_{snb1}}(t) \\ &= \frac{V_{out} - V_{C_{snb1}}(0)}{L_{l1}} \sqrt{L_{l1} C_{snb1}} \sin\left(\frac{1}{\sqrt{L_{l1} C_{snb1}}} t\right) \\ &+ I_{L_{m_{max}}} \cos\left(\frac{1}{\sqrt{L_{l1} C_{snb1}}} t\right) \end{aligned} \tag{6}$$

$$\begin{aligned} v_{L_{l1}}(t) &= L_{l1} \frac{d i_{C_{snb1}}(t)}{dt} \\ &= V_{out} - V_{C_{snb1}}(0) \cos\left(\frac{1}{\sqrt{L_{l1} C_{snb1}}} t\right) \\ &- I_{L_{m_{max}}} \frac{L_{l1}}{\sqrt{L_{l1} C_{snb1}}} \sin\left(\frac{1}{\sqrt{L_{l1} C_{snb1}}} t\right) \end{aligned} \tag{7}$$

$$V_{L_m} + v_{L_{l1}} - v_{C_{snb1}} = 0 \rightarrow v_{C_{snb1}} = v_{L_{l1}} + V_{L_m} \rightarrow v_{C_{snb1}} = v_{L_{l1}} - V_{out} \tag{8}$$

At $t = t_2$, the leakage inductance current, given by Equation (6), is maximum but it circulates in the opposite direction than in Stage 2. For $t = t_2$, the snubber capacitor recovers the initial voltage of Stage 1. The output diode current $i_{D_{out}}$ is given by Equation (9), and the main switch blocking voltage is given by Equation (10).

$$i_{D_{out}}(t) = i_{L_m}(t) - i_{L_{l1}}(t) \tag{9}$$

$$V_{DSmain1_{off}} = v_{L_{l1}}(t) + V_{L_m} - V_{C_{in1}} \;\rightarrow\; V_{DSmain1_{off}} = v_{L_{l1}}(t) - V_{out} - V_{P_1} \tag{10}$$

2.4. Stage 4: $t_2 < t \leq t_3$

Figure 5 shows that S_{snb1} is now disactivated. The leakage inductance current flows through the magnetizing inductance, the input capacitor C_{in1}, and the diode of the main switch. The energy stored in the leakage inductance is returned to the input capacitor C_{in1}, increasing the conversion efficiency. At $t = t_3$, the leakage inductance current decreases to zero, the leakage inductance voltage $V_{L_{l1}}$ is defined by Equation (11), and the time when the leakage inductance current decreases to zero can be calculated by Equation (12). In the secondary winding, the output diode current starts to decrease because the energy stored in the magnetizing inductance was delivered to the output capacitor. Additionally, this current also flows to the load.

$$V_{L_{l1}} = V_{P_1} - V_{L_m} \;\rightarrow\; V_{L_{l1}} = V_{C_{in1}} + V_{out} \tag{11}$$

$$t_3 - t_2 = V_{L_{l1}} \cdot \frac{d_2\, T_s}{2(V_{Cin1} + V_{out})} \tag{12}$$

2.5. Stage 5: $t_3 < t \leq t_4$

In Figure 6, S_{MAIN1} and S_{snb1} are turned off. The output diode current decreases to zero at $t = t_4$. The output diode turn-on time is defined by Equation (13).

$$t_4 - d_1 T_s = \frac{V_{C_{in1}}\, d_1 T_s}{V_{out}} \;\rightarrow \Delta t_4 = \frac{V_{P_1}\, d_1 T_s}{V_{out}} \tag{13}$$

2.6. Stage 6: $t_4 < t \leq T_s/3$

In Figure 7, all the switches are deactivated. The energy stored in the output capacitor C_{out} is delivered to the load. The output capacitor current is defined by (14).

$$I_{C_{out}} = -I_{out} \tag{14}$$

2.7. Stage 7 to 12: $T_s/3 < t \leq 2T_s/3$

The six stages described above consider the energy extraction from PV panel 1. Then, the next six stages, that is, from Stage 7 to Stage 12, will correspond to the energy extraction from PV panel 2 (Figure 8). The energy extraction from PV panel 2 is similar to that performed in PV panel 1, and the operation mode is the same as described for the first six stages. Therefore, the equations are the same, but the time interval goes from $T_s/3$ (for Stage 7) to $2T_s/3$ (for Stage 12).

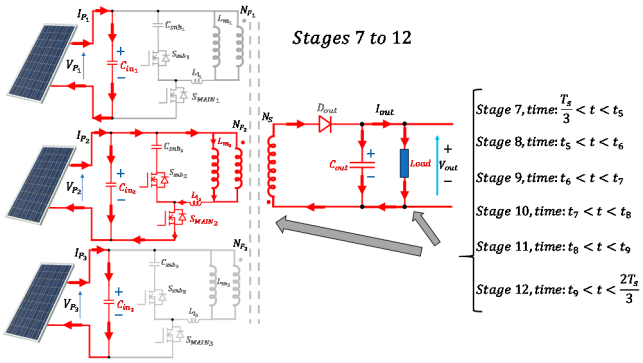


Figure 8. Schematic of stages 7 to 12, time: $T_s/3 < t < 2T_s/3$.

2.8. Stage 13 to 18: $2T_s/3 < t \leq T_s$

For the final six stages, that is, from Stage 13 to 18, as shown in Figure 9, energy extraction from PV panel 3 is carried out. Again, the operation and mathematical expressions are the same as described for the first PV panel, but now in a time interval from $2T_s/3$ (for Stage 13) to T_s (for Stage 18).

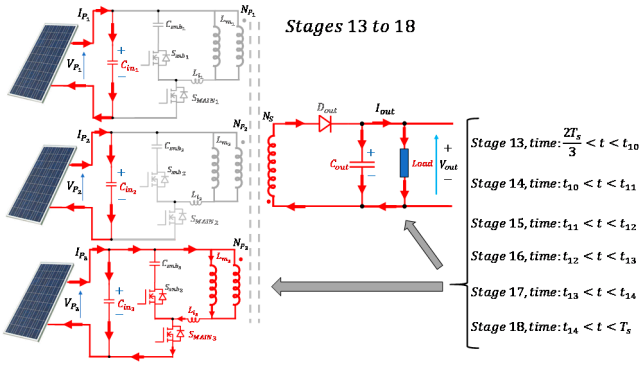


Figure 9. Schematic of stages 13 to 18, time: $2T_S/3 < t < T_s$.

3. Maximum Power Point Tracking

To ensure the extraction of the maximum power available from the PV array, an MPPT algorithm must be used [28,29]. In this work, the perturb & observe (P&O) method for MPPT was implemented [30]. Figure 10 shows a scheme regarding the MPPT implementation for the proposed topology, where each converter module, and consequently each PV panel, uses an independent P&O algorithm to maximize the power extraction from the PV array. Figure 11 shows the control scheme applied to each PV panel, where the subscript i refers to the i-th flyback primary winding. The MPPT method generates a voltage reference

for the corresponding PV panel output capacitor. This reference is processed by a closed-loop control strategy based on a proportional integral controller. The output of the voltage controller is a duty cycle to regulate the gating signals of the main and snubber switches.

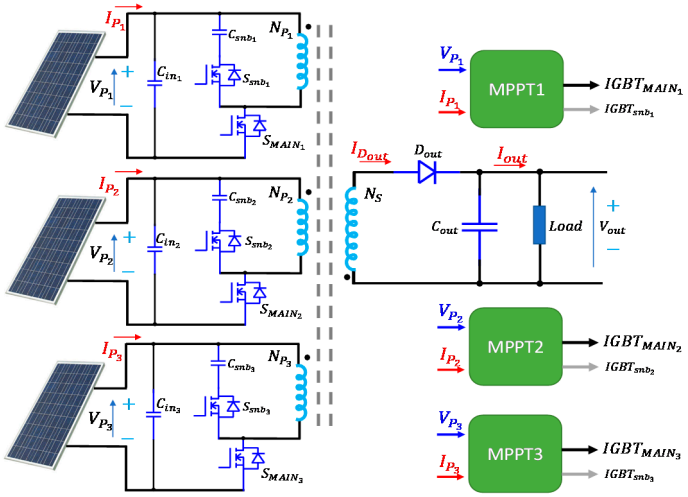


Figure 10. Schematic of the MPPT for the topology proposed.

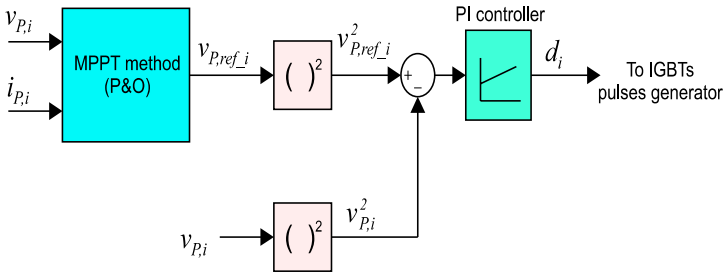


Figure 11. MPPT control scheme for each PV module.

4. Flyback Transformer Core Design

In this work, the flyback transformer core considered a U-type-geometry ferrite-based core (N27 and N87 Siferrit® materials). Joining two U-type magnetic cores, an O-type core is formed, obtaining two symmetrical air gaps, as can be seen in Figure 12. According to this geometry, and considering the approach in [31], the expression that relates the product of the areas of the window A_w and transversal A_e to the parameters of the circuit is defined by Equation (15), where d_{max} is the maximum duty cycle, $i_{prim_{rms}}$ is the rms primary winding current, ΔB is the differential magnetic density, K_P is the primary utilization factor, K_W is the utilization factor of the winding area, and J is the current density. Since the converter operated in DCM, the expression (15) can be rewritten in terms of the input power, obtaining Equation (16), where P_{in} is the input power of one PV panel. The expression that defines the air gap δ in terms of input power is defined by Equation (17).

$$A_e A_w = V_{in}\, d_{max} \frac{i_{prim_{rms}}}{\Delta B\, f_s\, K_P\, K_W\, J} \tag{15}$$

$$A_e A_w = P_{in}\, \frac{\sqrt{4/3}}{\Delta B\, f_s\, K_P\, K_W\, J\, \sqrt{d_{max}}} \tag{16}$$

$$\delta = P_{in}\, \frac{2\,\mu_0}{B^2\, f_s\, A_e} \tag{17}$$

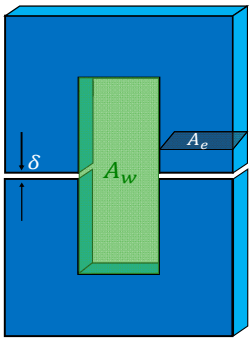


Figure 12. O-type ferrite core for each flyback transformer.

As can be seen in Equations (16) and (17), the input power is proportional to the product $A_e\ A_w$ and the air gap δ. In the proposed topology, since each converter input module transferred energy to the secondary side during a period T_s/N, the average power processed by the transformer in a switching period T_s was only the one produced by a single PV panel, whereas the total power managed by the converter corresponded to that generated by the N PV panels (three in this work). Therefore, the core was designed to process only one-third of the total power. This is an advantage in terms of cost–volume compared to other flyback topologies where the transformer must be designed for the total converter power [11–13,16].

5. Input Capacitor Design

In this section, a brief analysis of the input capacitor C_{in} is presented. In steady state and operating at rated power, the nominal duty cycle was approximately $d_{nom} = 0.25$, and the maximum duty cycle (limited by the switching period $T_s/3$ since three PV panels were being used) was $d_{max} = 0.33$. In this work, PV panels rated at 340 W and with nominal voltage and current of 37 V and 9.18 A, respectively, were used.

According to the current waveform in the input capacitor C_{in} (in parallel with the PV panel), the area under the ΔQ curve in the charging cycle must be equal to the discharge area due to the energy balance in the capacitor.

The area under the discharging curve (Figure 13) is formed by the turned-off time of the main switch, and the maximum amplitude of the current is $\Delta I_{C_{in}} + I_{C_{inmin}}$, where $I_{C_{inmin}}$ is the minimum capacitor current amplitude.

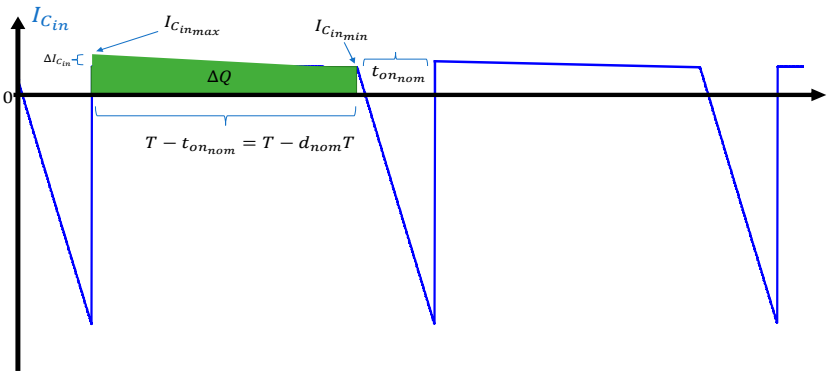


Figure 13. Simulated input capacitor current.

Assuming an ideal operation, in one commutation period, this area is equal to the average current delivered by a PV panel and defined by $I_{PV_{DC}}$. Thus, ΔQ is defined by Equation (18), and C_{in} is defined by Equation (19), where ΔV_{PV} is the PV panel voltage ripple desired:

$$\Delta Q = (T_s - d_{nom}T_s)I_{DC_{PV}} = C\Delta V_{PV} \quad (18)$$

$$C_{in} = \frac{(1 - d_{nom}) I_{DC_{PV}}}{\Delta V_{PV} \cdot f_s} \tag{19}$$

6. Simulation Results

In this section, the simulation results are presented. The simulation parameters are shown in Table 1. Each PV panel received different solar irradiance, i.e., PV1: 900 W/m^2, PV2: 1000 W/m^2, and PV3: 800 W/m^2. This allowed us to verify the operation of the topology and the MPPT algorithm, with different duty cycles for the individual flyback modules.

Table 1. Simulation parameters.

Description	Parameter
PV panels power	340 [W$_P$]
Input capacitors, $C_{in_1} = C_{in_2} = C_{in_3}$	100 [µF]
Output capacitors, C_{out}	470 [µF]
Snubber capacitors, $C_{snb_1} = C_{snb_2} = C_{snb_3}$	0.1[µF]
Magnetizing Inductance, L_m	17 [µH]
Flyback transformer turn ratio, N_{P_n}/N_S	1
Leakage inductances, $L_{l_1} = L_{l_2} = L_{l_3}$	0.5 [µH]
Load (resistive)	100 [Ω]
Number of primary windings, N_P	3
Switching frequency, f_s	10 [kHz]

Figure 14 shows four waveforms. Figure 14a shows the control signals of the main and snubber switches. As can be noted, to protect the devices, there was a dead time between the gating signals of the main and the snubber switches. Active snubbers allowed the drain-source voltages of the main switches not to exceed the allowed ratings and to reduce the dv/dt (this is further shown in the experimental results). Figure 14b shows the currents in the main switches and in the output diode. Slightly different peak values can be appreciated in the three switches currents due to the different solar irradiances. Figure 14c,d shows the voltages and currents of the solar modules, respectively, where again, different magnitudes can be observed. The performance of the individual MPPT implemented for each PV panel was then verified, considering different irradiance conditions.

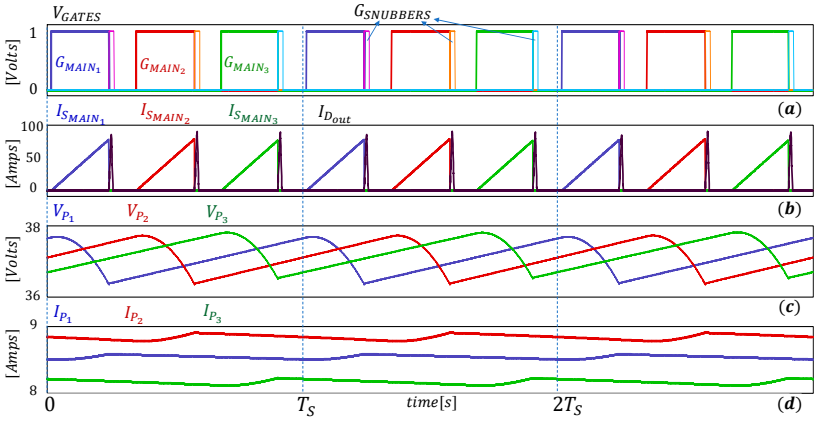


Figure 14. Simulated waveforms: (**a**) Main and snubber switches gate control signals. (**b**) Main switches drain currents and output diode current. (**c**) PV panels' voltage. (**d**) PV panels' current.

Figure 15 shows five waveforms. The switches voltages are shown in Figure 15a–c and it can be seen that their magnitudes did not exceed 200 V. In Figure 15d, the output voltage is depicted, which had an average value of 320 V. Finally, Figure 15e shows the power in the PV panels (green) and the output power of the proposed converter (blue).

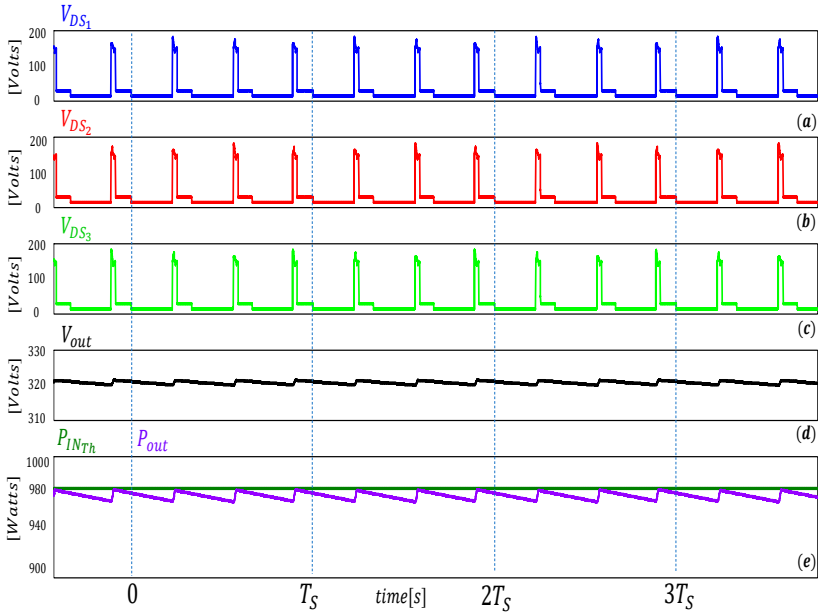


Figure 15. Simulated waveforms: (**a**–**c**) Drain-source main switches' voltages. (**d**) Output voltage. (**e**) Input and output power.

In Figure 16, the operation of the MPPT can be observed. The power available in the solar panels is shown in green, and the converter output power in purple. Step changes in the solar irradiance were applied. The converter output power closely followed the input available power, validating the correct operation of the MPPT algorithm.

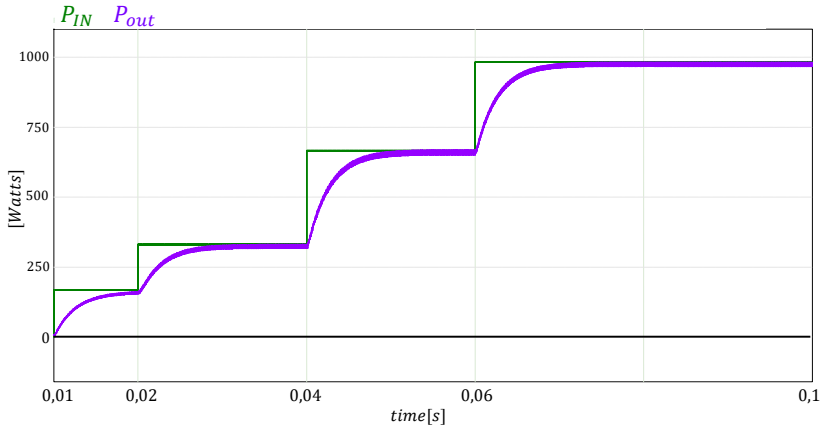
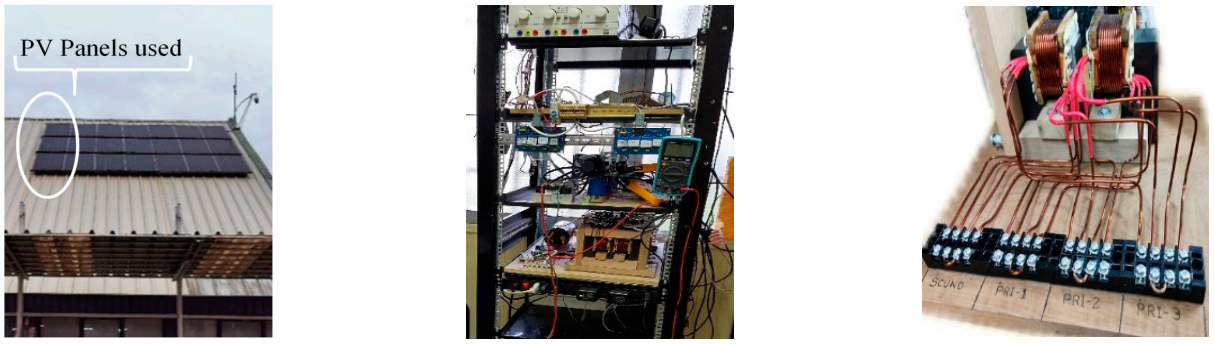


Figure 16. Simulation waveforms. Input power (dark green) and output power (purple).

7. Experimental Results

A power converter laboratory prototype was built, and the photovoltaic installation available at the Electrical Engineering Department of the University of La Frontera in Temuco, Chile, was used (see Figure 17a). In Figure 17b, the implemented setup for the proposed topology is shown, and in Figure 17c, the flyback transformer designed and built for the converter is presented. The system parameters are the same as those of the simulations presented in Table 1. A digital signal processor Texas Instrument F28379D was used as a control platform. Optical fiber was used for the transmission of the semiconductors gating signals. For the main switches, MOSFETs IPW65R041CFD were used, and for the snubber switches, MOSFETs model TK20A60W were considered. The diode model STTH9012TV was used in the converter output. The output capacitor C_{out} is in polypropylene to obtain a low series equivalent resistance allowing an increase in the conversion efficiency. The model of the PV panels used was CSUN340-72P, rated at

340 Wp. The experimental system was validated with the same levels of radiation for each PV panel.



(**a**) (**b**) (**c**)

Figure 17. (**a**) PV panels used to test the converter. (**b**) Laboratory experimental setup. (**c**) Flyback transformer built with three primary winding and three secondary windings.

Figures 18–21 were obtained around 12 PM. Figure 18 shows the voltages of the three PV panels and the converter output voltage. It can be noted that the magnitude of the three average voltages was the same (~37 V). The voltage ripple was due to the action of the MPPT control that worked at a frequency of 10kHz. On the other hand, a very low ripple can be observed in the converter output voltage waveform (green) which had an average value of 311 V.

Figure 19 shows the currents of the PV panels (blue, pink, and yellow) and the converter output current (green). The magnitude of the output current was constant and equal to 3.1, while a resistive load of 100 Ω was supplied.

Figure 20 shows the main switches' voltages. The maximum values did not exceed 170 V. In classical flyback topologies, the energy stored in the transformer leakage inductance produces a dv/dt on the main switch; in this work, this problem was solved with the proposed active snubber. This snubber limited the dv/dt and injected the energy stored in the transformer's leakage inductance back to the input capacitor C_{in}, increasing the conversion efficiency. The waveforms were similar to the simulated ones shown in Figure 15.

Figure 21 shows the currents on each main switch and the output diode current. The peak current of the main switches was approximately 68 A. For the output diode, the peak current was about 80 A.

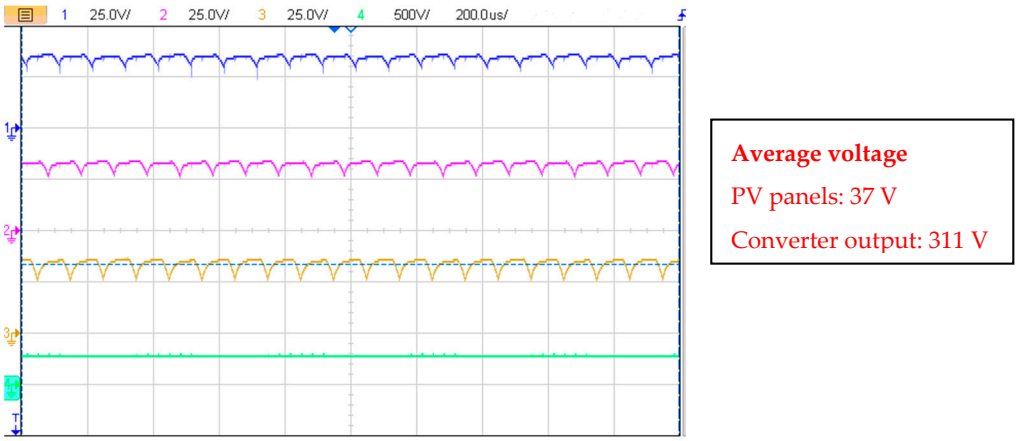


Figure 18. Experimental waveforms. Input voltages: PV panel 1 (blue), PV panel 2 (pink), and PV panel 3 (yellow); scale: 25 V/div. Converter output voltage (green); scale: 500 V/div. Base time: 200 µs/div.

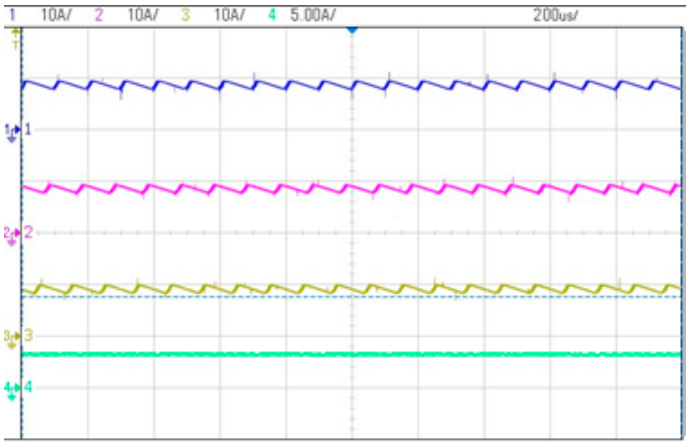


Figure 19. Experimental waveforms. PV panels' currents: PV panel 1 (blue), PV panel 2 (pink), and PV panel 3 (yellow); scale: 10 A/div. Converter's output current (green); scale: 5 A/div. Base time: 200 µs/div.

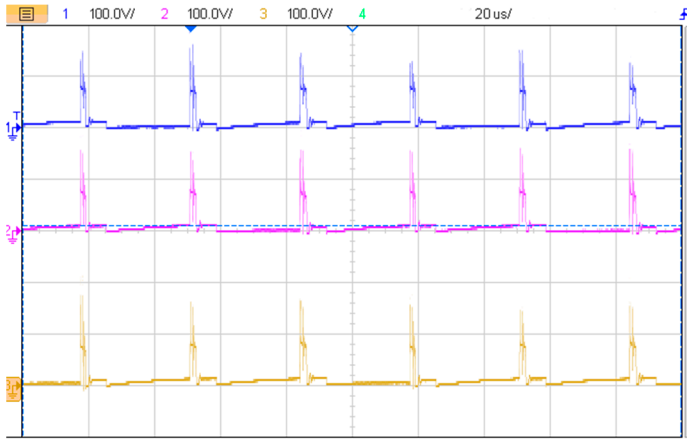


Figure 20. Experimental waveforms. Drain-source voltage: main switch 1 (blue), main switch 2 (pink), and main switch 3 (yellow); scale: 100 V/div. Base time 20 µs/div.

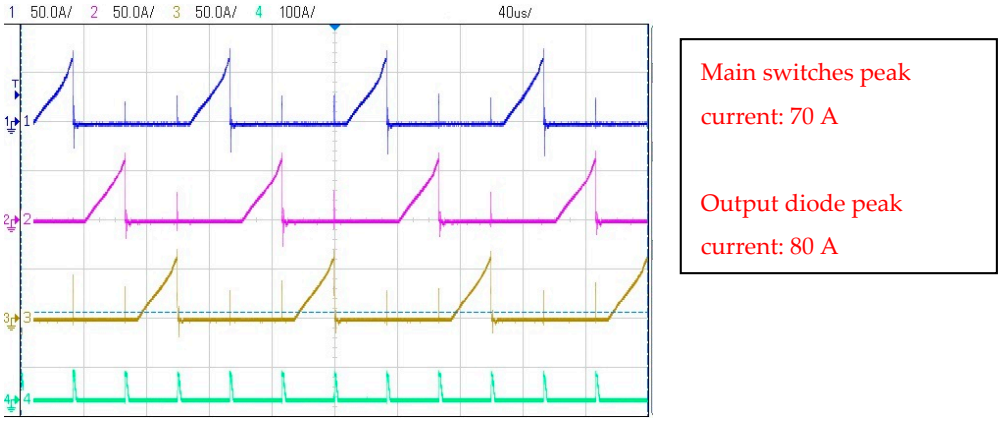


Figure 21. Experimental waveforms. Current: main switch 1 (yellow), main switch 2 (pink), and main switch 3 (yellow); scale 50 A/div. Output diode current (green); scale: 100 A/div. Base time Base time 40 µs/div.

The experimental results of Figures 22 and 23 were obtained while operating the converter in the afternoon, close to sunset, when solar irradiation is much lower than at noon. Thus, a reduction in the main switches' currents and the output diode's current can

be appreciated in Figure 22. The maximum magnitude of the main switches' currents was approximately 25 A, and that of the output diode's was 35 A.

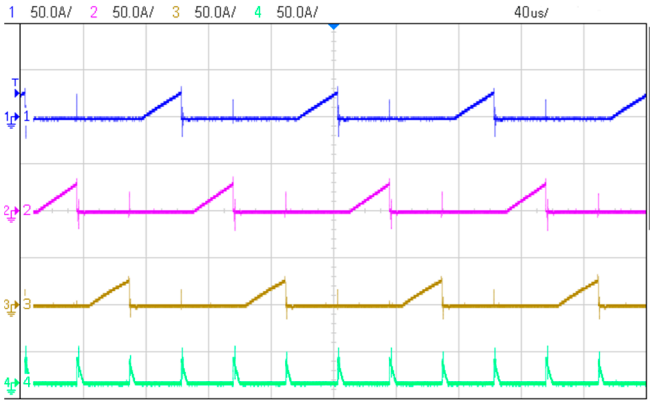


Figure 22. Experimental waveforms near sunset. Current: main switch 1 (yellow), main switch 2 (pink), and main switch 3 (yellow); scale 50 A/div. Output diode current (green); scale: 50 A/div. Base time Base time 40 µs/div.

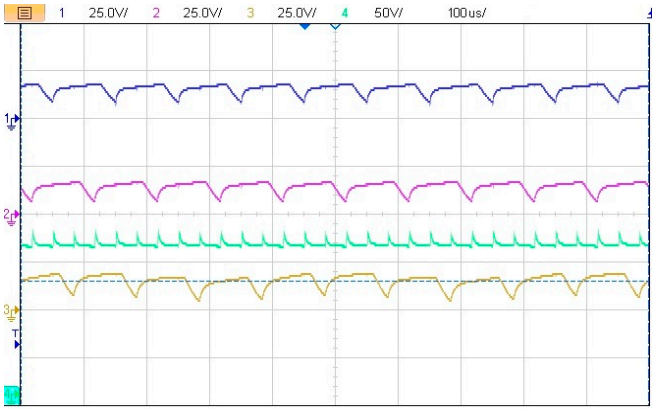


Figure 23. Experimental waveforms near sunset: Input voltages: PV panel 1 (blue), PV panel 2 (pink), and PV panel 3 (yellow); scale: 25 V/div. Converter output voltage (green); scale: 50 V/div. Base time 100 µs/div.

In Figure 23, the PV panels' voltages are shown as well as the converter's output voltage. It can be seen that the voltage of the panels, as well as the converter output voltage are reduced compared to Figure 17, as a result of the lower solar irradiance. The average voltages of the PVs were 16 V, and the output converter's average voltage was 165 V.

8. Converter Efficiency

The experimental measurement of the converter input and output voltages and currents (Figures 18 and 19) allowed us to calculate the efficiency of the proposed topology. For this calculation, the sum of the power generated by the three PV panels (Table 2) was determined to obtain the total input electrical power P_{in}. On the other hand, the output power P_{out} was measured in the load. Then, the converter efficiency was calculated as $\eta = 100 \cdot P_{out}/P_{in}$. The efficiency values of the converter were obtained at different times under different conditions of solar irradiance.

Figure 24 summarizes the results. It is clear that at noon, when the PV panels delivered a power close to their rated value, the highest efficiency was obtained ($\eta = 96.4\%$). Additionally, a theoretical analysis of the losses associated with each component of the proposed converter is presented in Appendix A.

Table 2. Measured power.

	Hour						
Power [W]	**8 am**	**10 am**	**12 pm**	**2 pm**	**4 pm**	**6 pm**	**7 pm**
PV panel 1	179.0	297.6	337.1	332.4	317.9	285.0	162.5
PV panel 2	175.0	307.5	332.4	329.3	319.0	281.9	165.6
PV panel 3	177.0	304.6	334.1	329.6	318.8	283.1	160.3
Converter output power	492.0	858.5	967.2	948.6	912.0	806.6	458.0

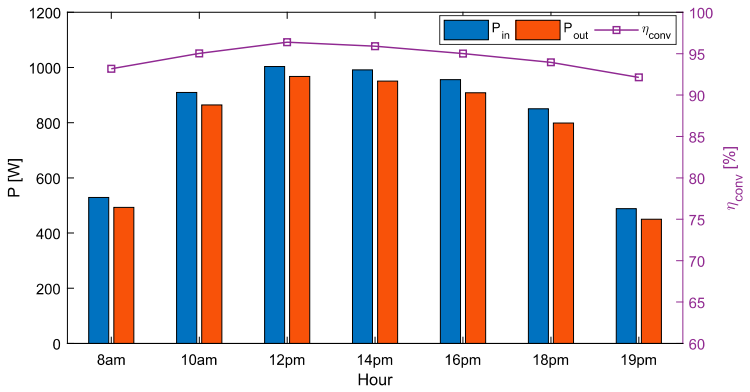


Figure 24. Experimental efficiency results.

9. Conclusions

A modified multi-winding DC–DC power converter topology has been proposed for photovoltaic applications. The operating states and mathematical expressions have been presented. The converter has advantages such as better magnetic use of the core compared to similar topologies, since it should process only a fraction of the converter's total power at a time. Moreover, it is built with only one secondary winding and one output diode, reducing the volume and number of power devices compared to classical interleaved topologies.

Simulations and experimental results showed the feasibility of the proposed topology, with all PV panels operating under an MPPT algorithm. Very good efficiency of the power converter topology was obtained for different solar irradiation conditions.

Author Contributions: Conceptualization, C.P., R.P. and J.R.; methodology, C.P., J.R., M.D. and H.Y.; software, C.P., H.Y. and I.A.; validation, C.P., J.R., M.D. and C.M.; formal analysis, C.P. and J.R.; investigation, C.P., C.M. and J.R.; resources, J.P., I.A., R.V., J.R. and R.P.; data curation, C.P., J.R. and I.A.; writing—original draft preparation, C.P., R.P. and J.R.; writing—review and editing, C.P., J.R., R.P., J.P.; visualization, I.A. and R.V.; supervision, C.P., J.P. and R.P.; project administration, C.P., R.V. and J.P.; funding acquisition, R.P. and J.P. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by ANID/PIA/ACT192013, ANID/FONDAP/15110019 and ANID/FONDECYT/1201616.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: The authors thank the financial support provided by Universidad de La Frontera—Chile and Pontificia Universidad Católica—Chile.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A. Converter Power Losses Analysis

In this appendix, a brief analysis of the power losses in the proposed converter is presented [31].

Main switches' power losses (P_{MS}): they include conduction losses and switching losses. Thus, power losses are defined by (A1) or (A2), where d is the duty cycle, t_r is rising time, and t_f is the falling time of the switch.

$$P_{MS} = 3\left(\int_0^{dT_s} v_{DS}(t)\cdot i_D(t)dt + \int_0^{t_r} v_{DS}(t)\cdot i_D(t)dt + \int_0^{t_f} v_{DS}(t)\cdot i_D(t)dt\right) \quad \text{(A1)}$$

$$P_{MS} = 3\left(\underbrace{\int_0^{dT_s} i_D(t)\cdot R_{ds_{on}}dt}_{Conduction\ losses} + \underbrace{\int_0^{t_r} i_D(t)\cdot R_{ds_{on}}dt + \int_0^{t_f} i_D(t)\cdot R_{ds_{on}}(t)dt}_{Switching\ losses}\right) \quad \text{(A2)}$$

Snubber-switches losses (P_{SS}): the power loss in the snubber switches is defined by:

$$P_{SS} = 3\left(\underbrace{\int_0^{dT_s} v_{DS}(t)\cdot i_D(t)dt}_{Conduction\ losses} + \underbrace{\int_0^{t_r} v_{DS}(t)\cdot i_D(t)dt + \int_0^{t_f} v_{DS}(t)\cdot i_D(t)dt}_{Switching\ losses}\right) \quad \text{(A3)}$$

Cables' losses (P_{Cu}): the power loss in the cables of the converter is defined by (A4), where $i_{C_{rms}}$ is the RMS current, and R_{cu} is the cables' resistance (skin effect include).

$$P_{Cu} = i^2_{C_{rms}}(t)\cdot R_{cu} \quad \text{(A4)}$$

Capacitors' losses (P_{Cs}): the power losses in capacitors are defined by the current waveform for each capacitor of the converter. In the converter, all capacitors are in polypropylene for low series-equivalent resistance. Thus, the capacitor losses are defined by (A5), where $i_{Cin_{rms}}$ is the RMS capacitor's current, and $R_{SE_{Cin}}$ is the series-equivalent resistance. The same equation is valid to calculate the losses in every converter capacitor considering the corresponding current and equivalent resistance.

$$P_{Cs} = 3\left(i^2_{Cin_{rms}}(t)\cdot R_{SE_{Cin}} + i^2_{Csnb_{rms}}(t)\cdot R_{SE_{Csnb}}\right) + i^2_{Co_{rms}}(t)\cdot R_{SE_{Co}} \quad \text{(A5)}$$

Flyback transformer's losses (P_{FT}): the power losses in the flyback transformer are defined by (A6), where $i_{prim_{rms}}$ and $i_{sec_{rms}}$ are the primary and secondary winding RMS current, respectively, $R_{eq_{prim}}$ and $R_{eq_{sec}}$ are the equivalent-resistor of the primary and secondary winding, respectively.

$$P_{FT} = 3\left(i^2_{prim_{rms}}(t)\cdot R_{eq_{prim}}\right) + i^2_{\mathrm{sec}_{rms}}\ (t)\cdot R_{eq_{sec}} \quad \text{(A6)}$$

Output diode's losses (P_{D_o}): the power losses in the output diode are defined for the conduction and non-conduction states. In Equation (A7), $v_d(t)$ and $i_d(t)$ are the diode's voltage and current, respectively.

$$P_{D_o} = 3\left(\int_0^{dT_s} v_d(t)\cdot i_d(t)dt + \int_0^{t_f} v_d(t)\cdot i_d(t)dt\right) \quad \text{(A7)}$$

Using the simulator, the power losses for each element were obtained, considering the converter operating at the rated power, and the results are shown in Table A1:

Table A1. Simulated power losses.

Power Losses	Value [W]
Main switches	13.10
Snubber switches	6.20
Cables	0.10
Capacitors	1.09
Flyback transformer	2.66
Output diode	7.60
Total losses	**30.75**

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