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Design and Control of a Battery Charger/Discharger Based on the Flyback Topology

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Featured Application: Interface low-voltage battery packs with medium-voltage or high-voltage DC buses, e.g., DC buses in microgrids or electric vehicles.

Abstract: Devices connected to microgrids require safe conditions during their connection, disconnection and operation. The required safety is achieved through the design and control of the converters that interface elements with the microgrid. Therefore, the design of both power and control stages of a battery charger/discharger based on a flyback is proposed in this paper. First, the structure of a battery charger/discharger is proposed, including the battery, the flyback, the DC bus, and the control scheme. Then, three models to represent the battery charger/discharger are developed in this work; a switched model, an averaged model, and a steady-state model, which are used to obtain the static and dynamic behavior of the system, and also to obtain the design equations. Based on those models, a sliding-mode controller is designed, which includes the adaptive calculation of one parameter. Subsequently, a procedure to select the flyback HFT, the output capacitor, and the K_v parameter based on operation requirements of the battery charger/discharger is presented in detail. Five tests developed in PSIM demonstrate the global stability of the system, the correct design of the circuit and controller parameters, the satisfactory regulation of the bus voltage, and the correct operation of the system for charge, discharge and stand-by conditions. Furthermore, a contrast with a classical PI structure confirms the performance of the proposed sliding-mode controller.

Keywords: adaptive control parameter; battery interface; circuital simulations; co-design; HFT; safety requirements

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1. Introduction

A DC microgrid can be defined as a power system formed by renewable energy sources (RESs), energy storage devices (ESDs), loads connected to a DC bus (see Figure 1), and a control system that manages the energy resources to supply the loads [1]. The RESs use the local resources to generate the power required by the loads. The power produced by some RESs can be imposed by the control system (e.g., fuel cells and hydro); while the power produced by other sources depends on the environmental conditions, like photovoltaic (PV) generators and wind turbines. Moreover, the loads vary over time since they depend on the specific application. Therefore, in a microgrid, it is common to have power unbalances between the RES and the loads.

Such power unbalances are compensated by regulating the DC bus voltage using one (or more) ESD and a charging/discharging system [1]. On the one hand, when the load exceeds the generation, the DC bus voltage tends to decrease; then, the ESD is discharged to balance generation and load, as consequence, the DC bus voltage increases and returns to its reference value. On the other hand, the DC bus voltage tends to increase when the generation exceeds the load; in that case, the ESD is charged to guarantee the power

balance and return the DC bus voltage to its nominal value. Finally, when generation and load are equal, the ESD does not supply or absorb power (stand-by). Moreover, it is worth noting that the DC bus voltage regulation is important in a microgrid to provide safe operating conditions for the loads since most of the RESs work as current sources assuming a regulated DC bus voltage.

Figure 1. General structure of a DC microgrid.

An ESD charging/discharging system is typically formed by a storage device, a bidirectional power converter, and a control system. The DC bus voltage (v_{dc}) is usually greater than the battery voltage (v_b); hence, bidirectional step-up converters like Boost [2–4] or Buck-Boost [5,6] are commonly used. Considering that these converters have limited voltage gains, a typical value of v_b is 12 V [7–9], and the values of v_{dc} in microgrid applications vary in wide range, but are significantly greater than v_b (e.g., 48 V [10–12], 200 V [13]), or higher [14]; then, multiple batteries are connected in series and parallel to reach the required voltage and storage capacity levels, respectively. Those batteries have different electrical characteristics due to manufacturing imperfections, uniform aging, and continuous charging/discharging cycles; these differences produce excessive heat and accelerated degradation of the batteries [15]. That is why there is a necessity for battery balancing systems [15,16] or charging/discharging systems implemented with high-gain power converters to connect each battery, or arrays of parallel batteries, directly to the DC bus. Such a charging/discharging system would avoid the necessity of a balancing system providing some advantages like a high ESDs modularity, and the connection of batteries with several technologies and electrical characteristics. Moreover, this charging/discharging system would permit a simple connection and disconnection of batteries to adjust the storage capacity and the use of second-life batteries coming from applications like electric vehicles.

A bidirectional flyback converter is a feasible option to implement such an ESD charging/discharging system since it provides galvanic isolation between the ESD and the DC bus, it has a simple structure, and it can provide high voltage gains. One disadvantage of the flyback converter is its discontinuous input current, which produces significant ripples in the battery current reducing its life cycle [17,18]. This disadvantage is shared by other charging/discharging systems based on Buck, Buck-Boost, or Zeta converters and has been mitigated by connecting a capacitor in parallel to the battery. Such a capacitor does not affect the dynamic response of the charging/discharging system and absorbs the high frequency components of the battery current [19,20].

A state-of-the-art in this topic shows that the flyback converter has been used to implement battery charging systems for generic applications [21,22], electric vehicles [23–26], phones [27], PV systems [28,29], and microgrids [6]. Additionally, the flyback converter has also been used for other applications involving batteries like power supply of DC motors [19,30], LED drivers [20], and rectifiers [31]. Nevertheless, the authors have not found

up to now any ESD charging/discharging system with a flyback converter to regulate the voltage in a DC bus.

The design of the flyback converter and the control strategy is necessary to obtain the desired performance of the charging/discharging system. In the literature, it is possible to find different design procedures and equations to determine the flyback magnetizing inductance (L_m), output capacitance (C_{dc}), and transformer's turns ratio (n) for battery charging or discharging systems. In [21,30,32], the authors introduce procedures and equations to determine L_m and n , as well as other elements for the snubber circuit [21] and additional characteristics of the high-frequency transformer (HFT) [32]. An interesting aspect of the procedure presented in [21] is that it includes the calculation of three parameters required by the proposed controller (peak current mode controller with exponential compensation ramp). However, those procedures do not include the design of C_{dc} [21,30,32] and the controllers do not regulate the DC bus voltage [21], are not clearly explained [30], or are not included [32].

Other papers provide equations to size the elements of flyback converters used in battery charging applications. In [25,31], the authors provide equations to determine L_m , n , and C_{dc} for step-down flyback converters for a rectifier [31] and an electric vehicle charger. While in [27,28] the authors provide additional equations to determine more characteristics of the snubber circuit elements [27] and the HFT [28] for a phone battery charger [27] and a PV-based uninterruptible power supply [28]. Moreover, other papers are focused on the design of the flyback HFT for a LED illumination system [20] or on providing equations to calculate just L_m [24,33] or L_m and C_{dc} [19,26] for flyback-based battery charging applications.

Regarding the controllers proposed in the literature for battery charging systems that use flyback converters, most of the papers use linear controllers, while others use specialized controllers (like peak current control [21,34] or fuzzy controller [23]) or do not include a control structure [22,29,31–33,35]. A cascade controller is used in [24–26], where the outer loop is a PI controller to regulate v_b , and the inner loop is a PI that tracks a reference of the battery current (i_b). In [24], both PIs are tuned by using frequency response to guarantee a desired phase margin and crossover frequency; while the other two papers do not include a design procedure for the PIs [26] or do not provide clear information of the controller structure [25]. Some authors use one PI [6,20,27] or one two-poles two-zeros compensator [19,30] to regulate the flyback output voltage. On the one hand, the PI controller proposed in [27] is tuned by trial and error using different values of the proportional and integral gains; whereas the PIs introduced in [6,20] do not include a design procedure. On the other hand, the compensators introduced in [19,30] use frequency response to tune the controller parameters; nonetheless [30], they do not provide details about the controller design criteria.

From the literature review, the authors identified that there is not a flyback-based battery charging/discharging system to regulate the voltage of a DC bus. However, it is possible to find different battery charging or discharging systems for different applications that illustrate the feasibility of using flyback converters as a power interface for batteries. Moreover, some flyback-based battery interfaces propose design procedures of the main converter components like L_m , C_{dc} , and n . Nevertheless, those procedures consider a single operating point of the converter, a single operating mode (i.e., charging or discharging), and do not consider the effect of the flyback parameters on the closed-loop system stability. As consequence, the design of the controller and flyback converter are two independent procedures, which may restrict the stability regions of the system. Additionally, linear converters are the most widely used approach for flyback-based charging or discharging systems. These controllers are designed using linearized models on a particular operating point; therefore, they cannot guarantee the system stability for any operating condition and mode (i.e., charging, discharging, and stand-by).

This paper proposes a flyback-based DC bus voltage regulation system and a co-design procedure of the flyback converter and its control system, where the last is implemented

with an adaptive Sliding-Mode Controller (SMC). This paper has three main contributions: (1) a DC bus voltage regulation system that provides high voltage gain and galvanic isolation, which allows the direct connection of a battery to a DC bus and the protection of the battery from faults in the DC bus; (2) an adaptive SMC that guarantees the system stability in any operating condition and mode (i.e., charging, discharging, or stand-by); (3) a detailed co-design procedure of the flyback parameters (L_m , C_{dc} , and n) and the SMC parameters considering the system stability.

The paper begins with the modeling of the proposed charging/discharging system (Section 2) followed by the stability analysis of the proposed Sliding-Mode Controller (SMC) (Section 3), which considers the voltage at C_{dc} , the current through L_m , the DC bus current, and two constants (K_v and K_i). Then, the paper introduces the implementation of the proposed SMC along with the analysis of the maximum switching frequency and the dynamic calculation of K_i (Section 4). Later, the paper presents the co-design procedure to determine the HFT parameters (L_m and n), C_{dc} , and K_v , to guarantee the system stability (Section 5). Finally, simulation results validate the proposed procedure and illustrate the dynamic and static performance of the proposed charging/discharging system under different operating conditions (Section 6) and the conclusions close the paper (Section 7).

2. Proposed Charger/Discharger

The proposed charger/discharger circuit is based on a bidirectional flyback converter; thus, the classical output diode must be replaced by a second Mosfet. Figure 2 presents the proposed circuit, where Mosfet M_2 replaces the output diode of the unidirectional Flyback converter, while Mosfet M_1 is in the same position for both unidirectional and bidirectional topologies.

Figure 2. Proposed circuit for the charger/discharger based on the flyback topology.

The flyback converter includes a HFT, which provides galvanic isolation and a high voltage conversion ratio. In the circuit of Figure 2, the HFT is highlighted in green color, and it is modeled accounting for both the magnetizing L_m and leakage L_k inductances [35,36]. The magnetizing inductance is modeled at the primary side, which allows analyzing the effect of the primary control signal u on the circuit. Instead, the leakage inductance is modeled at the secondary side, which enables the analysis of the dynamic behavior of the DC bus voltage v_{dc} . The HFT is modeled, without loss of generality, with a turn ratio $1 : n$, but any other relation can be adopted.

In this bidirectional circuit, the primary control signal u activates/deactivates the Mosfet M_1 at the primary side of the HFT, while the complementary control signal $\bar{u} = 1 - u$ activates/deactivates the Mosfet M_2 at the secondary side of the HFT. The circuital model of the battery charger, depicted in Figure 2, models the interaction between sources and loads connected to the DC bus as a single bus current i_{dc} , which is the result of subtracting

the sources and loads currents, i.e., $i_{dc} = (i_{i1} + i_{i2} + \dots + i_{in}) - (i_{o1} + i_{o2} + \dots + i_{om})$ using the nomenclature of Figure 1. In addition, the DC bus capacitance is modeled with the C_{dc} capacitor, which collects the output capacitances of the sources and the input capacitances of the loads connected to the bus.

The charger/discharger proposed in Figure 2 also includes a control system aimed at regulating the bus voltage v_{dc} , which is needed to provide a safe operating condition to both sources and loads. Such a control system is designed using the sliding-mode control (SMC) theory, and its analysis and stability are studied in the following section. The outputs of the SMC are the converter control signals u and $\bar{u}$, thus no PWM is required. Figure 2 also describes the measurements needed by the SMC: current of both the primary i_p and secondary i_s sides of the HFT, battery voltage v_b , DC bus voltage v_{dc} , and current i_{dc} . Since both battery and DC bus are isolated by the HFT, a single ground reference is not present, instead the battery and DC bus voltages are measured using differential voltage sensors S_{vb} and S_{vdc} , respectively. From the circuit it is also noted that the battery current is equal to the current at the primary side of the HFT, thus $i_b = i_p$. Finally, the SMC receives the reference value v_r of the DC bus voltage.

2.1. Switched Model

The mathematical model of the charger/discharger is obtained by studying the differential equations governing the converter for the two possible conditions of the control signal u , which are reported as follows:

- When $u = 1$ ($\bar{u} = 0$) Mosfet M_1 is ON and Mosfet M_2 is OFF, which imposes the following differential equations on the magnetizing inductance current i_{Lm} and bus voltage v_{dc} :

$$\frac{d i_m}{dt} = \frac{v_b}{L_m} \quad (1)$$

$$\frac{d v_{dc}}{dt} = -\frac{i_{dc}}{C_{dc}} \quad (2)$$

- When $u = 0$ ($\bar{u} = 1$) Mosfet M_1 is OFF and Mosfet M_2 is ON. For this analysis the effect of both the leakage L_k inductance and bus voltage is calculated at the primary side of the HFT, while the effect of the magnetizing inductance is calculated at the secondary side of the HFT:

$$\frac{d i_m}{dt} = -\frac{v_{dc}/n}{L_m + L_k/n^2} \quad (3)$$

$$\frac{d v_{dc}}{dt} = \frac{(i_m/n) - i_{dc}}{C_{dc}} \quad (4)$$

Combining the previous differential equations leads to the following switched model:

$$\frac{d i_m}{dt} = \frac{v_b \cdot u}{L_m} - \frac{v_{dc} \cdot (1 - u)}{n \cdot L_q} \quad (5)$$

$$L_q = L_m + \frac{L_k}{n^2} \quad (6)$$

$$\frac{d v_{dc}}{dt} = \frac{1}{C_{dc}} \cdot \left[\frac{i_m \cdot (1 - u)}{n} - i_{dc} \right] \quad (7)$$

Moreover, the leakage inductor current i_k , and the currents i_p and i_s presented in Figure 2, are:

$$i_k = i_s = \frac{i_m}{n} \cdot (1 - u) \quad (8)$$

$$i_p = i_m \cdot u \quad (9)$$

2.2. Averaged Model

The averaged model is obtained by averaging the previous equations within the switching period T_{sw} . Such a procedure is performed by replacing the binary control signal u by its averaged value, which corresponds to the converter duty cycle:

$$d = \frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} u \cdot dt \quad (10)$$

Then, the averaged model of the charger/discharger is the following one:

$$\frac{d i_m}{dt} = \frac{v_b \cdot d}{L_m} - \frac{v_{dc} \cdot (1-d)}{n \cdot L_q} \quad (11)$$

$$\frac{d v_{dc}}{dt} = \frac{1}{C_{dc}} \cdot \left[\frac{i_m \cdot (1-d)}{n} - i_{dc} \right] \quad (12)$$

Moreover, the averaged leakage inductor current i_k and i_p current are:

$$i_k = i_s = \frac{i_m}{n} \cdot (1-d) \quad (13)$$

$$i_p = i_m \cdot d \quad (14)$$

2.3. Steady-State Model

The steady-state relations between the previous physical variables are obtained by considering the averaged differential equations equal to zero, which leads to:

$$i_m = \frac{n}{1-d} \cdot i_{dc} \quad (15)$$

$$d = \frac{M}{M + n \cdot L_q / L_m} \quad , \quad M = \frac{v_{dc}}{v_b} \quad (16)$$

Other important expressions needed for the converter design are the voltage and current ripple magnitudes. In this work, the design will be focused on the current ripple at the magnetizing inductance and the voltage ripple at the bus voltage, since the first one affects the transformer rating and the second one is defined by the requirements of the devices connected to the bus. The ripple at the magnetizing inductance is calculated from (1), which forces the increment of i_m during $d \cdot T_{sw}$ seconds (when $u = 1$); thus, the current ripple in i_m , around the steady-state value given in (15), is given in (17). In such an expression, $F_{sw} = 1/T_{sw}$ is the switching frequency.

$$\delta i_m = \frac{v_b \cdot d}{2 \cdot L_m \cdot F_{sw}} \quad (17)$$

Similarly, the voltage ripple in v_{dc} , around the steady-state value defined by (16), is calculated from (2) as given in (18).

$$\delta v_{dc} = \frac{i_{dc} \cdot d}{2 \cdot C_{dc} \cdot F_{sw}} \quad (18)$$

3. Sliding-Mode Controller Design

The correct operation of the charger/discharger requires a suitable controller to ensure both global stability and the desired speed correcting the voltage deviations caused by perturbations in the bus current. Therefore, this work proposes an SMC, where the switching function is designed based on the following conditions:

- The error between the bus voltage v_{dc} and the desired value (reference) v_r must be corrected, thus the term $[K_v \cdot (v_{dc} - v_r)]$ is introduced, where K_v is a parameter.

- The perturbations introduced in the bus current i_{dc} could be quickly compensated by the magnetizing inductor current i_m , thus the term $[K_i \cdot i_m - i_{dc}]$ is introduced, where K_i is a parameter.

Based on the previous considerations, the following switching function Ψ and sliding-surface Φ are defined:

$$\Psi = K_v \cdot (v_{dc} - v_r) + K_i \cdot i_m - i_{dc} \quad (19)$$

$$\Phi = \{\Psi = 0\} \quad (20)$$

A stable SMC ensures the system operates within the sliding surface [37,38]. Therefore, if the proposed SMC is stable, it will ensure the charger/discharger operation within the sliding surface (20), thus $v_{dc} = v_r$ and $K_i \cdot i_m = i_{dc}$. Since the bus current i_{dc} changes depending on the operation condition, the parameter K_i must be dynamically adapted; hence, the proposed controller is an adaptive SMC. The adaptive value of K_i is discussed afterward.

The stability of an SMC is evaluated using three tests [37,38]: transversality, reachability, and equivalent control. Those proofs are performed in the following subsections.

3.1. Transversality Condition

The transversality condition proves the presence of the control signal u into the derivative of the switching function Ψ ; therefore, this condition evaluates the capability of the SMC to modify the system behavior. The mathematical formalization of this procedure is given in (21).

$$\frac{d}{du} \left(\frac{d\Psi}{dt} \right) \neq 0 \quad (21)$$

This analysis is based on the switching function derivative, which is calculated as given in (22).

$$\frac{d\Psi}{dt} = \frac{K_v}{C_{dc}} \cdot \left[\frac{i_m \cdot (1-u)}{n} - i_{dc} \right] + K_i \cdot \left[\frac{v_b \cdot u}{L_m} - \frac{v_{dc} \cdot (1-u)}{n \cdot L_q} \right] - \frac{di_{dc}}{dt} \quad (22)$$

Then, replacing Equations (22), (15), and (16) into (21) leads to the expression given in (23).

$$\frac{d}{du} \left(\frac{d\Psi}{dt} \right) = -\frac{K_v \cdot i_{dc}}{C_{dc} \cdot n} \cdot \left(M \cdot \frac{L_m}{L_q} + n \right) + K_i \cdot \left(\frac{v_b}{L_m} + \frac{v_{dc}}{n \cdot L_q} \right) \quad (23)$$

The following subsection will explain that the sign of the transversality value defines the reachability conditions, thus the sign of (23) must be the same for any operating condition. The values of K_v , C_{dc} , n , M , L_m , L_q , v_b , and v_{dc} are positive; the values of K_v and K_i are also positive as will be demonstrated in Section 3.4, but the bus current i_{dc} could be positive, negative, or zero. Evaluating expression (23) for $i_{dc} = 0$ leads to a positive value; hence, the proposed SMC must have positive transversality. Therefore, expression (23) must be positive, which leads to the following design equation for the SMC parameters:

$$-\frac{K_v \cdot i_{dc}}{C_{dc} \cdot n} \cdot \left(M \cdot \frac{L_m}{L_q} + n \right) + K_i \cdot \left(\frac{v_b}{L_m} + \frac{v_{dc}}{n \cdot L_q} \right) > 0 \quad (24)$$

In conclusion, the SMC fulfills the transversality condition when expression (24) is satisfied, thus such an expression must be considered in the calculation of the parameters.

3.2. Reachability Conditions

The reachability conditions evaluate the ability of the SMC to reach the desired surface starting from any operating condition. The concepts of the reachability analysis are:

- If the system is operating under the surface ($\Psi < 0$), the switching function derivative must be positive ($\frac{d\Psi}{dt} > 0$) to ensure that the system is able to reach the surface ($\Psi = 0$). This first concept is formalized as follows:

$$\lim_{\Psi \rightarrow 0^-} \frac{d\Psi}{dt} > 0 \quad (25)$$

- If the system is operating above the surface ($\Psi > 0$), the switching function derivative must be negative ($\frac{d\Psi}{dt} < 0$) to ensure that the system is able to reach the surface ($\Psi = 0$). This second concept is formalized as follows:

$$\lim_{\Psi \rightarrow 0^+} \frac{d\Psi}{dt} < 0 \quad (26)$$

However, the sign of the transversality condition defines the behavior of the switching function derivative, thus it is necessary to define the effective reachability conditions:

- A positive transversality sign implies that positive changes on u (from 0 to 1) impose a positive switching function derivative. The formal description of this condition is $\frac{d}{du} \left(\frac{d\Psi}{dt} \right) > 0 \Rightarrow \frac{d\Psi}{dt} > 0$ when $u = 1$.
- A negative transversality sign implies that negative changes on u (from 1 to 0) impose a positive switching function derivative. The formal description of this condition is $\frac{d}{du} \left(\frac{d\Psi}{dt} \right) < 0 \Rightarrow \frac{d\Psi}{dt} > 0$ when $u = 0$.

Taking into account that the design condition defined in (24) imposes positive transversality, the general reachability conditions (25) and (26) are rewritten as the effective conditions (27) and (28), respectively.

$$\lim_{\Psi \rightarrow 0^-} \frac{d\Psi}{dt} \Big|_{u=1} > 0 \quad (27)$$

$$\lim_{\Psi \rightarrow 0^+} \frac{d\Psi}{dt} \Big|_{u=0} < 0 \quad (28)$$

The previous reachability conditions are analyzed by replacing the switching function derivative (22) into inequalities (27) and (28), obtaining the design expressions given in (29) and (30), respectively, where expressions (15) and (16) have also been used.

$$-\frac{K_v \cdot i_{dc}}{C_{dc} \cdot n} + \frac{K_i \cdot v_b}{L_m} > \frac{di_{dc}}{dt} \quad (29)$$

$$\frac{v_{dc}}{n \cdot L_q} \cdot \left(\frac{K_v \cdot i_{dc} \cdot L_m}{C_{dc} \cdot v_b} - K_i \right) < \frac{di_{dc}}{dt} \quad (30)$$

In conclusion, the SMC fulfills the reachability conditions when expressions (29) and (30) are satisfied, thus those expressions must be considered in the calculation of the parameters.

3.3. Equivalent Control Condition

The equivalent control condition evaluates that the average value of the control signal u is always constrained within the control signal limits $[0, 1]$. Taking into account that the average value of u is the converter duty cycle d , as given in (10), the equivalent control condition, in practice, evaluates the non-saturation of the duty cycle:

$$0 < u_{eq} = d < 1 \quad (31)$$

The equivalent control is calculated within the surface and with a trajectory parallel to the surface ($\Psi = 0$ and $\frac{d\Psi}{dt} = 0$) [37,38], replacing u by its averaged value d . Hence, solving switching function derivative (22) equal to zero, for $u_{eq} = d$, results as follows:

$$u_{eq} = d = \frac{\frac{di_{dc}}{dt} - \frac{K_v \cdot i_m}{C_{dc} \cdot n} + \frac{K_v \cdot i_{dc}}{C_{dc}} + \frac{K_i \cdot v_{dc}}{n \cdot L_q}}{-\frac{K_v \cdot i_m}{C_{dc} \cdot n} + \frac{K_i \cdot v_b}{L_m} + \frac{K_i \cdot v_{dc}}{n \cdot L_q}} \quad (32)$$

Replacing the u_{eq} value (32) into inequality (31) leads to the same expressions (29) and (30) obtained from the reachability analysis. Therefore, fulfilling the reachability conditions also ensures that the SMC fulfills the equivalent control condition; hence, the duty cycle will not be saturated.

Finally, the SMC will provide global stability when the system parameters fulfill the restrictions imposed in (24), (29), and (30).

3.4. Closed-Loop Dynamics

Taking into account that the SMC parameters fulfill the restrictions (24), (29) and (30), the SMC ensures $\Psi = 0$, thus $K_v \cdot (v_{dc} - v_r) + K_i \cdot i_m - i_{dc} = 0$. Since the main perturbation sources are the changes on the bus current, i_m or K_i must be adjusted to compensate the changes on i_{dc} : the relation between i_m and i_{dc} , given (15), shows that $i_{dc} = \frac{1-d}{n} \cdot i_m$, thus K_i must be defined as given in (33) to ensure the compensation of i_{dc} .

$$K_i = \frac{1-d}{n} > 0 \quad (33)$$

Moreover, since the SMC is in charge of driving the Mosfets states, the closed-loop dynamics of the bus voltage must be described using the averaged model. In addition, the correct operation of the SMC ($\Psi = 0$) with the K_i value defined in (33) imposes $K_i \cdot i_m - i_{dc} = -K_v \cdot (v_{dc} - v_r)$, which is replaced into the averaged model (12) to obtain the closed-loop dynamics of the bus voltage under the action of the SMC:

$$\frac{d v_{dc}}{dt} = \frac{1}{C_{dc}} \cdot [-K_v \cdot (v_{dc} - v_r)] \quad (34)$$

The previous equation is an equivalent linear expression, which can be analyzed using the Laplace transformation as follows:

$$\frac{V_{dc}(s)}{V_r(s)} = \frac{1}{\frac{C_{dc}}{K_v} \cdot s + 1} \quad (35)$$

The equivalent dynamics of the DC bus voltage, reported in (35), exhibits a first-order behavior with an equivalent time constant $\tau = \frac{C_{dc}}{K_v}$; hence, the settling-time t_s of the bus voltage is calculated as $t_s = 4 \cdot \tau$ [39], which leads to the design equation for the parameter K_v of the SMC:

$$K_v = \frac{4 \cdot C_{dc}}{t_s} > 0 \quad (36)$$

In conclusion, the design of K_i , as given in (33), ensures the compensation of the perturbations on i_{dc} ; and the design of K_v , as given in (36), ensures a settling time equal to t_s in the bus voltage.

4. Implementation of the Sliding-Mode Controller

The implementation of sliding-mode controllers for power converters is usually performed using comparators with hysteresis to limit the switching frequency [40]. Therefore, the practical sliding surface is defined as given in (37), where H is the hysteresis amplitude,

i.e., the hysteresis band is $[-\delta\Psi, +\delta\Psi]$. It must be put into evidence that the switching function Ψ is the same one defined in (19), the change occurs at the comparison limits (from 0 to $\pm\delta\Psi$).

$$\Phi_H = \{\Psi \leq \delta\Psi\} \quad (37)$$

Based on the reachability conditions reported in (27) and (28), the control law required to reach the hysteresis band is obtained as follows:

- If $\Psi > +\delta\Psi$, it is required $\frac{d\Psi}{dt} < 0$ to reach $[-\delta\Psi, +\delta\Psi]$ (the hysteresis band), which is achieved with $u = 0$.
- If $\Psi < -\delta\Psi$, it is required $\frac{d\Psi}{dt} > 0$ to reach $[-\delta\Psi, +\delta\Psi]$, which is achieved with $u = 1$.

The previous control law is formalized with the logic equation given in (38), which generates the main control signal u , and requires the calculation of the switching function Ψ . The following subsection describes, in detail, the synthesis of this control law.

$$u = \begin{cases} 1 & \text{if } \Psi < -\delta\Psi \\ 0 & \text{if } \Psi > +\delta\Psi \end{cases} \quad (38)$$

4.1. Synthesis of the Control Law

The first step for the synthesis of the control law is the calculation of the switching function, which has two main terms: $K_v \cdot (v_{dc} - v_r)$ and $K_i \cdot i_m - i_{dc}$. The first term is simple to calculate since K_v is the constant given in (36), v_{dc} is measured using a voltage sensor, and v_r is defined as an input of the SMC. The calculation of this first term is illustrated in Figure 3 by using a subtractor and a gain for K_v .

Figure 3. Proposed sliding-mode controller for the battery charger/discharger.

The second term, instead, requires the dynamic calculation of K_i , and i_m is not physically measured in the circuit. The calculation of K_i , reported in (33), requires calculating the duty cycle as given in (16), which is done by measuring both v_{dc} and v_b to perform the required mathematical operation with the constants n and L_q/L_m . Then, $1-d$ is calculated, which is divided by n . The dynamic calculation of K_i is defined in (39) and illustrated in Figure 3 (green block) using gains, an adder, and a divider.

$$K_i = \frac{v_b}{v_{dc} \cdot L_m/L_q + v_b \cdot n} \quad (39)$$

The second term requires the value of i_m , which is not measured directly. However, from the switched expressions for i_p and i_s , given in (8) and (9), it is possible to reconstruct i_m from the measurement of i_p and i_s as follows:

$$i_m = \begin{cases} i_p & \text{if } u = 1 \\ i_s \cdot n & \text{if } u = 0 \end{cases} \quad (40)$$

The previous i_m reconstruction enables the calculation of the switching function (19) from i_p and i_s , which is used to modify the control law given in (38) as follows:

$$u = \begin{cases} 1 & \text{if } \Psi_s < -\delta\Psi \quad \text{where } \Psi_s = K_v \cdot (v_{dc} - v_r) + K_i \cdot n \cdot i_s - i_{dc} \\ 0 & \text{if } \Psi_p > +\delta\Psi \quad \text{where } \Psi_p = K_v \cdot (v_{dc} - v_r) + K_i \cdot i_p - i_{dc} \end{cases} \quad (41)$$

Finally, such a practical control law is implemented using multipliers, adders, subtractors, comparators, and an S-R Flip-Flop. The Flip-Flop is used to keep the value of u inside the hysteresis band, where $u = 1$ is imposed by activating the set (S) signal, while $u = 0$ is imposed by activating the reset (R) signal. Moreover, the Flip-Flop also produces the complementary control signal $\bar{u}$ without the need for additional hardware. Finally, the complete synthesis of the practical control law is illustrated in Figure 3 (red block), which corresponds to an adaptive sliding-mode controller due to the dynamic calculation of the parameter K_i . In such a figure, the blue signals correspond to physical measurements, while the red signals are the outputs of the SMC.

4.2. Switching Frequency

The switching frequency of the dc/dc converter must be constrained to the limit imposed by the Mosfets; otherwise, the SMC will not be able to properly regulate the charger/discharger.

The switching frequency F_{sw} is the result of the Mosfet activation/deactivation at the limits of the hysteresis band, thus the ripple in the switching function $\delta\Psi$ must be calculated. The correct operation of the SMC guarantee that $v_{dc} = v_r$ (bus voltage regulation) and $\frac{1-d}{n} \cdot i_m = i_{dc}$ (current balance at the output capacitor); hence, from the switching function definition (19) it is obtained the following ripple equation:

$$\Psi_{ripple} = K_v \cdot \delta v_{dc} + \frac{1-d}{n} \cdot \delta i_m \quad (42)$$

The charger/discharger must be designed to provide low-harmonic distortion to the DC bus; therefore, δv_{dc} must be small, but δi_m depends on the transformer parameters. In addition, Equations (1) and (2) show that the derivatives of v_{dc} and i_m have opposite signs, as consequence, the most negative value of δv_{dc} occurs when δi_m has the most positive value. Therefore, the maximum value of Equation (42) is achieved when $\delta v_{dc} \approx 0$, which is used to obtain the maximum switching frequency of the charger/discharger:

$$\lim_{\delta v_{dc} \rightarrow 0^+} \Psi_{ripple} = \delta\Psi = \frac{1-d}{n} \cdot \delta i_m \quad (43)$$

Replacing Equations (15) and (17) into (43) leads to an expression for the maximum switching frequency of the charger/discharger:

$$F_{sw,max} = \frac{v_b \cdot M \cdot L_q}{2 \cdot \delta\Psi (L_m \cdot M + n \cdot L_q)^2} \quad (44)$$

Finally, the parameter $\delta\Psi$ of the SMC, which corresponds to the peak value of the hysteresis band, must be calculated from (44) to ensure a maximum switching frequency in agreement with Mosfets limitations.

4.3. Bus Capacitance and Voltage Perturbation

The term switching function of the SMC is designed to compensate for the perturbation at the bus current; however, an instantaneous change on the bus current will produce a voltage perturbation on the DC bus. This phenomenon is unavoidable since the capacitor current is the result of the instantaneous change on the bus current and the leakage current, which has a non-instantaneous change defined by (8). Therefore, after a perturbation in the bus current, the capacitor current is not zero, which produces a bus voltage perturbation.

This phenomenon is illustrated in Figure 4, where a step-like change in the bus current i_{dc} is considered. In this example, the bus current changes from the maximum discharge value $i_{dc(0)} > 0$ to the maximum charge value $i_{dc(f)} < 0$ with almost an almost infinite derivative $\frac{di_{dc}}{dt} \rightarrow -\infty$, which produces the following behavior:

- A stable bus voltage requires to fulfill the charge balance principle; thus, the average capacitor current must be zero, i.e., $i_{Cdc} = i_k - i_{dc} = 0$.
- The leakage current i_k was originally defined to have an average value equal to the DC current previous to the perturbation $i_{dc(0)}$.
- The step-change on the DC current to the new value $i_{dc(f)}$ produces an instantaneous change on the capacitor current equal to $i_{dc(0)} - i_{dc(f)}$.
- The SMC must reduce i_k to have an average value equal to the new DC current $i_{dc(f)}$, thus the control signal must be set to $u = 0$.
- The leakage current changes with a limited derivative defined by (5) and (8), thus i_k takes a time T_d to reach $i_{Cdc} = i_k - i_{dc} = 0$.
- During T_d , the i_{Cdc} current is positive because $i_k > i_{dc}$; hence, a positive charge is introduced into the capacitor, which increases the bus voltage.
- This process produces an undesired deviation Δv_{dc} into the bus voltage, which must be limited to avoid damages on both the loads and sources connected to the bus.

Therefore, this paper proposes to develop a design equation for C_{dc} based on the maximum Δv_{dc} value acceptable for a safe operation of the devices connected to the bus.

The first step is to calculate the maximum change on the capacitor current, which occurs when the dc current changes at the peak of the leakage current, i.e., $\max(i_k)$. From Equation (8), it is noted that $i_k = \frac{i_m}{n}$ for $u = 0$. Replacing the previous values into $\max(i_k)$, and adding the ripple δi_m given in (17) to calculate the peak value of i_m , it is possible to obtain (45):

$$\max(i_k) = \max\left(\frac{i_m}{n}\right) = \frac{i_m + \delta i_m}{n} \quad (45)$$

The net change on $i_{Cdc} = i_k - i_{dc}$ that causes the voltage deviation, as observed in Figure 4, is:

$$\Delta i_k = \max(i_k) - i_{dc(f)} \quad (46)$$

Since the leakage current takes T_d seconds to reach the $i_{Cdc} = 0$ [A] condition, i.e., $i_k = i_{dc(f)}$, the charge Q_{Cdc} introduced into the bus capacitor C_{dc} during this perturbation is:

$$Q_{Cdc} = \int_0^{T_d} i_k - i_{dc(f)} dt = \frac{1}{2} \cdot T_d \cdot \Delta i_k \quad (47)$$

T_d is calculated from the condition $i_k = i_{dc(f)}$, considering the relation $i_k = \frac{i_m}{n}$ for $u = 0$ given in (8), and using the derivative of i_m for $u = 0$ given in (3) to calculate the derivative of i_k :

$$T_d = \frac{\max(i_k) - i_{dc}(f)}{\frac{v_{dc}}{n^2 \cdot L_q}} \quad (48)$$

Now, taking into account that the charge (47) introduced in C_{dc} produces the voltage deviation $\Delta v_{dc} = \frac{Q_{Cdc}}{C_{dc}}$, and using the previous expressions for T_d given in (48), Q_{Cdc} given in (47), Δi_k given in (46), $\max(i_k)$ given in (45), and δi_m given in (17), the voltage deviation caused by a step-like DC current perturbation is:

$$\Delta v_{dc} = \frac{n^2 \cdot L_q}{2 \cdot v_{dc} \cdot C_{dc}} \cdot \left[\frac{i_{dc(0)}}{1-d} + \frac{v_b}{2 \cdot F_{sw} \cdot n \cdot L_m} - i_{dc(f)} \right]^2 \quad (49)$$

Finally, the capacitance C_{dc} of the DC bus must be calculated from (49) to ensure a maximum Δv_{dc} value that guarantees a safe operation of the devices connected to the bus. Since the bus capacitor collects the output capacitances of the sources and the input capacitances of the loads connected to the bus, C_{dc} could be increased to the desired value by adding an external capacitor. However, if the required C_{dc} is lower than the collected capacitance of sources and loads, the voltage deviation will be lower than the maximum safe value and a correct operation is achieved.

Figure 4. Example of a bus voltage deviation due to fast current perturbations.

5. Design Procedure and Application Example

This section provides a summary of the design procedure for both the charger/discharger circuit and SMC parameters. Moreover, the design procedure is illustrated using an application example based on realistic conditions.

The first step of the design process is to define the design requirements. Table 1 reports the requirements adopted for illustrating the design process, where a standard 12 [V] volt battery must be connected to a 48 [V] bus, which is used in DC microgrids [10–12]. The battery charger/discharger must be designed to provide or absorb a maximum of 1 [A], with a maximum slew-rate (current derivative) of 50 [A/ms], which could completely charge (SOC = 100%) a EnerSys NP0.8-12-ND [41] lead-acid battery (12 V–0.8 Ah) in 48 min, or charge/discharge the 10% of the SOC in 4.8 min.

The sources and loads require a maximum voltage ripple of 0.5 [%] for a correct operation, and those devices could be damaged for voltage perturbations higher than 3.5 [%], which could be triggered by the highest current perturbation possible, i.e., a step from the maximum current (1 [A]) to the minimum current (−1 [A]) or vice versa, thus ± 2 [A]; moreover, the bus voltage must exhibit a settling time lower than 1 [ms]. Since the ripple in the magnetizing current defines the peak values of the currents at both primary and secondary sides of the HFT, that peak ripple was limited to 5 [A]. Finally, the maximum switching frequency achievable with the adopted Mosfets is 30 [kHz], but any switching frequency below that value is acceptable.

Table 1. Parameters for the application example.

Parameter	symbol	Value
Battery voltage	v_b	12 [V]
Reference value for the bus voltage	v_r	48 [V]
Maximum ripple of the DC bus voltage	$\delta v_{dc}/v_{dc}$	0.5 [%]
Maximum perturbation of the DC bus voltage	$\Delta v_{dc}/v_{dc}$	± 3.5 [%]
Settling time of the DC bus voltage	t_s	1 [ms]
Maximum switching frequency	$F_{sw,max}$	30 [kHz]
Maximum ripple of the magnetizing current	δi_m	5 [A]
Maximum dc current	i_{dc}	± 1 [A]
Maximum instantaneous current perturbation	Δi_{dc}	± 2 [A]
Maximum dc current derivative	$\max\left(\frac{di_{dc}}{dt}\right)$	± 50 [A/ms]

5.1. Selection of the HFT

The second step is to select the HFT. Figure 5 shows the effect of L_m and n values on both δi_m and F_{sw} magnitudes. Such a figure was constructed using expressions (16), (17), (33) and (44) with the parameters in Table 1; the figure shows that reducing L_m increases, exponentially, the current ripple; while the switching frequency depends on both the ripple and inductance magnitudes. Decreasing the turn ratio n affects, in a similar way, both the current ripple and switching frequency. Thus, decreasing at the same time both the inductance and turn-ratio is not a suitable option; instead, increasing both L_m and n enables to select small ripples and low switching frequencies, but the HFT becomes bulkier, heavier, and more expensive.

The previous figure is useful to design a custom HFT since such an analysis enables to fine-tune both the turn-ratio and magnetizing inductance. However, construct an HFT is not a trivial task since specialized equipment is needed, e.g., a frequency analyzer. Therefore, using a commercial HFT is a simpler alternative; for example, Table 2 reports the characteristics of four commercial HFT designed for dc/dc applications. The turn-ratio of those HFT can be used to extract sections of Figure 5 to evaluate the current ripple and switching frequency imposed by those transformers.

Figure 5. Effect of L_m and n values on both δi_m and F_{sw} .

Table 2. Parameters of some commercial HFT designed for dc/dc applications.

Transformer	n [–]	L_m [μ H]	L_k [μ H]	Datasheet
XFRMS	1.4	35	0.45	[42]
Vitec	5.4	20	4	[43]
Nascent	8.0	75	11	[44]
Pulse	12	18	0.75	[45]

Figure 6 shows the effect of L_m on both δi_m and F_{sw} for the turn-ratio values of the HFT reported in Table 2, where a wide range of turn-ratios are available; i.e., from $n = 1.4$ to $n = 12$. The figure shows that XFRMS ($n = 1.4$) and Vitec ($n = 5.4$) HFT are able to provide both $\delta i_m < 5$ [A] and $F_{sw} < 30$ [kHz], operating near the limit of the feasibility zone due to the L_m and L_k values of those HFT, which are reported in Table 2. However, the Pulse ($n = 12$) HFT will provide a switching frequency under 20 [kHz], which is not desirable since that frequency is in the range of the audible noise. A similar, but much worst condition is achieved with the Nascent ($n = 8$) HFT, which will provide a switching frequency under 5 [kHz].

Another important analysis needed to define the HFT concerns the range of duty cycle available for the SMC: the average duty cycle of the flyback converter must not be near the saturation, otherwise the duty cycle could be saturated when the SMC acts to compensate a perturbation; therefore, it is desirable to have a duty cycle margin for the SMC operation. In this example, a margin of 30% is selected, thus the average duty cycle must be between 30% and 70%; such a value can be modified depending on the load profile. The average duty cycle achieved with the HFT of Table 2 was calculated from expressions (6), (15), and (16), and it is summarized in Figure 7. This analysis shows that XFRMS ($n = 1.4$) and Pulse ($n = 12$) transformers require an average duty cycle of 74% and 25%, respectively, thus those HFT are out of the desired duty cycle range. Instead, the Vitec ($n = 5.4$) and Nascent ($n = 8$) HFT are inside the desired duty cycle range with average duty cycles of 42.5% and 33.3%, respectively; however, the Vitec ($n = 5.4$) HFT provides a better duty cycle range since its average duty cycle is near to the 50%. Finally, the only HFT in Table 2 providing an acceptable switching frequency and duty cycle range is the Vitec ($n = 5.4$), thus such a transformer is selected to design the charger/discharger.

Figure 6. Effect of L_m on both δi_m and F_{sw} for turn-ratio values of some commercial HFT. (a) $n = 1.4$ and XFRMS HFT; (b) $n = 5.4$ and Vitec HFT; (c) $n = 8.0$ and Nascent HFT; (d) $n = 12.0$ and Pulse HFT.

Figure 7. Average duty cycle achieved with the HFT of Table 2.

The final calculation of this subsection concerns the hysteresis band limit, which is obtained from expression (44) using the inductances of the selected HFT, which results in $\delta \Psi = 0.5$ [A].

5.2. Selection of the Bus Capacitance

The third step is to design the bus capacitance to fulfill both the maximum ripple $\delta v_{dc}/v_{dc} < 0.5$ [%] and the maximum perturbation of the DC bus voltage $\Delta v_{dc}/v_{dc} < 3.5$ [%]. Therefore, expressions (16), (18), (44), and (49) are used to analyze the $\delta v_{dc}/v_{dc}$ and $\Delta v_{dc}/v_{dc}$ values for different bus capacitances, and those results are synthesized in Figure 8.

Figure 8. $\delta v_{dc}/v_{dc}$ and $\Delta v_{dc}/v_{dc}$ for different C_{dc} values.

The previous figure shows that any capacitor higher than 48.85 μF , which is the minimum C_{dc} acceptable, fulfills both the maximum ripple and maximum perturbation of the DC bus voltage. From the figure, it is evident that such a limit C_{dc} value fulfills the maximum $\Delta v_{dc}/v_{dc}$, and provides a much smaller ripple $\delta v_{dc}/v_{dc}$. Finally, the bus capacitor is selected as the near commercial value $C_{dc} = 50 \mu\text{F}$, which provides $\Delta v_{dc}/v_{dc} = 3.4 \%$ and $\delta v_{dc}/v_{dc} = 0.35 \%$, thus fulfilling both maximum ripple and maximum perturbation of the DC bus voltage.

5.3. Calculation of K_v

The fourth step is to calculate the K_v parameter of the SMC using expression (36), which must fulfill the stability conditions given in (24), (29), and (30). Figure 9 shows the K_v values for different settling times and bus capacitances, taking into account that such K_v values fulfill the stability conditions. Finally, in that figure are highlighted the $C_{dc} = 50 \mu\text{F}$ value selected in the previous subsection, and the maximum settling time $t_s = 1 \text{ ms}$, which results in the $K_v = 0.2 \text{ A/V}$ value. Since the selected condition [$t_s = 1 \text{ ms}$, $C_{dc} = 50 \mu\text{F}$, $K_v = 0.2 \text{ A/V}$] is within the feasibility zone defined by the stability conditions, $K_v = 0.2 \text{ A/V}$ ensures both global stability of the SMC and the desired settling time $t_s = 1 \text{ ms}$ for the bus voltage.

Figure 9. K_v calculation for different settling times and bus capacitances.

Finally, the fourth step described in this section enables to design a stable battery charger/discharger, based on the flyback topology, fulfilling the conditions required to ensure a safe operation for both sources and loads connected to a DC bus.

6. Simulation Results

This section presents circuital simulations of the proposed battery charger/discharger, which validate the design procedure developed in the previous sections. Figure 10 shows the circuital implementation of the battery charger/discharger in the power electronics simulator PSIM, where the flyback converter follows the same circuital structure described in the theoretical circuit of Figure 2, including the voltage sensors for v_{dc} and v_b , and the current sensors for i_p , i_s and i_{dc} .

Figure 10. Circuital implementation of the battery charger/discharger in PSIM.

The circuital implementation also includes the implementation of the adaptive sliding-mode controller described in Figure 3, where can be observed the dynamic calculation of K_i . Such SMC implementation is defined by the hysteresis band limit $\delta\Psi$ using two voltage sources, but such a limit could be also imposed using zener diodes, requiring a single power source for polarization. The addition/subtraction and gain functions can be implemented using operational amplifiers, while the multiplication and division functions can be implemented with integrated circuits. Moreover, the S-R flip-flop produces the main u and complementary $\bar{u}$ control signals, which are observed in the circuital implementation of Figure 10. Finally, the simulation uses a current source to produce the dc current profile in the bus, which could produce three possible states: discharge the battery ($i_{dc} > 0$), charge the battery ($i_{dc} < 0$), and battery in stand-by ($i_{dc} = 0$); thus, the SMC must be able to regulate the charger/discharger in those operating conditions.

6.1. Performance Evaluation

The first test, reported in Figure 11, evaluates the correct operation of the charger/discharger concerning the ripple limits. Thus, the charger/discharger was set in the operating conditions defined for the design process (Table 1), with a bus current $i_{dc} = 1$ [A] and a reference $v_r = 48$ [V], which produces a duty cycle $d = 42.5$ [%], a switching frequency $F_{sw} = 25.3$ [kHz] and $K_i = 0.1067$ [A/V]. Therefore, the steady-state duty cycle is inside the acceptable range defined in Figure 7, and the switching frequency is lower than the maximum limit $F_{sw,max} = 30$ [kHz] defined in Table 1. The simulation reports a DC voltage ripple $\delta v_{dc} = 0.36$ [%] (top waveforms), which is lower than the maximum

acceptable ripple of 0.5 [%]; this is expected since the bus capacitor was defined as higher than the minimum limit reported in Figure 8. In addition, the current ripple in i_m is equal to the design value $\delta i_m = 5$ [A] imposed in Table 1 (second waveforms), this is expected since the magnetizing inductance of the selected Vitec HFT imposes that δi_m value as observed in Figure 6b. The simulation also confirms the stability of the SMC (third waveforms), since the switching function Ψ is always trapped inside the hysteresis band $[-0.5, +0.5]$, where $\delta\Psi = 0.5$ [A] was calculated at the end of Section 5.1. Finally, the control signal u is depicted at the bottom of the figure, which confirms the control law: $u = 1$ imposes a positive switching function derivative (Ψ increases), and $u = 0$ imposes a negative switching function derivative (Ψ decreases).

Figure 11. Steady-state operation for $i_{dc} = 1$ [A].

The second test is performed to evaluate the reachability of the surface starting from outside of the hysteresis band. Figure 12 shows a first simulation in which the switching function starts above the hysteresis band ($\Psi > +\delta\Psi$), where the SMC follows the practical control law reported in (41): when $\Psi = \Psi_p > +\delta\Psi$ the control signal is set to 0 ($u = 0$), which imposes a negative derivative on the switching function ($\frac{d\Psi}{dt} < 0$), forcing Ψ to enter in the hysteresis band $[-0.5, +0.5]$, keeping the switching function trapped into that band, which ensures global stability. A second simulation shows a similar behavior, but with the switching function starting below the hysteresis band ($\Psi < -\delta\Psi$). In this case, the control signal is set to 1 ($u = 1$) to impose a positive derivative on the switching function ($\frac{d\Psi}{dt} > 0$), forcing Ψ to enter in the hysteresis band, also keeping the switching function trapped into that band; this is in agreement with the SMC control law (41). Therefore, the simulations of Figure 12 confirm that the designed SMC fulfills the reachability conditions, since the charger/discharger is always controlled to enter into the sliding surface from any operation condition outside the surface, thus the system is always driven to stability.

The third test is designed to evaluate the response of the charger/discharger to current derivatives on the DC bus surpassing the limit defined in Table 1. This condition can occur when a load connected to the bus experiments a failure leading to a short-circuit, thus requesting a large current step to the bus. Similarly, if a source experiments a sudden failure, thus will produce a step in current requested by the loads to the battery, since the current provided by the sources will be instantaneously reduced. Figure 13 presents a first simulation (left) in which the bus current changes with the design limit $\frac{di_{dc}}{dt} \leq 50$ [A/ms],

thus the switching function remains inside the hysteresis band. This confirms that the SMC parameters fulfill both the transversality and reachability conditions imposed in (24), (29), and (30), which provide both global stability and the desired bus voltage performance. The second simulation (right) considers a bus current perturbation with almost infinite derivative (step change), thus $\frac{di_{dc}}{dt} \geq 50$ [A/ms], which forces the switching function to leave the hysteresis band. However, since that high current derivative disappears when the perturbation ends, the reachability of the SMC forces the system to enter the hysteresis band, ensuring again global stability. Therefore, the proposed charger/discharger and SMC could support even step-like perturbations in the DC bus current, since the reachability conditions will force the system into stability as demonstrated in the previous and these tests, i.e., simulations reported in Figures 12 and 13.

Figure 12. Reachability of the hysteresis band. Left: reachability from $\Psi > +\delta\Psi$; Right: reachability from $\Psi < -\delta\Psi$.

Figure 13. Stability on low-frequency and high-frequency current perturbations. **Left:** low-frequency perturbation; **Right:** high-frequency perturbation.

The fourth test evaluates the performance of the charger/discharger in compensating the bus voltage after a step-current occurs in the DC bus. The results of this test are reported in Figure 14, where the maximum instantaneous current perturbation of 2 [A], defined in Table 1, is considered. Since the bus capacitor was designed under the minimum C_{dc} capacitor reported in Figure 8, the maximum voltage deviation achieved with the designed charger/discharger is lower than the limit defined in Table 1 (3.5%), achieving $\Delta v_{dc}/v_{dc} = 3.35\%$. Thus, the designed charger/discharger ensures a safe bus voltage to the devices connected to the bus, even under an extreme step-like perturbation on the bus current. This satisfactory behavior is achieved due to the dynamic change of the K_i parameter, which enables the SMC to adapt the sliding surface to the instantaneous operation conditions of the system. Finally, the simulation also confirms that the settling time $t_s = 1$ [ms] for the bus voltage, imposed in Table 1, is achieved; this precise behavior is caused by the exact calculation of $K_v = 0.2$ [A/V] performed in Figure 9, which takes into account the $C_{dc} = 50$ [μ F] value adopted for the implementation. In conclusion, this test confirms the correctness of the closed-loop dynamics reported in expression (35), and the accurate calculation of K_v using expression (36) and Figure 9.

The last test is designed to evaluate the charger/discharger behavior in the three possible operating states: battery discharge ($i_{dc} > 0$), battery charge ($i_{dc} < 0$), and battery in stand-by ($i_{dc} = 0$). Moreover, the test also evaluates the performance of the system for the transition between those operation states, which is a realistic condition since the power flow requested to the battery could suddenly change depending on the operation of both sources and loads. The results of this test are presented in Figure 15, where the DC bus current changes from 1 [A] (battery discharge), to 0 [A] (battery in stand-by) to -1 [A] (battery charge). Since the perturbations have a 1 [A] amplitude, which is half of the perturbation evaluated in the previous test, the deviation of the DC bus voltage is much smaller, thus a safe operation is provided to the devices connected to the bus. Moreover, the simulation also reports the duty cycle, which is never saturated; therefore, the equivalent control condition (31)–(32) is always fulfilled and the system has global stability for all the operating conditions. Similarly, the switching frequency is always lower than the maximum limit (44), defined in Table 1, which confirms the correctness of the HFT selection reported in Figure 6b. In conclusion, this last test demonstrates the ability of the proposed charger/discharger to operate in all the possible conditions of the battery, providing global stability within those states and in the transitions between the states.

Figure 14. Performance in the compensation of the bus voltage.

Figure 15. Transition between battery discharge, battery charge, and battery in stand-by.

Summarizing, the five tests performed to the proposed charger/discharger verify the global stability of the system, the correct design of the circuit and controller parameters, the satisfactory regulation of the bus voltage, and the correct operation of the system for charging, discharging, and stand-by conditions. Therefore, it is confirmed that this solution will provide safe conditions to the devices connected to the DC bus, which is the main objective of a battery charger/discharger in a microgrid.

6.2. Comparison with a Classical Control System

An additional evaluation was carried out by contrasting the performance of the proposed SMC with a classical solution based on PI controllers. The first step to design this classical controller solution is to obtain a linearized model depending on the duty cycle d of the converter. This process starts with the averaged model presented in Section 2.2, which is evaluated at the steady-state conditions defined in Section 2.3 using the values given in Tables 1 and 2 (Vitec HFT). The resulting linear model is given in expressions (50) and (51), which describe the small-signal models of both the bus voltage and magnetizing current depending on the duty cycle.

$$\frac{\hat{v}_{dc}}{\hat{d}} = \frac{-3.471 \times 10^4 \cdot s + 2.222 \times 10^9}{s^2 + 1.131 \times 10^7} \quad (50)$$

$$\frac{\hat{i}_m}{\hat{d}} = \frac{1.041 \times 10^6 \cdot s + 1.839 \times 10^8}{s^2 + 1.131 \times 10^7} \quad (51)$$

Analyzing the small-signal model of the bus voltage, given in (50), shows that the system exhibits a non-minimum phase behavior due to the positive zero of the transfer function, thus it will be almost impossible to regulate the bus voltage with a single PI controller. This type of system is commonly controlled using a cascade structure [24,26], where an inner controller regulates another state variable to reduce the order of the system. In this case, the other state variable available is the magnetizing current, which small-signal model (51) has a negative zero, thus it has a minimum phase behavior that can be regulated with a single PI controller. Then, the current control loop reported in (52) was designed, using the pole-placement technique [46], to provide a settling time of the magnetizing

current (i_m) equal to 0.2 ms and a closed-loop bandwidth of 8 kHz, which is below the switching frequency imposed by the PWM driving the Mosfets ($F_{sw} = 30$ kHz).

$$\text{Current control loop} \Rightarrow \hat{d} = \frac{0.037 \cdot (s + 1.442 \times 10^4)}{s} \cdot (\hat{i}_r - \hat{i}_m) \quad (52)$$

Since the settling time of i_m is five times smaller than the settling time defined in Table 1 for the bus voltage ($t_s = 1.0$ ms), the cascade voltage controller is designed by considering a correct control of the magnetizing current, thus $\hat{i}_m \approx \hat{i}_r$ where $\hat{i}_r$ is the small-signal reference for the magnetizing current. Therefore, the dc bus voltage model is simplified by assuming $\hat{i}_m \approx \hat{i}_r$ to obtain the reduced-order model reported in (53), which describes the behavior of the bus voltage to changes on the magnetizing current. Finally, a voltage control loop is designed to provide the current reference $\hat{i}_r$ to the current control loop; such a voltage control loop, reported in (54), was designed using the pole-placement technique to provide the desired settling time and maximum voltage deviation defined in Table 1.

$$\frac{\hat{v}_{dc}}{\hat{i}_m} = \frac{0.5761}{0.00027 \cdot s} \quad \text{where} \quad \hat{i}_m \approx \hat{i}_r \quad (53)$$

$$\text{Voltage control loop} \Rightarrow \hat{i}_r = \frac{5.568 \cdot (s + 3960)}{s} \cdot (v_r - \hat{v}_{dc}) \quad (54)$$

The output of the inner (current) control loop is the duty cycle, thus a PWM is used to impose that duty cycle to the Mosfets with a fixed switching frequency $F_{sw} = 30$ kHz. Figure 16 presents the comparison between the performance of the proposed SMC solution and the classical cascade PI structure presented in this subsection. The main perturbation of the charger/discharger is the bus current which exhibits changes with the amplitude defined in Table 1: it is observed that the proposed SMC ensures both the desired settling time and maximum voltage deviation, while the PI structure only fulfills the settling time since the voltage deviation is higher than the limit Δv_{dc} . Despite the PI structure was designed to ensure the desired voltage deviation, the change in the duty cycle modifies the operating point of the system, which prevents that the PI structure from being able to ensure the desired performance.

Figure 16. Comparison between the proposed SMC and a classical PI structure.

Moreover, the simulation of Figure 16 shows the dynamic advantage of the SMC over the PI structure, since the magnetizing current reaches the steady-state condition much faster, thus a lower bus voltage deviation occurs. This is also observed in the duty cycle imposed by the controllers, where the SMC imposes a faster control action in comparison with the PI structure, thus ensuring a fast compensation of the bus voltage. It must be noted that the PI structure defined in (52) and (54) was designed near the speed limit imposed by the switching frequency defined in Table 1: the maximum bandwidth of the inner controller is usually between $1/10 = 0.1$ and $1/5 = 0.2$ of the switching frequency since that is the range of validity for the linearized model [46], in this example, it was possible to increase that ratio to 0.266, but further increments could cause an unstable operation. Therefore, classical linear controllers are not able to ensure the desired behavior of the flyback charger/discharger for all the operating conditions; instead, following the design procedure proposed in this paper ensures that the proposed SMC imposes the desired performance under any condition.

7. Conclusions

The correct design of power and control stages of a battery charger/discharger was presented and validated in this paper. The development of three battery charger/discharger models in order to: design an SMC, establish design equations, and operate the system under requirements and safely, were presented. Particularly, the design equations were used to graph the relations among variables, parameters, and limits enlightening the design procedure. The requirement conditions include maximum ripple and perturbation of the DC bus voltage, a settling time of the DC bus voltage, a maximum switching frequency, and a maximum ripple of the magnetization current. All the requirements were achieved and illustrated through five tests carried out in PSIM. The first test evaluated the correct operation of the battery charger/discharger concerning the ripple limits; the second test evaluated the reachability of the surface achieved by the SMC; the third test verified the response of the battery charger/discharger to current derivatives on the DC bus; the fourth test evaluated the performance of the battery charger/discharger in regulating the bus voltage after a step of current in the DC bus; and the fifth test verified the behavior of the battery charger/discharger in the three possible operating states: charge, discharge, and battery stand-by. That test also evaluated the transition between states. Finally, a comparison of the SMC solution with a classical PI structure was carried out. Although the PI controller was designed to fulfill the requirements of the battery charger/discharger, specifically a desired voltage deviation, the change on the duty cycle modified the operating point of the system, which disabled the PI structure to ensure the desired performance criteria. Because of the excellent behavior of the system facing the perturbations, future work can be focused on extending the design to include the uncertainties of the experimental implementation.

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