Article

High Linearity DC-38 GHz CMOS SPDT Switch

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Abstract: In this paper, we demonstrate a low-loss and high-linearity DC-38 GHz CMOS SPDT switch for 5G multi-band communications in 0.18 μm CMOS. Traveling-wave matching (CLCL network) is used for the output-port (ports 2 and 3) matching and isolation enhancement, while π -matching (CLC matching) is adopted for the input-port (port 1) matching. Positive/negative gate-bias is adopted for linearity enhancement because larger P_{in} (i.e., AC signal with larger negative V_{in}) is required to conduct the off-state series switch transistor. Negative-body bias is used for insertion-loss reduction because the off-state series switch transistor is closer to an open state. The SPDT switch achieves insertion loss of 0.4–1.4 dB, 3.6–4.3 dB, and 4.5–5.9 dB, respectively, for DC-6 GHz, 21–29 GHz, and 31–38 GHz. Moreover, the SPDT switch achieves isolation of 37.5–59.4 dB, 25.7–28.7 dB, and 24.3–25.2 dB, respectively, for DC-6 GHz, 21–29 GHz, and 31–38 GHz. At 28 GHz, the SPDT switch achieves remarkable input 1-dB compression point ($IP_{1\text{dB}}$) of 25.6 dBm, close to the simulated one (28 dBm). To the authors' knowledge, this is one of the best $IP_{1\text{dB}}$ results ever reported for millimeter-wave (mm-wave) SPDT switches.

Keywords: CMOS; millimeter-wave; SPDT; switch

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1. Introduction

The 5G new radio (NR) frequency bands include the sub-6 GHz frequency range 1 (FR1) and the 24.25–52.6 GHz frequency range 2 (FR2). Compared with the compound semiconductor technologies [1], CMOS processes have the advantages of low cost and high integration [2–6]. Recently, CMOS phased-array transceivers for 28 GHz 5G systems have become popular due to the rapid advancement of the CMOS technology [7,8]. For instance, [8] demonstrates a 28 GHz phased-array transceiver with data rate of 15 Gb/s in 65 nm CMOS for 5G NR band N257 (26.5–29.5 GHz). There are several types of millimeter-wave (mm-wave) switches, such as the single-pole single-throw (SPST) switch, the single-pole double-throw (SPDT) switch, the double-pole single-throw (DPST) switch, and the double-pole double-throw (DPDT) switch (see Figure 1). The DPST switch is equivalent to the combination of two SPST switches, while the DPDT switch is equivalent to the combination of two SPDT switches. For time-division duplexing (TDD) mm-wave communication systems, mm-wave switches are important components. In each path of the mm-wave phased-array transceivers, instead of using two independent antennas (i.e., one receive antenna and one transmit antenna), the SPDT switch can be used for switching between the transmit mode and the receive mode. This leads to a 50% reduction of the required number of antennas.

Figure 1. Illustrative diagrams of the (a) SPST, (b) SPDT, (c) DPST, and (d) DPDT switch.

On-chip SPDT switch normally exhibits decent insertion loss, isolation, and power-handling capability (in the transmit mode). For the SPDT switch in Figure 1b, in the condition of port-1-to-port-2 (P1-to-P2) being on and port-1-to-port-3 (P1-to-P3) being off, the signals from the transmitter (at port 2) are sent to the antenna (at port 1) for transmit. Decent P1-to-P3 isolation (antenna-to-RX isolation) and P2-to-P3 isolation (TX-to-RX isolation) (i.e., small S_{31} and S_{32}) are required. Moreover, in the condition of P1-to-P2 being off and P1-to-P3 being on, the signals received by the antenna (at port 1) are sent to the receiver (at port 3). Decent P1-to-P2 isolation (antenna-to-TX isolation) and P2-to-P3 isolation (i.e., small S_{21} and S_{32}) are required. Overall, in addition to small chip area, the basic requirements for an SPDT switch include small input return loss (for port-1 and the on-state port, and almost total reflection for the off-state port), low insertion loss, good isolation, and decent power handling capability (normally evaluated by the input 1-dB compression (IP_{1dB})) over the band of interest. For sub-6 GHz, SPDT switch with series-shunt transistor structure is commonly used due to its low insertion loss, high isolation, good power performance, and small area [6]. This SPDT switch structure normally exhibits small input and output matching bandwidth from DC to several GHz, so it is not applicable to the mm-wave band. For the 24.25–52.6 GHz (mainly 28/39 GHz) FR2 5G band, $\lambda/4$ -transmission-line (TL)-based SPDT switches are commonly used due to its low insertion loss, decent isolation, and good power performance [9,10]. However, this SPDT switch has the disadvantage of occupying a relatively large chip area. To reduce the chip area, lumped-LC-based or transformer-based SPDT switches have been proposed [11]. These SPDT switch structures normally exhibit medium insertion-loss (or gain) bandwidth around the center frequency, not including the sub-6 GHz band. Clearly, the abovementioned SPDT switches are not suitable for dual band, such as the sub-6 GHz and the 28 GHz, 5G applications. A wideband SPDT switch structure, which covers the sub-6 GHz and the 28 GHz 5G bands, is desirable.

Several excellent mm-wave SPDT switches have been reported (see Table 1) [1–6]. However, the overall performance still has room for improvement. For instance, in [4], a 15–25 GHz SPDT switch with alternate nMOS and pMOS as series and shunt transistors in 28 nm CMOS process is demonstrated. Low insertion loss of 0.6–2 dB is achieved. However, isolation of 15–31.5 dB and IP_{1dB} of 22.1 dBm are not good enough. In this work, to demonstrate that low insertion-loss, high isolation (greater than 24 dB), high linearity (IP_{1dB} greater than 25 dBm), and wideband (covering the sub-6 GHz and the 28 GHz bands) operation can be achieved for a CMOS SPDT, we propose a low insertion-loss, high isolation, and high-linearity CMOS SPDT switch with single-series-double-shunt transistor structure and π /traveling-wave input/output matching for sub-6 GHz and 28 GHz 5G communications. Traveling-wave- and π -matching are adopted for broadband output and input matching, respectively. The required capacitance for the traveling-wave-matching is

provided by the parasitic capacitance at drain nodes of the double-shunt transistors (M_2 , M_3 , M_5 , and M_6 in Figure 2). The required right-side capacitance for the π -matching is provided by the parasitic capacitance at source node of the single-series transistors (M_1 and M_4 in Figure 2). Positive/negative gate-bias and negative body-bias are used for linearity and insertion loss enhancement, respectively. The proof-of-concept SPDT switch is designed and implemented in a cost-effective 1P6M 0.18 μm CMOS process (with cutoff frequency f_T of 60 GHz), which has been used to design and implement a 28 GHz receiver front-end with acceptable performance [12]. Instead of the adopted 0.18 μm CMOS process, insertion losses of the SPDT switch can be further enhanced if an advanced process, such as the 28 nm CMOS process with thicker top metal layer in [4], is available.

Figure 2. Circuit diagram and chip photo of the DC-38 GHz SPDT switch.

Table 1. Summary of this work and recently reported SPDT switches.

	Frequency (GHz)	Insertion Loss (dB)	Isolation (dB)	IP _{1dB} (dBm)	CMOS Process
This Work	0–6	0.4–1.4	37.5–59.4	NA	0.18 μm
	21–29	3.6–4.3	25.7–28.7	25.6 (@28 GHz)	
	31–38	4.5–5.9	24.3–25.2	NA	
[1]	35–70	2.2–2.9	>40	17.3 (@45 GHz)	0.1 μm PHEMT
[2]	0–20	0.4–1	20–42.7	15 (@10 GHz)	0.18 μm SOI
	20–40	1–5	17–20	NA	
[3]	24	3.5	16	28.7	90 nm
[4]	15–25	0.6–2	15–31.5	22.1 * (@20 GHz)	28 nm
[5]	5	2	42.7	21 *	0.18 μm
[6]	0–10	0.4–1.8	23–42	20 (@5.8 GHz)	0.18 μm

* Simulation. + 0.3 dB compression point.

2. Circuit Design

Figure 2 shows the circuit diagram and chip microphotograph of the SPDT switch. The SPDT switch occupies a chip area of $0.619 \times 0.633 \text{ mm}^2$, i.e., 0.392 mm^2 . The SPDT switch is design and implemented by a 1P6M 0.18 μm CMOS process with top metal (M_6) thickness of $2.34 \mu\text{m}$. The interconnection lines and inductors are mainly implemented by M_6 . Only the underneath interconnection lines are implemented by the fifth-layer metal (M_5). Traveling-wave (CLCL) matching is used for isolation and output-port (ports 2 and 3) matching enhancement. π (CLC)-matching is used for the input-port (port 1) matching. Positive/negative gate-bias is used for linearity enhancement because larger input power P_{in} (i.e., AC signal with larger negative input voltage V_{in}) is required to conduct the off-state series switch transistor. Negative-body bias is adopted for insertion-loss reduction mainly due to the off-state series switch transistor being closer to an open-state.

Figure 3a–c shows the simulated scattering parameters (S-parameters) versus frequency characteristics of the SPDT switch in the condition of P1-to-P2 being on and P1-to-P3 being off. The bias conditions are $V_{\text{DD}}/V_{\text{SS}} = 1.8 \text{ V}/-1.8 \text{ V}$ and $V_{\text{DD}}/V_{\text{SS}} = 2.5 \text{ V}/-2.5 \text{ V}$. Figure 3a shows the simulated input reflection coefficient at port-1 (S_{11}) and port-2 (S_{22}). At $V_{\text{DD}}/V_{\text{SS}}$ of $2.5 \text{ V}/-2.5 \text{ V}$, the SPDT switch achieves minimum S_{11} of -29.2 dB at DC,

and S_{11} smaller than -10 dB for 0–34.1 GHz, corresponding to -10 dB input matching bandwidth ($f_{10\text{dB}}$) of 34.1 GHz. The result is close to the simulated one ($f_{10\text{dB}}$ of 33.8 GHz (0–33.8 GHz)) for $V_{\text{DD}}/V_{\text{SS}}$ of 1.8 V/−1.8 V. Moreover, at $V_{\text{DD}}/V_{\text{SS}}$ of 2.5 V/−2.5 V, the SPDT switch achieves minimum S_{22} of -29.3 dB at DC, and S_{22} smaller than -10 dB for 0–39.9 GHz, corresponding to $f_{10\text{dB}}$ of 39.9 GHz. The result is close to the simulated one ($f_{10\text{dB}}$ of 40.5 GHz (0–40.5 GHz)) for $V_{\text{DD}}/V_{\text{SS}}$ of 1.8 V/−1.8 V.

Figure 3. Simulated (a) S_{11} and S_{22} ; (b) S_{21} and S_{31} ; (c) S_{33} and S_{32} ; and (d) $\text{IP}_{1\text{dB}}$ of the SPDT switch.

Figure 3b shows the simulated S_{21} and S_{31} . The magnitude of S_{21} is the insertion loss between port 1 and port 2. For $V_{\text{DD}}/V_{\text{SS}}$ of 2.5 V/−2.5 V, the SPDT switch achieves S_{21} lower than 2.4 dB for 0–28 GHz and 5.6 dB for 0–38 GHz. The result is slightly better than the simulated one (insertion loss lower than 2.6 dB for 0–28 GHz and 5.9 dB for 0–38 GHz) for $V_{\text{DD}}/V_{\text{SS}}$ of 1.8 V/−1.8 V because transistors M_1 and M_2/M_3 are closer to being short and open, respectively. Moreover, the magnitude of S_{31} is the isolation between port 1 and port 3. For $V_{\text{DD}}/V_{\text{SS}}$ of 2.5 V/−2.5 V, the SPDT switch achieves S_{31} better than 25.5 dB for 0–28 GHz and 25.26 dB for 0–38 GHz. The result is slightly better than the simulated one (isolation better than 23.9 dB for 0–28 GHz and 23.66 dB for 0–38 GHz) for $V_{\text{DD}}/V_{\text{SS}}$ of 1.8 V/−1.8 V because transistors M_4 and M_5/M_6 are closer to being open and short, respectively.

Figure 3c shows the simulated input reflection coefficient at port-3 (S_{33}) and S_{32} of the SPDT switch. For 0–38 GHz, the SPDT switch achieves S_{33} of -1.66 ~ -3.83 dB for $V_{\text{DD}}/V_{\text{SS}}$ of 2.5 V/−2.5 V, and -1.94 ~ -4.22 dB for $V_{\text{DD}}/V_{\text{SS}}$ of 1.8 V/−1.8 V, close to the ideal value of 0 dB (i.e., port 3 is short). Compared with $V_{\text{DD}}/V_{\text{SS}}$ of 1.8 V/−1.8 V, better S_{33} is achieved for $V_{\text{DD}}/V_{\text{SS}}$ of 2.5 V/−2.5 V because transistors M_4 and M_5/M_6 are closer to being open and short, respectively. Moreover, the magnitude of S_{32} is the isolation between the transmitter and the receiver (TX-to-RX isolation). For $V_{\text{DD}}/V_{\text{SS}}$ of 2.5 V/−2.5 V, the SPDT switch achieves TX-to-RX isolation better than 25.9 dB for 0–28 GHz and 22.5 dB for

0–38 GHz. The result is slightly better than the simulated one (TX-to-RX isolation better than 23.8 dB for 0–28 GHz and 20.6 dB for 0–38 GHz) for V_{DD}/V_{SS} of 1.8 V/−1.8 V because transistors M_4 and M_5/M_6 are closer to being open and short, respectively.

Figure 3d shows the simulated power gain (i.e., $P_{out}(\text{dBm}) - P_{in}(\text{dBm})$) against P_{in} characteristics at 28 GHz in various V_{G2} and V_B conditions. As can be seen, positive/negative gate-bias is helpful for linearity enhancement (15.1 dBm, from 16 dBm (for the case with $V_{G1}/V_{G2}/V_B$ of 2.5 V/0/0) to 31.1 dBm (for the case with $V_{G1}/V_{G2}/V_B$ of 2.5 V/−2.5 V/0)) because larger P_{in} (i.e., AC signal with larger negative V_{in}) is required to conduct the off-state series switch transistors M_4 . Negative-body bias is helpful for insertion-loss reduction due to M_4 being closer to being open.

3. Results

On-wafer three-port S-parameters measurement of the SPDT switch was conducted by a Keysight N5245A network analyzer. Figure 4a–c shows the measured S-parameters versus frequency characteristics of the SPDT switch in the condition of P1-to-P2 being on and P1-to-P3 being off. Figure 4a shows the measured S_{11} and S_{22} of the SPDT switch. At $V_{DD}(=V_{G1})/V_{SS}(=V_{G2}=V_B)$ of 2.5 V/−2.5 V, the SPDT switch achieves S_{11} of −12.6~−26.8 dB for 0.1–6 GHz and −7.3~−26.8 dB for 0.1–38 GHz. The result is close to the measured one (−12.4~−25.8 dB for 0.1–6 GHz and −7.2~−25.8 dB for 0.1–38 GHz) for V_{DD}/V_{SS} of 1.8 V/−1.8 V, and the one (−11.1~−26.8 dB for 0.1–6 GHz and −6.1~−26.8 dB for 0.1–38 GHz) for V_{DD}/V_{SS} of 1.8 V/0 V. Moreover, at V_{DD}/V_{SS} of 2.5 V/−2.5 V, the SPDT switch achieves S_{22} of −12.5~−25.7 dB for 0.1–6 GHz and −6.9~−25.7 dB for 0.1–38 GHz. The result is close to the measured one (−12.5~−25.7 dB for 0.1–6 GHz and −6.9~−25.7 dB for 0.1–38 GHz) for V_{DD}/V_{SS} of 1.8 V/−1.8 V, and the one (−12.5~−25.7 dB for 0.1–6 GHz and −6.9~−25.7 dB for 0.1–38 GHz) for V_{DD}/V_{SS} of 1.8 V/0 V.

Figure 4. Measured (a) S_{11} and S_{22} ; (b) S_{21} and S_{31} ; (c) S_{33} and S_{32} , and (d) IP_{1dB} of the SPDT switch.

Figure 4b shows the measured S_{21} and S_{31} of the SPDT switch. For V_{DD}/V_{SS} of 2.5 V/−2.5 V, the SPDT switch achieves insertion loss of 0.4–1.4 dB for 0.1–6 GHz, 3.6–4.3 dB for 21–29 GHz, and 4.5–5.9 dB for 31–38 GHz. The result is close to the measured one (0.5–1.5 dB for 0.1–6 GHz, 3.8–4.6 dB for 21–29 GHz, and 4.8–6.4 dB for 31–38 GHz) for V_{DD}/V_{SS} of 1.8 V/−1.8 V, and better than the one (0.5–1.7 dB for 0.1–6 GHz, 4.5–5.6 dB for 21–29 GHz, and 5.9–7.9 dB for 31–38 GHz) for V_{DD}/V_{SS} of 1.8 V/0 V. Clearly, positive/negative gate-bias and negative body-bias are helpful for insertion-loss reduction, mainly due to the off-state series switch transistor M_4 being more close to being open. Moreover, the SPDT switch achieves isolation of 37.5–59.4 dB for 0.1–6 GHz, 25.7–28.7 dB for 21–29 GHz, and 24.3–25.2 dB for 31–38 GHz. The result is close to the measured one (35.7–60.3 dB for 0.1–6 GHz, 24.2–26.5 dB for 21–29 GHz, and 23–23.7 dB for 31–38 GHz) for V_{DD}/V_{SS} of 1.8 V/−1.8 V, and the one (35.6–60.3 dB for 0.1–6 GHz, 25.2–27.4 dB for 21–29 GHz, and 24.4–24.8 dB for 31–38 GHz) for V_{DD}/V_{SS} of 1.8 V/0 V.

Figure 4c shows the measured S_{33} and S_{32} of the SPDT switch. For 0–38 GHz, the SPDT switch achieves S_{33} of −1.99~−3.05 dB for V_{DD}/V_{SS} of 2.5 V/−2.5 V, −2.23~−3.25 dB for V_{DD}/V_{SS} of 1.8 V/−1.8 V, and −1.84~−2.87 dB for V_{DD}/V_{SS} of 1.8 V/0 V, close to the ideal value of 0 dB (i.e., port 3 is short). Compared with V_{DD}/V_{SS} of 1.8 V/−1.8 V, better S_{33} is achieved for V_{DD}/V_{SS} of 2.5 V/−2.5 V because transistors M_4 and M_5/M_6 are closer to being open and short, respectively. Moreover, for V_{DD}/V_{SS} of 2.5 V/−2.5 V, the SPDT switch achieves TX-to-RX isolation better than 25.4 dB for 0–28 GHz and 23.6 dB for 0–38 GHz. The result is slightly better than the simulated one (TX-to-RX isolation better than 24.4 dB for 0–28 GHz and 22.6 dB for 0–38 GHz) for V_{DD}/V_{SS} of 1.8 V/−1.8 V because transistors M_4 and M_5/M_6 are closer to being open and short, respectively. P_{out} versus P_{in} measurement of the SPDT switch was conducted by a Keysight N9030A PXA signal analyzer in conjunction with a Keysight E8257D PSG analog signal generator.

Figure 4d shows the measured power gain versus P_{in} characteristics of the SPDT switch at 28 GHz and V_{G1} (equal to V_{DD}) of 1.8 V in the condition of P1-to-P2 being on and P1-to-P3 being off. As can be seen, the SPDT switch with V_{G2} and V_B (equal to V_{SS}) of −1.8 V achieves IP_{1dB} of 25 dBm and power gain of −4.3 dB (at P_{in} of 0 dBm), better than those (IP_{1dB} of 20 dBm and power gain of −5.6 dB at P_{in} of 0 dBm) of the SPDT switch with V_{G2} and V_B of 0 V. Moreover, in the bias condition of V_{DD}/V_{SS} equal to 2.5 V/−2.5 V, the SPDT switch achieves measured IP_{1dB} of 25.6 dBm, close to the simulated value of 28 dBm. To the authors' knowledge, this is one of the best IP_{1dB} results ever reported for mm-wave SPDT switches. Clearly, positive/negative gate-bias and negative body-bias are beneficial for linearity enhancement because larger P_{in} (i.e., AC signal with larger negative V_{in}) is required to conduct the off-state series switch transistor M_4 .

Table 1 is a summary of the SPDT switch and recent reported state-of-the-art SPDT switches with similar operation frequency. Compared with the SPDT switch in 0.1 μ m GaAs PHEMT in [1], our SPDT switch achieves better IP_{1dB} . Compared with the SPDT switch in 0.18 μ m SOI CMOS in [2], our SPDT switch achieves comparable return loss, insertion loss, and better isolation and IP_{1dB} . Compared with the SPDT switch in 90 nm CMOS in [3], our SPDT switch achieves better insertion loss and isolation. Compared with the SPDT switches in 28 nm and 0.18 μ m CMOS in [4–6], our SPDT switch achieves comparable return loss, insertion loss, and isolation, and better $IP_{0.3dB}/IP_{1dB}$. Overall, the results indicate that the SPDT switch is suitable for multi-band 5G communications.

4. Conclusions

In conclusion, a wideband and high-performance SPDT switch structure, which covers the sub-6 GHz and the 28 GHz 5G bands, is desirable. Most SPDT switches are not applicable to these two bands due to limited bandwidth. Although there are a few SPDT switch structures covering these two bands, the overall performance, especially the IP_{1dB} , still has room for improvement. In this work, we demonstrate a low insertion-loss, high isolation, and high-linearity DC–38 GHz CMOS SPDT switch for sub-6 GHz and 28 GHz 5G communications. Wideband input matching is achieved by adopting the π -matching (CLC

matching). Broadband output matching and isolation enhancement (between the outputs) are attained by using the traveling-wave matching (CLCL network). Positive/negative gate-bias is adopted for linearity enhancement because larger P_{in} (i.e., AC signal with larger negative V_{in}) is required to conduct the off-state series switch transistor. Negative-body bias is used for insertion-loss reduction because the off-state series switch transistor is closer to open-state. At DC-6 GHz, the SPDT switch obtains excellent insertion loss of 0.4–1.4 dB, and isolation of 37.5–59.4 dB. At 28 GHz, the SPDT switch accomplishes insertion loss of 4.2 dB, isolation of 25.9 dB, and prominent IP_{1dB} of 25.6 dBm, one of the best IP_{1dB} results ever reported for mm-wave SPDT switches. The decent result of the wideband SPDT switch demonstrates its potential for sub-6 GHz and 28 GHz 5G communications.

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