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Power Sharing Control in a Grid-Tied DC Microgrid: Controller Hardware in the Loop Validation

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Citation: Samano-Ortega, V.; Rodríguez-Estrada, H.; Rodríguez-Segura, E.; Padilla-Medina, J.; Aguilera-Alvarez, J.; Martínez-Nolasco, J. Power Sharing Control in a Grid-Tied DC Microgrid: Controller Hardware in the Loop Validation. *Appl. Sci.* **2021**, *11*, 9295. <https://doi.org/10.3390/app11199295>

Academic Editors: Isabel María Moreno García, Rafael López Luque and Isabel Santiago Chiquero

Received: 9 August 2021

Accepted: 4 October 2021

Published: 7 October 2021

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Abstract: This article presents the development of a low-cost control hardware in the loop platform for the validation and analysis of controllers used for the management of power sharing between the main grid and a DC microgrid. The platform is made up of two parts: a main grid interconnection system emulator (MGISE) and a controller under test (CUT). The MGISE operates on a 260 V DC bus and includes a 1000 W photovoltaic array, a DC variable load and a single H full bridge converter (HFBC). The CUT includes a phase locked loop and a main cascade control structure composed of two PI controllers. Both the MGISE and the CUT were embedded on an NI myRIO-1900 development board and programmed using LabVIEW virtual instrumentation software. These devices communicate with each other using analog signals representing the AC side current, the DC side voltage, and the HFBC control signal. The MGISE operates with an integration time of 6 μ s and its performance is validated by comparing it with a simulation in PSIM. The integration time of the MGISE, the development boards used, as well as its programming environment, and the results obtained from the comparison with PSIM simulation, show that the proposed platform is useful for the validation of controllers for power sharing, with a simple implementation process compared to other hardware description methods and with a low-cost platform.

Keywords: controller hardware in the loop; grid-tied microgrid; h full bridge converter; microgrid

1. Introduction

In recent years, CO₂ emissions have increased significantly, and this has caused an increase in the average temperature of the planet and a threat to the health and well-being of humanity. This situation has raised awareness regarding the effects of global warming produced by CO₂ emissions, motivating research that evaluates the effect of energy consumption on climate change. Compared with fossil fuels, renewable energies (RE) facilitate a significant reduction in CO₂ emissions and consequently, the effects of climate change are reduced [1]. In response to this, electrical systems around the world have begun a transition following three trends known as the “three D’s”: Decentralization, Decarbonization and Democratization. Although the factors and details that guide the “three D’s” may differ from place to place, microgrids (μ Gs) have emerged as a flexible architecture for the deployment of distributed energy sources, including renewable generation (such as photovoltaic cells, small wind turbines, and mini hydro), which satisfy a wide range of needs [2].

According to their mode of operation, μ Gs can be categorized into isolated μ Gs (i- μ Gs) and grid-tied μ Gs (gt- μ Gs); i- μ Gs are mainly used in remote applications where

power supply through the MG is not feasible, while μ Gs operate both in islands and interconnected with the main grid (MG) [3]. The interconnection between the DC μ Gs and the MG is achieved using power electronic converters (PECs), so correct operation of the DC μ G depends largely on the adequate control of these converters [4]. Typically, the μ G control is made through a hierarchical scheme, including three levels: for locally measured power exchange, for voltage or frequency regulation and for optimal and economical global μ G operation [5]. This hierarchical structure allows multiple controllers' interoperability as well as several coupled elements through PECs such as those used in the μ G and MG power exchange [6].

The main function of this type of converter is the power sharing between the AC side and the DC side [7]. Therefore, this active and reactive power sharing plays an essential role in control algorithms of the interconnection converters [8]. Various studies have been published on power sharing control algorithms, and some of these are described below. In [9], a Linear Quadratic Regulator-Based Current Control is proposed for the management of power sharing between the AC and DC buses of a hybrid μ G. Study [10] proposes a predictive voltage model and a power control method to manage power sharing between a μ G and the MG. In [11], a nonlinear coordinated control strategy for parallel bidirectional power converters for a hybrid AC/DC μ G is proposed. In this topology, two bidirectional converters are used; one of them oversees transferring power between the AC side and the DC side. In [12], a droop control strategy is proposed for the control of a bidirectional AC/DC converter used for an electric airplane. Finally, study [13] discusses control techniques for current-controlled and voltage-controlled bidirectional converters in a hybrid AC/DC μ G.

In contrast, increasing advances in computer systems and the need to create different types of prototypes that simulate the behavior of physical systems in real time have led to the use of complex, sophisticated and expensive simulation tools. However, traditional simulation systems have the disadvantage of not recreating the actual operating conditions of physical systems. One option to solve this problem is to use the Hardware in the Loop (HIL) real-time simulation (RTS) technique, which reduces the gap between simulation and real conditions [14]. The development of physical systems on HIL platforms is carried out in various areas: For example, [15] proposes a novel HIL simulation configuration using the dSPACE SCALEXIO board with the aim of verifying the validity of an active control strategy of a conventional railway vehicle with a rigid axle set of wheels; this RTS has an integration time (IT) of 10 μ s. Conversely, [16] describes the details of an HIL platform (HILP) that uses the dSPACE RCP board for the implementation of an electromechanical system of an aircraft that allows evaluation of landing gear performance. Furthermore, in [17], the development of an HILP with an IT of between 1 and 2 ms is presented to perform analysis of the behavior of cyber-physical energy systems using the RT-LAB and OPNET software.

Several HIL commercial development platforms have been presented. These platforms offer HIL pre-configured system libraries in their programmatic environments, as well as specific HIL-focused hardware that features a communication layer. Nonetheless, these platforms are generally high cost, making them inaccessible for some researchers. In the search for the development of low-cost HIL platforms, [18] proposes a flexible platform for the simulation of embedded control strategies; in the validation stage of their proposal, they present two case studies: the first is an automotive application and the second a space application. In this proposal, an FPGA is not used because complex languages for description of hardware are required to make good use of resources from the devices. Instead, a computer with a DAQ-6703 data acquisition system was used as an interface; this HILP has a 200 μ s IT. In this same manner, [19] proposes a low-cost HILP, with an IT of between 1 and 1.5 μ s, for the simulation of electrical machines and their controllers. The implementation of the system is carried out on the Texas Instruments DSP TMS28379D board using C language; in this research, results were compared with commercial PSIM models. When working with platforms where the designer must embed their proposals, it

is necessary to choose appropriate methods for the design and implementation of HILPs. In [20], two methods are proposed for the implementation of HILPs; these methods seek to compare a system with the optimal resolution to have a performance comparable to the real system, and a second conservative method for resolution of the variables using the FPGA Xilinx XST0 development board (DB). An HILP was developed to validate these methods with an IT of 10 ns.

Working with HILPs presents a low-cost option that allows developers to test new prototypes by performing reliable experiments in a short time. One of the areas where HILPs are being used for the validation of various proposals is in power electronics, specifically in elements that make up the DC μ Gs. In [21], an experimental platform for wind turbines based on HIL was presented for the study of control structures. In [22], the MATLAB/XSG environment was used for the mathematical modeling of the aerodynamic and mechanical aspects of a real wind turbine. The Xilinx FPGA Virtex 5 LX50 T DB with an IT of 50 μ s was used, and rapid prototyping using MATLAB/Xilinx System Generation was performed.

Among the investigations carried out on DC μ Gs, there are applications that focus on the PECs that comprise them. In [23], an HIL simulation with an IT of 50 μ s was used to validate the proposal of a resonance mitigation controller used in series with a source voltage controller in a dual active bridge converter. To implement the system, an OPAL-RT simulator was used. A similar emulator was used in [24] to implement a DC μ G and test its proposed power management system; this application was developed with an IT of 1 ms. In [25], a modular development for the control of PECs was presented using a P-HIL platform, with an IT of between 9.44 and 15.72 μ s, based on a Xilinx Zynq-7000 development system. In [26], an HILP to test control algorithms was presented; this research focused on an energy administration technique. Furthermore, in [27], the design of an HILP, with a 100 μ s IT, of a multilevel converter that includes a control system test scheme based on the FPGA OP5607, was presented. Investigations in converters may include other aspects in addition to their electrical characteristics; for example, in [28], an electrothermal model of an interleaved boost converter was developed using an FPGA. The HILP was designed using a graphical programming environment in LabVIEW, embedding the system in the NI-7975R FlexRIO DB with an IT of 25 ns.

For the design and implementation of HILPs to emulate DC μ Gs, various DBs have been used. In [29], the Typhoon 602+ platform was used to emulate the behavior of a DC μ G with an IT of 1 μ s, while for the TMS32028335DSPC, Spartan 6XC6SLX16FPGA DBs were used to control the different converters, which operate with a modulation frequency of 10 kHz. These implementations were carried out to analyze the effect of the drivers on the transitions of the DC μ G converters. In [30], the same platform to emulate a DC μ G was used; this time, the objective was to measure the effectiveness of the proposed Adaptive Droop Control; the control systems are embedded in a Texas Instruments DSP DB. In contrast, in [31], a robust control strategy was presented to solve the stability problems caused by constant power loads in a DC μ G. To demonstrate the operation of the proposed controller, a simulation in MATLAB was compared with experimental results using an HILP implemented on the DSP (TMS320F28035) DB. National Instruments platforms have also been used. In [32], a DC μ G HILP was developed to validate the behavior of a DC bus voltage control system; in this design, the NI-PXIe-1078 DB was programmed with LabVIEW software. In [33], an HILP of a DC μ G using an RT-LAB and NI cRIO-9030 emulator was implemented; with this platform, the behavior of the system controllers, as well as their stability, were tested. In [34], an HILP was proposed, with an IT of 20 μ s, as a new method to develop and test control algorithms and operation strategies in DC μ Gs; this proposal uses RT-LAB (OP5600) for the implementation of the components of DC μ G and an NI cRIO-9025 DB for the control and administration of the DC μ G. In [35], the stability of the converters connected in parallel in a DC μ G is analyzed; for this, an HILP was developed with the RT-LAB software and an AD7606 data acquisition board. In [36], an OPAL-RT device was used to emulate the behavior of a DC μ G, presenting the

advantage of considering delays and errors; these considerations allow the characteristics of the fuzzy controller proposed in this research to be strengthened.

An HIL simulation is considered control hardware in the loop (C-HIL) when the power elements of a system are emulated in real time, while its controller, or part of it, is embedded in an external hardware device [37]. This technique allows experimentation with real controllers under a wide range of operating conditions without the risk of damaging real components [38] and has been used to validate controllers in PECs. In [39], work was carried out with an i- μ G, a C-HIL with an IT less than 1 μ s to validate the controllers applied to a photovoltaic system, and a storage system using batteries. In [40], a C-HIL platform to validate the control strategies applied to a multifunctional converter was developed. In this platform, the controller was emulated in a dSPACE with a 6 μ s IT. In [41], the C-HIL technique to validate different control strategies applied to a universal PQ compensator for low-voltage distribution networks was used. The HILP used had an IT of 15,625 μ s.

This article proposes the development of a C-HIL platform for the analysis of controllers aimed at managing the power sharing between a DC μ G, with a photovoltaic array (PA) as the main source of energy, and the MG, considered as first-level controllers in the μ G's hierarchical control structure. The proposed platform consists of two elements: a real-time emulator that reproduces the behavior of the main grid interconnection system (MGISE) and a controller under test (CUT) to validate the platform. The emulator includes a PA with a maximum power of 1000 W, a bidirectional AC/DC converter based on the H full bridge converter (HFBC) topology, and a load on the DC side; also this emulates the MG. The emulator operates with a 6 μ s IT. It has three analog outputs that represent the DC side voltage, the AC side current and the voltage signal of the MG; it also has an analog input that represents the control signal of the HFBC. The CUT, on the other hand, has two main parts: a phase-locked loop (PLL) type Park-PLL and a main control structure that includes two loops nested with PI controllers.

The proposed HILP allows for cascaded PI controller validation. This controller is simple and is effective for energy transfer management while having low computational costs during implementation. The results obtained with the proposed implemented C-HIL technique platform demonstrate its usefulness and that this platform could be an option for researchers, such as [7–13], to validate their controllers before an experimental prototype implementation. The HILP offers advantages during the validation process, in comparison with a software simulation, because of a test feature that allows the real time behavior of real hardware implemented controllers to be observed, obtaining the same results that would have been obtained with a real system and permitting observation of environmental variable changes as well, such as the behavior of the MG. In order to guarantee real time execution of the HILP, the hardware device's IT is the most important variable to take into account. The proposed HILP has an IT of 10 μ s; this time is enough to emulate real time continuous signals. In comparison with dedicated HIL platforms, the proposed HIL features low-cost hardware. It has a self-owned, high-level description environment, which facilitates and expedites platform development, and, in comparison with solutions such as those presented in [22], a tripartite software to embed the developed systems in the hardware is not required. All of these advantages together offer a useful and versatile HILP, built for power sharing controller analysis in μ Gs applications, with features such as low cost and benefits comparable to those of the commercial platforms.

The article is divided into five sections. Section 1 comprises the introduction. Section 2 presents a description, modeling and design of the elements that make up the main grid interconnection system (MGIS); the elements included in this section are HFBC, a PA and the controller proposed to validate the C-HIL platform. Section 3 describes the implementation of the systems in the NI myRIO-1900 (myRIO) DB and the conformation of the C-HIL platform interconnecting the emulator in real time that reproduces the behavior of the HFBC and the controller. Section 4 shows the results obtained with the C-HIL platform for a series of open loop and closed loop experiments, with the HFBC operating as a rectifier and inverter. The results obtained in this section are compared with results

obtained through software simulations in MATLAB and PSIM. Finally, Section 5 presents the discussion and conclusions related to the advantages that our proposal presents over some similar proposals reported in the literature.

2. MGIS: Description, Modeling, and Design

The topology used for the implementation of the MGIS shown in Figure 1 includes a single-phase HFBC made up of a power stage; switches Q_1 , Q_2 , Q_3 and Q_4 ; a capacitor C ; and an inductor L that has an associated resistance r . This topology is typical for the interconnection of distributed generation systems and μ Gs with the MG [42]. Additionally, the proposed topology includes a PA in the DC side, which represents the main source of energy that feeds the DC load, R . When the energy generated in the PA is greater than that consumed by the DC load, the rest of the energy is transferred to the MG. In the event that the energy generated by the PA is not enough to satisfy the demand of the DC load, the necessary energy is extracted from the MG. i_{pv} represents the electric current supplied by the PA; i_R is the current of the DC load R ; i_c is the current in the capacitor C ; v_{dc} is the DC bus voltage, which, in turn, represents the DC side voltage of the HFBC; i_{dc} is the DC side current of the HFBC; v_{ab} is the AC side voltage of the HFBC; i_a is the AC side power of the HFBC, which, in turn, corresponds to the electric current of inductor L ; and v_g , which corresponds to the voltage of the MG.

Figure 1. Main grid interconnection system topology.

The proposal is based on the design of a platform to evaluate the controller's operation used in power sharing between a μ G and the MG in a stage prior to its implementation in the field, eliminating the risk of damage to the real device. An isolation transformer is not contemplated in the proposed topology; however, it is recommended to include it in its physical implementation.

2.1. Photovoltaic Array Description and Modelling

For PA modeling, a Keysight E4360A photovoltaic panels emulator was used as a reference. As mentioned in [43–48], the device is used to substitute a real PA, presenting identical behavior. The emulator reproduces the characteristic current–voltage photovoltaic curve, based on parameters such as the open-circuit voltage V_{oc} ; the voltage and current in the maximum power point V_{mpp} and I_{mpp} , respectively; and the short-circuit current I_{sc} [49], while adding two extra variables (R_s and N), which are dependent on the four previously mentioned parameters. Equation (1) defines the relationship of the PA current I_p and its voltage V_p .

$$I_p = \frac{V_{p0}(I_p) - V_p}{R_p} \quad (1)$$

The terms $V_{p0}(I_p)$ and R_p are calculated according to Equations (2) and (3).

$$V_{p0}(I_p) = \frac{V_{oc} \left\{ V_{oc} \ln \left[2 - \left(\frac{I_p}{I_{sc}} \right)^N + \ln(2) R_s I_{sc} \right] \right\}}{\ln(2) [V_{oc} + R_s I_{sc}]} \quad (2)$$

$$R_p = \frac{V_{oc} R_s}{V_{oc} + R_s I_{sc}} \quad (3)$$

In contrast, Equations (2) and (3) depend on the variables R_s , a and N , which are a function of the input parameters (V_{oc} , V_{mpp} , I_{sc} and I_{mpp}), calculated with Equations (4)–(6).

$$R_s = \frac{V_{oc} - V_{mpp}}{I_{mpp}} \quad (4)$$

$$a = \frac{V_{mpp} \left(1 + \frac{R_s I_{sc}}{V_{oc}} \right) + R_s (I_{mpp} - I_{sc})}{V_{oc}} \quad (5)$$

$$N = \frac{\ln(2 - 2^a)}{\ln \left(\frac{I_{mpp}}{I_{sc}} \right)} \quad (6)$$

2.2. H Full Bridge Converter Description and Modeling

In order to propose the HFBC model, a sinusoidal type u modulating function is initially defined as described by Equation (7).

$$u = m \sin(\omega t + \alpha) \quad (7)$$

where m is the amplitude of the modulator, α is its phase angle with respect to the MG voltage, ω is its angular frequency defined as $\omega = 2\pi f$ and f defines the operating frequency of the HFBC, which is equal to the frequency of the MG. To generate the switching function of the power switches Q_1 , Q_2 , Q_3 and Q_4 , the sinusoidal pulse width modulation (SPWM) unipolar technique type was used [50]. The HFBC power circuit and the schematic SPWM modulator are shown in Figure 2.

Figure 2. Schematic SPWM modulator and the stage formed by the power devices.

Once the switching strategy has been defined, a simplified HFBC circuit is generated by replacing the two power switches on each branch with a single pole double throw (SPDT) switch. With this simplification, the power circuit of Figure 2 is reduced to the form shown in Figure 3, where $Q_1 - Q_2$ are replaced by SW_1 and $Q_3 - Q_4$ by SW_2 .

Figure 3. H full bridge converter simplified circuit using SPDT switches.

From the simplified representation of the power circuit shown in Figure 3, the dependence between the voltages and currents of the AC side and the DC side is obtained. Table 1 shows the possible combinations of the switching functions of the SPDT switches, and the values obtained for v_{ab} and i_{dc} in terms of v_{dc} and i_a . The variables q_1 and q_2 are the switching functions of SW_1 and SW_2 , respectively, and the variable q is defined as $q = (q_1 - q_2)$.

Table 1. Definition of the switching functions.

q_1	q_2	q	v_{ab}	i_{dc}
0	0	0	0	0
0	1	-1	$-v_{dc}$	$-i_a$
1	0	1	v_{dc}	i_a
1	1	0	0	0

The switching function q is equivalent to the sum of the modulating signal, u , and several high frequency components, due to the presence of the triangular signal in the modulator, which are neglected because the frequency of the triangular signal is much higher than the frequency of the modulating signal, so that $q = u$ [51]. From this equivalency and Table 1, expressions for v_{ab} and i_{dc} are obtained in terms of v_{dc} and i_a , as shown in Equations (8) and (9).

$$v_{ab} = uv_{dc} \quad (8)$$

$$i_{dc} = ui_a \quad (9)$$

With Equations (8) and (9), a new simplification of the power stage of the scheme presented in Figure 1 is generated, replacing the switches with dependent current and voltage sources, obtaining the simplified scheme of the MGIS as illustrated in Figure 4. By applying Kirchhoff's voltage law (KVL) in the loop that includes the inductor L , the expression presented in Equation (10) is obtained. Subsequently, when using Kirchhoff's current law (KCL) on the node that includes the capacitor C , the expression of Equation (11) is generated.

Figure 4. Representation of the switched model.

$$\frac{di_a}{dt} = \frac{1}{L} [uv_{dc} - i_a r - v_g] \quad (10)$$

$$\frac{dv_{dc}}{dt} = \frac{1}{C} \left[-ui_a - \frac{1}{R}v_{dc} + i_{PV} \right] \quad (11)$$

2.3. H Full Bridge Converter Design

The HFBC design requires the dimension of the passive elements. These are evaluated for maximum values of active power P , and reactive Q . To achieve the maximum symmetric compensation of active and reactive power to the DC bus voltage, a value twice the magnitude of the voltage for the MG V_g is given. Additionally, when the highest amount of power is shared, the amplitude of v_{ab} is equal to v_{dc} ; this implies, according to Equations (7) and (8), that $m = 1$. Applying these considerations, the coupling inductor is calculated with Equation (12) [52].

$$L = \frac{V_g^2 \sin(\alpha_1)}{\omega P_{max}} \quad (12)$$

where P_{max} is the maximum active power; α_1 is calculated with Equation (13), where Q_{max} is the maximum reactive power.

$$\alpha_1 = \arcsin\left(\frac{-P_{max}}{2\sqrt{Q_{max}^2 + P_{max}^2}}\right) - \arctan\left(\frac{-P_{max}}{Q_{max}}\right) \quad (13)$$

In contrast, the capacitor in the DC side is calculated with Equation (14), where Δv_{dc} is the ripple of the DC side voltage [52].

$$C = \frac{Q_{max}}{\omega \Delta v_{dc} V_g \sin\left(\arctan\left(\frac{Q_{max}}{P_{max}}\right)\right)} \quad (14)$$

2.4. Open Loop Main Grid Interconnection System Response

To validate the behavior of the MGIS, its responses were evaluated in open loop for the two operation modes: rectifier and inverter. To calculate the amplitude and phase of the modulating signal that determines the desired operating state, the AC loop presented in the diagram in Figure 4 is considered. For this validation, a value of zero was established for reactive power. This condition is desirable since it implies the state of operation with greater efficiency. Under this consideration, the HBFC AC side voltage is in phase with the AC side current so that its magnitude, V_{ab} , is determined with Equation (15) as a function of the instantaneous active power that is shared, P , and the magnitude of the AC side current, I_a .

$$V_{ab} = \frac{2P}{I_a} \quad (15)$$

With this condition, when applying the KVL to the AC loop in Figure 4, Equations (16) and (17) are obtained for the rectifier and inverter modes of operation, correspondingly. Two equations are generated from this loop, since, in the rectifier mode, the HFBC transfers energy from the MG and uses it in the DC side while, in the inverter mode, the energy generated by the PA that is not consumed in the DC load is injected into the MG. With this change in the direction of the energy flow, the direction of the AC side current changes, so the inductor voltage, $(r + j\omega L)I_a$, changes sign.

$$V_g = V_{ab} + (r + j\omega L)I_a \quad (16)$$

$$V_g = V_{ab} - (r + j\omega L)I_a \quad (17)$$

In Equations (16) and (17), the variables V_g , V_{ab} and I_a represent the phasors of the MG voltage, the AC side voltage and the AC side current, respectively. From these equations, the phasor diagrams shown in Figure 5 were generated.

Figure 5. H full bridge converter phasor diagram for both rectifier and inverter modes.

$M = I_a \sqrt{r^2 + \omega^2 L^2}$ is the magnitude of the inductor voltage phasor. From these phasor diagrams, the phase angle of the modulator, α , is obtained by calculating its tangent with the triangle ABC, as shown in Equation (18).

$$\alpha = \begin{cases} \text{atan}\left(\frac{\omega LI_a}{V_{ab} - rI_a}\right); & \text{for inverter mode} \\ \text{atan}\left(\frac{-\omega LI_a}{V_{ab} + rI_a}\right); & \text{for rectifier mode} \end{cases} \quad (18)$$

Nevertheless, to obtain the value of α , it is necessary to know the value of I_a . The magnitude of the sides $\overline{AD}$ and $\overline{DB}$ of triangle ABD depend on I_a , while $\overline{AB} = V_g$ is known. Thus, when applying the law of cosines to triangle ABD, with respect to angle γ , Equation (19), which depends on I_a , is generated.

$$V_g^2 = \frac{4P^2}{I_a^2} + I_a^2 (r^2 + \omega^2 L^2) - 4P \sqrt{r^2 + \omega^2 L^2} \cos(\gamma) \quad (19)$$

Substituting the variables $k = \sqrt{r^2 + \omega^2 L^2}$ and $x = I_a^2$ in Equation (19) and rearranging them, Equation (20) is obtained.

$$V_g^2 + 4Pk \cos(\gamma) = \frac{4P^2}{x} + xk^2 \quad (20)$$

Finally, substituting, $U = V_g^2 + 4Pk \cos(\gamma)$ and $xk^2 = k^2 \frac{x^2}{x}$, Equation (21) is generated.

$$k^2 x^2 - Ux + 4P^2 = 0 \quad (21)$$

By solving Equation (21), the value of I_a is obtained where the value of α is determined with Equations (15) and (18). The angle γ , on which Equation (21) depends, is a function of the operation mode and is calculated from triangle BCD in Figure 5, as shown in Equation (22).

$$\gamma = \begin{cases} \text{atan}\left(\frac{\omega L}{r}\right); & \text{for inverter mode} \\ \pi - \text{atan}\left(\frac{\omega L}{r}\right); & \text{for rectifier mode} \end{cases} \quad (22)$$

Finally, the magnitude of the modulator is determined from Equations (7) and (8), as shown in Equation (23).

$$m = \frac{V_{ab}}{v_{dc}} \quad (23)$$

2.5. Controller Description

The control scheme proposed to validate the work as a C-HIL platform is made up of two sections: (1) a PLL, which generates a sinusoidal signal in phase with the MG ($\hat{\theta} = \omega t$) and (2) the control structure, composed of two nested loops with PI controllers, whose output is the modulating signal u . The diagram of the implemented controller is shown in Figure 6.

Figure 6. H full bridge converter controller.

The PLL block of the controller in Figure 6 is type Park-PLL, which is based on the Park's transformation and is characterized by being robust, having a relatively fast transient response and a high rejection of disturbances [53]. The Park-PLL diagram is presented in Figure 7.

Figure 7. Park-PLL diagram.

In this structure, $\hat{\theta}$ is the approximation of the phase angle of the MG. The signals $v_g|_r$ and $v_g|_i$ are, respectively, the voltage of the MG and a signal that corresponds to this same voltage, with a phase shift of $\frac{\pi}{2}$ rad; this phase shift was generated using a quarter cycle delay. These signals constitute the rotating frame of reference of Park's transformation and are defined by Equations (24) and (25).

$$v_g|_r = V_g \sin(\theta) \quad (24)$$

$$v_g|_i = V_g \sin\left(\theta - \frac{\pi}{2}\right) = -V_g \cos(\theta) \quad (25)$$

where $\theta = \omega t$ is the phase angle of the MG voltage. In contrast, the signal v_q is defined from the Park transformation [54], as shown in Equation (26).

$$v_q = v_g|_r \cos(\hat{\theta}) + v_g|_i \sin(\hat{\theta}) = V_g \sin(\theta - \hat{\theta}) \quad (26)$$

The reference $v_q^* = 0$ implies that $\sin(\theta - \hat{\theta}) = 0$ for this to be true, and the difference between the angles must be zero, therefore, $\theta = \hat{\theta}$ when the system stabilizes.

3. HIL Implementation

Two myRIOs were used for the implementation of MGISE and CUT. Devices such as field programmable gate arrays (FPGAs) and digital signal processors are common in the development of real time emulators using generic low-cost hardware [55], and the myRIO integrates both technologies in a single board with a 40 MHz clock [56]. These platforms have differential high-impedance analog inputs, which allows them to be interconnected while maintaining an optimized common mode rejection ratio (CMRR) in balanced circuits. In addition, the parallel processing of the FPGA allows the rapid resolution of multiple

equations simultaneously with integration periods in the order of tens of microseconds. Ref. [57] uses a Xilinx Virtex 7 FPGA-based platform to validate the management system in a μ G by an HIL simulation and generates simulation steps between 200 ns and 2 μ s. In [58], a platform to emulate a photovoltaic system was implemented using a myRIO; this platform operates at a 1 ms integration time. Ref. [59] uses cRIO, FPGAs and a processor to emulate a μ G with simulation steps of around 5 μ s. Another advantage of this system is that its programming can be carried out using a high-level graphic language; this results in the development of applications more easily and quickly compared to other techniques [60]. The hardware description of the emulator proposed in this study was carried out using LabVIEW virtual instrumentation software. To achieve high performance, high throughput blocks with fixed point data types were used; these types of operation and data have a direct impact on the performance of the application, as well as on the use of hardware resources [61]. The proposed HILP implementation process is presented in this section. It is comprised of a real time emulator that reproduces the HFBC behavior, the controller, and their interconnection.

3.1. C-HIL Platform

The C-HIL platform proposed in this study is composed of two parts: the MGISE and the CUT. The MGISE emulates the behavior of the MG and the topology presented in Figure 1. For its implementation in hardware, this emulator was divided into two sections: the first is responsible for emulating the behavior of the PA (PAE) and the second emulates the HFBC (HFBCCE). Similarly, the CUT implementation was divided into two blocks: the PLL and the main control structure. The configuration of the proposed platform is presented in Figure 8.

Figure 8. C-HIL platform configuration.

The MGISE and CUT were implemented independently on one myRIO each. These two boards communicate with each other through analog signals; the signals v_g , v_{dc} and i_a , which represent the MG voltage, the DC side voltage and the AC side current, are sent from the MGISE board to the CUT board and this, in turn, feeds back to the MGISE with the control signal u . With this configuration, it is possible to validate different structures and algorithms for the CUT. The controller described in this study was implemented to test the structure and validity of the developed platform, but it does not imply that it is the only controller that can be analyzed with the developed platform. The implementation of each of the parts that make up the C-HIL platform is described in the following sections.

3.2. Photovoltaic Array Emulator Implementation

To implement the PA model presented in Equation (1), a one-dimensional LookUp Table (LUT-1D) was used. This technique is used in studies such as [62–64] for HIL implementations. The model of Equation (1) was solved in MATLAB's Simulink generating

1024 equidistant values, between 0 and V_{oc} , for V_p . The block diagram implemented for this purpose is shown in Figure 9. The values obtained for I_p were divided by I_{sc} , scaled and rounded, so that integers obtained were between 0 and 65,535, representing current values between 0 and I_{sc} . These values were then saved on a datasheet and assigned to the LUT-1D.

Figure 9. Block diagram used to generate the LUT-1D values.

For the implementation of the PAE, the voltage V_p was scaled with a factor $k_1 = \frac{1023}{V_{oc}}$ by means of a multiplication block. The output of this block was configured with a data type without a fractional part so that integer values between 0 and 1023 were obtained that represent the address of the LUT-1D. The output range of the LUT-1D is [0, 65535]; this range of values is scaled with a factor $k_2 = \frac{I_{sc}}{65535}$ by means of a multiplication block so that current values between 0 and I_{sc} were obtained at the output. Figure 10 shows the PAE implementation diagram.

Figure 10. Photovoltaic array emulator implementation.

3.3. H Full Bridge Converter Emulator Implementation

To embed the HFBC, the discrete model shown in Equations (27) and (28) was generated from Equations (10) and (11), where T is the period of the hardware device. Figure 11 shows the utilized schematic diagram for the implementation of the discrete model of the HFBC; this embedded system (ES) will act as the HFBC. The frequency of the MG, f , was established at 60 Hz and its amplitude at 180 V; a value of 0.4Ω was assigned to the resistance r , associated with the inductor; and a maximum active power level of 1200 W was defined. With these specifications and applying the calculations described in Section 2.3, L and C values of 4.1 mH and 4576 μ F were defined, respectively. This ES has the panel current I_p , the MG voltage v_g and the modulating signal u as inputs and as outputs of the DC side voltage v_{dc} and the AC side current i_a .

$$i_a(k) = \left(1 - \frac{rT}{L}\right) i_a(k-1) + \frac{uT}{L} v_{dc}(k-1) - \frac{T}{L} v_g(k-1) \quad (27)$$

$$v_{dc}(k) = \left(1 - \frac{T}{CR_L}\right) v_{dc}(k-1) - \frac{uT}{C} i_a(k-1) + \frac{T}{C} i_{PV}(k-1) \quad (28)$$

Figure 11. Implementation of the discrete H full bridge converter model.

3.4. Main Grid Interconnection System Emulator Implementation

For the implementation of MGISE, the ES presented in Figure 12 was developed. It integrates the ESs of the PAE and the HFBCE. The MGISE ES includes an analog input that represents the modulator signal u and two analog outputs that represent the variables v_{dc} and i_a . These input and output signals from the MGISE were used to interconnect with the CUT. The u signal takes values between -10 and 10 V, which, for this ES, represent values between -1 and 1 . The i_a signal, with voltage values between -10 and 10 V, represents a range between -256 and 256 A. Additionally, the v_{dc} signal, with values between 0 and 5 V, represents a range between 0 and 512 V for the ES. In addition, the MGISE ES includes two local variables that act as inputs; assigned as v_g and u , these two variables are the MG voltage and the modulating signal used for open loop tests. Additionally, the Boolean variables “Panel” and “Loop” determine the connection or disconnection of the panel and the operation of the MGISE in open loop and closed loop, correspondingly. The MGISE is performed with an integration time of $6 \mu\text{s}$; this time is the result of an iterative process in which, initially, an integration period and a data weight are defined (to represent the constants dependent on the period). Later, the time of the actual implementation of a cycle is measured and compared with the selected period; then, the period is reduced, the weight of the data is redefined and the real time is measured again. At a certain point, a reduction in time period implies an implementation of real time greater than the one proposed, so that there is a minimum period for which the real and defined times coincide [61]. This process was carried out for each of the ES presented in this section. Constants k_3 to k_5 were used to normalize analog signals.

Figure 12. Main grid interconnection system emulator implementation.

3.5. Open Loop

For the validation of the behavior of the MGISE in open loop, an ES was implemented that generates a modulating signal with variable amplitude m and phase angle φ . The amplitude and phase shift angle of the modulating signal are set by controls in this ES. In contrast, the MG voltage, v_g , is an emulated signal in the same while loop; in addition, this signal was connected to an analog signal that was compared with the signal generated with the PLL to verify its correct operation. The ES implemented for the emulation of these signals is shown in Figure 13. Constants k_6 to k_8 were used to normalize the analog signals.

Figure 13. Embedded system to emulate v_g and u signals.

3.6. Main Grid Interconnection System Emulator Real Time Processor

The ES of Sections 3.5 and 3.6 were implemented in the FPGA of a myRIO and this, in turn, was managed from the real time processor (RTP) of the myRIO. In the RTP, the variable $1 - \frac{T}{RC}$ of the discrete model of Equation (28) is defined. Additionally, through its control panel, the operator interacts with the MGISE. In this control panel, the operator has controls to define the variables R , of the HFBC model, “Panel” and “Loop”, described in Section 3.4, as well as the amplitude and phase angle of the modulation signal for open loop tests. In addition, indicators were employed to display the voltage on the DC side and the integration period of the FPGA.

3.7. Controller

To validate the MGISE as a platform for the development of the experimental stage on real controllers following the C-HIL technique, the controller described in Section 2.5 was embedded in a myRIO.

An essential element in the implementation of the controller is the action of the PI controller; this is because the structure of the control used has three of these controllers: one for the PLL and two for the main control structure. The discrete model of the PI controller defines the control action $u(k)$ in terms of the error $e(k)$, and the proportional, k_p , and integral, k_i , gains, as shown in Equation (29) [65].

$$u(k) = u(k-1) + k_p e(k) + (T k_i - k_p) e(k-1) \quad (29)$$

Figure 14 shows the ES block diagram to implement the model of Equation (29). The scheme presented in Figure 14 shows the PI controller of the PLL of Figure 7; however, similar diagrams were used for the inner loop and outer loop controllers of the control structure.

Figure 14. Block diagram for the implementation of the PI controller.

Another element that composes the PLL is the Park transformation. The programming employed to calculate the v_q component such as in Equation (26) is presented in Figure 15.

Figure 15. Block diagram for the implementation of the Park transformation.

The last block that composes the PLL is the integrator. For this element, if $x(k)$ is the result of the integration and $dx(k)$ is the variable which will be integrated, the model was proposed as shown in Equation (30). Additionally, the angle at the output of the integrator only takes values between 0 and 2. These values are interpreted in the $\sin(x)$ and $\cos(x)$ functional block of the structure shown in Figure 15, as if they took values between 0 and 2π . Figure 16 shows the schematic diagram to implement the integrator; in this diagram, the value of $T = 16.6 \mu s$. The block named “Select” is responsible for limiting the $x(k)$ output value between 0 and 2.

$$x(k) = x(k-1) + dx(k-1)T \quad (30)$$

Figure 16. Block diagram for implement the PLL integrator.

Figure 17 shows the implementation of the control structure. The presented controller in Figure 6 was implemented by using two loops. The first loop has a $16.65 \mu s$ execution time, allowing the loop to execute approximately 100 times for each MG period signal. In this loop, a PLL was implemented, joining Figure 14 to Figure 16 structures, the inner PI controller, the multiplication $u_1 * \sin(\hat{\theta})$ and the summing junction 2 (defined in Figure 6). This loop has analog input and output signals. The input signals represent the MG voltage and the AC side current and are received from the MGISE. The output signals are the control signal u , sent to the MGISE, and the value of $\sin(\hat{\theta})$; this signal is used to validate the PLL, comparing it with the MG voltage signal. The second loop includes an input (defined by the user in the PC) to define the DC side voltage reference (v_{dc}^*), the summing junction 1, the PI outer controller and the gain $\frac{2}{V_g}$ (defined in Figure 6); its input is the

voltage v_{dc} . This while loop has an execution time of 66.6 μ s. Constants k_9 to k_{13} were used to normalize the analog signals.

Figure 17. Control structure implementation.

4. Results

In order to validate the reliability of the MGISE, as well as its application and efficiency in the design of a C-HIL platform to analyze controllers that manage the power sharing between the MG and the PA, a set of experiments were carried out. The results of the responses from MGISE and the closed loop system were compared with simulations in PSIM and MATLAB. In Section 2.2, it is established that the HFBC operates with an SPWM modulating signal generated from a high-frequency surround system—that is, the real system is a commutated system; however, the MGISE was implemented by embedding the averaged model of the HFBC. When comparing the results obtained in the experimental stage with the results of the simulation in MATLAB, the software solution of the averaged model is compared, without restrictions on the type and weight of the data and with a continuous solution, with its hardware implementation, which is inherently restricted regarding the type and weight of the data and with a discrete solution. Thus, comparison of the MGISE with MATLAB only offers a measure of the fidelity between the embedded discrete system and a continuous system. Comparison of the results with the PSIM simulation has the purpose of contrasting the results obtained with the implementation of the C-HIL platform and results as close as possible to reality. In the PSIM, the system was simulated using an SPWM modulator signal, similar to how it would be carried out in a real setting (experimental prototype).

4.1. Photovoltaic Array

To analyze the different states of power sharing of the MGISE, a PA was used with a maximum power of 1000 W, a V_{oc} of 445 V, a V_{mp} of 360 V, an I_{sc} of 3 A and an I_{mp} of 2.78 A. The PAE's fidelity was verified by comparing the V-I characteristic curve obtained with the direct model of Equation (1) solved in MATLAB with the V-I characteristic curve obtained with the implementation of the LUT-1D, as presented in Figure 10. Figure 18 shows this

comparison: the red line corresponds to the characteristic curve V-I generated with the continuous model, while the green line is the characteristic curve generated by the PAE.

Figure 18. V-I characteristic curves of the direct model and the photovoltaic array emulator.

4.2. Open Loop Rectifier

For validation of the MGISE, an open loop experiment was performed operating in the rectifier mode. In this operating mode, it is assumed that the PA does not generate power, so the HFBC draws power from the MG to supply the DC load. In this experiment, a level of active power extracted from the MG, P , of 1200 W with a unity power factor was defined. The power consumed by the DC load depends on the voltage v_{dc} and the resistance value of R . The value of the DC bus voltage was established at 360 V, while the value of R was set at 110 Ω . With these values and applying the calculations described in Section 2.4, the modulation signal was defined with an amplitude of 0.48105 and a phase angle of -6.8346° . The frequency of the triangular signal f_c , in the case of the simulation in PSIM, was set at 9.6 kHz. Figure 19 shows the comparison between the results obtained from the simulations in MATLAB and PSIM, in addition to the results generated with the MGISE for the AC side current. The yellow line represents the response obtained in PSIM, the red line represents the results obtained in MATLAB, and finally, the green line represents the results generated with the MGISE. For this response, mean absolute errors of -0.26 A in regard to MATLAB and -0.27 A regarding PSIM were obtained. In contrast, Figure 20 shows the comparison between the results obtained in the simulation and the results obtained with the MGISE for the v_{dc} signal in the same experiment. For this variable, mean absolute errors of -1.47 V regarding MATLAB and -3.75 V regarding the PSIM were obtained.

Figure 19. i_a response under open loop and rectifier mode conditions.

Figure 20. v_{dc} response under open loop and rectifier mode conditions.

4.3. Open Loop Inverter

In this operation mode, the PA feeds the DC load with a DC voltage defined by the steady state response and the remaining energy is injected in the MG. With the aim of keeping the energy demanded by the DC load lower than the energy generated by the PA, the bus voltage was calculated at 360 V with a DC load of 2579 Ω . Under these conditions, the PA generates 1000 W, while the DC load consumes 50 W; the remaining 950 W are injected to the MG with a unit power factor. For this, the modulation signal was defined with an amplitude of 0.50953 and a phase angle of 5.103°. In Figure 21, the response of the AC current is presented, while, in Figure 22, the results obtained for the voltage v_{dc} in the same experiment are presented. The yellow line represents the data obtained on PSIM; the red line—the results obtained in MATLAB; and the green line—the results generated with the MGISE. In this experiment, mean absolute errors of -0.07 and -0.06 A for i_a were obtained with respect to MATLAB and PSIM. For the variable v_{dc} , mean absolute errors of -4.92 V and -3.13 V were obtained with respect to MATLAB and PSIM.

Figure 21. i_a response under open loop and inverter mode conditions.

Figure 22. v_{dc} response under open loop and inverter mode conditions.

4.4. PLL

To validate the results of the emulator with the PLL described in Section 2.5, the signal representing the MG voltage generated in the ES, shown in Figure 13, was compared with the signal $\sin(\hat{\theta})$ generated for the calculation of the Park transformation shown in Figure 15. In this comparison presented in Figure 23, the MG voltage is shown in red and the $\sin(\hat{\theta})$ signal of the Park transformation is shown in green.

Figure 23. Comparison between the MG voltage and the reference signal of the Park transformation.

4.5. Closed Loop Rectifier

To verify the behavior of the C-HIL platform operating in rectifier mode as presented in Figure 8, a DC load of 110Ω was selected with a reference of 360 V on the DC bus. Figure 24 shows the results obtained for the AC side current in the closed loop with the

MGISE operating in rectifier mode, while, in Figure 25, the behavior of voltage v_{dc} is shown. Finally, Figure 26 illustrates the results obtained for the active and reactive powers in this experiment. In Figures 24 and 25, the red line represents the response obtained in PSIM and the green line illustrates the results generated with the MGISE. In this experiment, regarding the PSIM, mean absolute errors of 0.3 A, -0.67 V, -10.79 W and -45.32 VAR were obtained for the variables i_a , v_{dc} , P and Q , correspondingly. In contrast, for the DC side voltage, an average value was obtained in steady state of 360 V. In Figure 26, the red line shows the results obtained for the active power in the PSIM simulation, the yellow line shows the reactive power obtained in PSIM, the green line shows the active power generated by the MGISE and the blue line shows the reactive power generated by MGISE. The values of these signals were calculated using a Park transformation. The negative value of the active power indicates that the energy was transferred from the AC side to the DC side.

Figure 24 shows the spectral analysis of the high-frequency current components. The components with the highest magnitude are as follows:

- Fundamental frequency (f): 60 Hz 13.85 Apk.
- Switching frequency (f_c): 9600 Hz 1.27 Apk, represents 9.22% of the fundamental peak value.
- High-frequency components: $f_c \pm 2f$: 9480 Hz / 9720 Hz 0.112 Apk, represents 0.8% of the fundamental peak value; $2f_c \pm f$: 19140 Hz / 19260 Hz 0.1811 Apk, represents 1.3% of the fundamental peak value.

The other components present an amplitude below 0.5% of the fundamental peak value.

Figure 24. i_a response under closed loop and rectifier mode conditions.

Figure 25. v_{dc} response under closed loop and rectifier mode conditions.

Figure 26. P and Q response under closed loop and rectifier mode conditions.

4.6. Closed Loop Inverter

In a similar way to the closed loop rectifier experiment, an experiment was carried out with the MGISE operating in inverter mode. For this experiment, the reference value of the DC bus voltage was 360 V, and the value of the DC load was 2579 Ω . Figure 27 shows the results obtained in this experiment for the AC side current, while, in Figure 28, the response obtained for the voltage v_{dc} is presented. Figure 29 shows the behavior of active power, while Figure 30 shows the results of reactive power. The values of this signal were obtained by means of the Park transformation. The positive value of these signals indicates that energy is transferred from the DC side to the AC side. In these figures, the lines in red represent the results obtained in PSIM and the lines in green the results generated by the MGISE. In this experiment, with respect to PSIM, mean absolute errors of -0.05 A, -0.81 V, 3.46 W and 115.89 VAR were obtained for the variables i_a , v_{dc} , P and Q , correspondingly. In contrast, for the DC side voltage, an average value was obtained in steady state of 359.92 V. Finally, Table 2 shows a summary of the mean absolute errors obtained for these responses.

Similar to the rectifier mode, the response of the spectral analysis of the current high-frequency components is shown in Figure 27. The components with the largest amplitude are as follows:

- Fundamental component (f): 60 Hz 10.00 Apk.
- Switching frequency (f_c): 9600 Hz 1.31 Apk, represents 13.1% of the fundamental frequency peak value.
- High-frequency components: $f_c \pm 2f$: 9480 Hz / 9720 Hz 0.1376 Apk, represents 1.37% of the fundamental frequency peak value; $2f_c \pm f$: 19140 Hz / 19260 Hz 0.17 Apk, represents 1.7% of the fundamental frequency peak value.

The other components present an amplitude below 0.64% of the fundamental frequency peak value.

Figure 27. i_a response under closed loop and inverter mode conditions.

Figure 28. v_{dc} response under closed loop and inverter mode conditions.

Figure 29. P response under closed loop and inverter mode conditions.

Figure 30. Q response under closed loop and inverter mode conditions.

Table 2. Mean absolute errors.

Operation Mode		Variable	Mean Absolute Error
Open loop rectifier	MATLAB	i_a	−0.26 A
		v_{dc}	−1.47 V
	PSIM	i_a	−0.27 A
		v_{dc}	−3.75 V
Open loop inverter	MATLAB	i_a	−0.07 A
		v_{dc}	−4.92 V
	PSIM	i_a	−0.06 A
		v_{dc}	−3.13 V
Closed loop rectifier		i_a	−0.3 A
		v_{dc}	−0.67 V
		P	−10.79 W
		Q	−45.32 VAR
Closed loop inverter		i_a	−0.05 A
		v_{dc}	−0.81 V
		P	3.46 W
		Q	115.89 VAR

5. Conclusions

Analysis of the MGISE response shows that the developed platform satisfactorily reproduces the behavior of the real system. This is verified by comparing the responses of the MGISE with the simulations. In the case of the variable i_a , in open loop, mean absolute errors of between −0.27 and −0.06 A were obtained. These errors represent a variation of between 0.58% and 1.94% with respect to the maximum and minimum values of this variable in the stable state, ranging from ± 10.28 A to ± 13.93 A, for the inverter and rectifier modes, respectively. Similarly, the errors obtained for the variable v_{dc} , in open loop, represent a variation of between 0.41% and 1.38% with respect to the average values that this variable reaches in stable state. In the case of closed loop experiments, the variable i_a presents variations between 0.44% and 1.96%, the variable v_{dc} presents variations between 0.19% and 0.22% and the variable P —between 0.4% and 0.88%; the average value of the variable Q in steady state oscillates the value of 0, so a relative error value was not calculated for it.

Given that the variation observed in the open loop is small, with a maximum error of 1.94%, it is concluded that the MGISE reproduces the behavior of the real system with acceptable fidelity. Conversely, even though the responses in closed loop differ to a greater extent compared to the responses in open loop, it is worth mentioning that the controller implemented in PSIM is a continuous controller, while the controller implemented for C-HIL platform validation is a discrete controller. Another important aspect is that in PSIM, both the controller and the MGIS operate simultaneously and synchronously, in the same simulation, so the PLL in PSIM will inherently present better results than in the embedded system. These two differences between the simulated controller in PSIM and the embedded controller influence the observed difference in the response of the controlled system. The HILP execution time is a feature to take into consideration in the difference between systems. A C-HIL simulation presents, generally, a time delay between acquisition and HILP signal generation, due to the hardware's propagation time. This time affects the total harmonic distortion, as discussed in [41]; nonetheless, the spectral analysis presented in the results section shows that the implemented platform integration time does not affect this variable significantly. In conclusion, the proposed platform demonstrates its usefulness in the validation of controllers for the management of power sharing between the MG and a DC μ G.

The IT of the proposed platform is 6 μ s; in the studies presented in Section 1, the ITs range between 10 ns and 2 ms, being more common order times of μ s. Of the 16 ITs

presented, 12 are in the range of 1 to 200 μ s. In this respect, the proposed platform presents an IT similar to those reported in the literature, being even lower than those reported in [15–18,22–25,27,34,41]. Of these studies, [17,23,24,27,34] use technologies destined for the development of HIL applications; they have their own programming environments, with functional blocks that represent the total dynamics of some elements and dedicated hardware. Therefore, the platform proposed in this study offers an IT similar to, and even less than, the ITs generated with dedicated platforms but at a lower cost. In [39–41], C-HIL platforms similar to the proposal are presented. In comparison with [41], the IT obtained in this work is smaller. The discussed works in [39–41] use a higher cost hardware in comparison with the DB used for the development of the HILP depicted in this paper. Conversely, the results obtained in [39–41] are valid even if they are not compared with a simulation or a real system, supporting the proposed viability for controller validation because of the comparison against a simulation, with satisfactory results.

With the proposed structure for the C-HIL platform and the methodology described for its implementation, it is possible to validate different controllers and algorithms under multiple operating conditions. With the proposed platform, it is possible, for example, to modify the characteristic V–I curve of the PA, to vary the frequency and amplitude of the MG and to modify the value of the DC load. With the MGISE of the independently embedded controller and a communication interface through analog signals between them, a change in the nature of the controller does not affect the constitution of the MGISE. Additionally, through the MGISE front panel, the user can modify the load on the DC side, select whether or not there is power generation in the PA, select between open loop and closed loop operation modes, as well as define the modulation signal for operations in open loop. Finally, the programming environment that was used makes it possible to reproduce and modify the proposed platform easily and quickly compared to the use of hardware description languages.

Author Contributions: Investigation, J.P.-M. and E.R.-S.; methodology, V.S.-O. and H.R.-E.; project administration, J.M.-N.; validation, J.A.-A. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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