# A Simple Two-Stage AC-AC Circuit Topology Employed as High-Frequency Controller for Domestic Induction Heating System 

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#### Abstract

The induction heating process at a domestic level is getting attention nowadays as this power converting topology ensures clean, reliable, flexible, and fast operation. The low input frequency is converted to required regulated high output frequency with indirect and direct power converting approaches. The circuit and control complexity and high conversion losses associated with indirect power converting approaches lower their uses for domestic induction systems. The direct ac-ac power conversion approach is one of the viable solutions for low and medium power level loads, especially for domestic induction heating loads. The circuit complexity, cost, and conversion losses of the direct power converting systems depend on the number of the controlled switching devices as each controlled switch requires one gate driving circuit and one isolated dc supply. Simplified pulse width modulation (PWM) switching control also lower their control effort. Therefore, in this article, a simplified direct ac-ac power converting approach is introduced for a high-frequency domestic induction heating system. Here, the regulation of the high output frequency is achieved by simply cascading the single-phase full-bridge rectifier with a full-bridge inverter with a simple control strategy. The characteristics of the developed topology are validated through simulation results of the Simulink-based platform and practical results of the developed practical setup.


Keywords: induction heating; controlled switching devices; gate driving circuit; full-bridge rectifier; full-bridge inverter; PWM switching control

## 1. Introduction

The widespread use of induction heating at a domestic level is due to its clean, reliable, fast, flexible, and highly efficient operation [1-4]. The popularity of this heating system is due to the development of high-frequency switching converters. These power converting circuits are extensively employed in induction heating systems and wireless power transfer systems. The wireless power transfer employed in autonomous vehicles for charging is normally induction-based. The other application that depends upon the induction phenomenon includes metal surface hardening, heat treatment, metal melting and electric ovens [5]. The generation of hot water for dishwashing, washing machine, and tea or coffee kettle is another use of induction heating process. Various fluid heating techniques are addressed in [6]. The conventional induction heating converters are realized in two
conversion stages. These techniques may include the thyristor-based rectification at the front end of the converting stages. The second stage may be a high-frequency voltage source or current source inverter for the generation of high-frequency outputs for induction purposes. The front-end rectifier circuit may be a PWM-controlled rectifier to improve the power quality of the first conversion stage. However, due to the use of bulky dc link inductor and capacitor, the power quality of the source current is poor, and the life cycle of the entire cycle is limited. These elements also increase the overall size, cost, and volume [7]. These power conversion approaches also have power quality concerns; therefore, their use is limited nowadays.

The other approach that tackles the drawback of a multistage converter is a matrix converter (direct ac-ac converter) that is implemented in a single power stage. The matrix converters may be realized as a three-phase to three-phase converter reported in [8] for dynamic voltage compensation between the two feeders of the power system. A three-phase to single-phase matrix converter is represented in [9,10]. In [9], an interface is developed between the three-phase system and single-phase distributed generator. The matrix converters for domestic level applications are single-phase to single-phase, as reported in [11-16]. In these single-phase matrix converters, the output voltage regulation is ensured through PWM control of high frequency-controlled devices. The output frequency regulation is obtained by controlling the turn-on and turn-off period of non-PWM-controlled switching devices. Input voltage sensing circuit is a mandatory requirement to detect the polarity of the input voltage. The control signals are non-symmetric, and their generation has to be aligned with the polarity of the input voltage. This would add unwanted delays, and the overall arrangement for the generation of the control signals becomes complicated. These types of matrix converters are not well suited for the application where only frequency regulation is required.

The problem of the complex control switching algorithm is effectively tackled in [17] by introducing the simple control scheme in which only two switching signals govern the overall circuit operation. Here the variable frequency at the output is insured by alternatively inverting and non-inverting the input voltage for both half cycles of the input voltage. This converter uses eight controlled switches and eight diodes, as can be seen in Figure 1. The emitter of each switching IGBT is connected to the anode of a diode. This connection arrangement of a transistor and diode simplifies the switching or control scheme. For example, four IGBTs $Q_{1}, Q_{4}, Q_{6}$, and $Q_{7}$, are turned on simultaneously with one control input. During positive input voltage, the turned-on IGBTs $Q_{4}$ and $Q_{7}$ cannot conduct as their series-connected diodes are reverse biased. In the same way, the turned-on IGBTs $Q_{1}$ and $Q_{6}$ remain off because their series-connected diodes maintain their reverse bias state once the input polarity is negative. The switching signal generated by a PWM controller is connected to an IGBT via a gate driving circuit. As there are eight IGBTs that are to be turned on and turned off, so the realization of this topology requires eight gate driving circuits. This overall impact increases the circuit size, cost, and complication. The reduction of two controlled switches (IGBTs or MOSFETs) and two diodes is ensured in [18] to simplify the circuit in terms of size and cost. Its realization only requires six diodes and six MOSFETs, as shown in Figure 2. This converter operates in a similar fashion as in [17] but with fewer solid-state devices. A center tap transformer-based direct ac-ac topology, as depicted in Figure 3, is introduced in [19]. Here a single-phase full-wave diode rectifier is connected at the output of the center tap transformer. Two fully controlled switching transistors are employed to realize the variable frequency at the output. There is a problem with the current shoot-through during the high-frequency operation. In addition, the use of the low-frequency center tap transformer has many power quality concerns that are reported in [20]. The large component count and solid-state devices are a big challenge in these converters.


Figure 1. Dual bridge direct ac-ac converter.


Figure 2. Direct frequency controller with reduced solid-state devices.


Figure 3. Direct frequency converter topology based on center tap transformer.
The use of large component count and solid-state devices is reduced in the proposed research. Here variable frequency at the output is ensured by cascading a single-phase
full-bridge diode rectifier and high-frequency full-bridge inverter by eliminating the dc-link capacitor at the intermediate stage. This elimination solves the problem of low reliability and reduces the size and cost. The output of the first stage is now a pulsating dc, meaning that the output is the absolute value of the input voltage. Then this output is converted to high-frequency ac with the help of a second-stage high-frequency inverter just by noninverting and inverting it. Therefore, with this circuit arrangement, only four diodes and four switching transistors ensure conversion of low input frequency to the high frequency at the output. There is no need to align the gating signal required for controlling the switching transistors with the input voltage, as the rectified voltage at the output of the first converting stage is a pulsating voltage, as there is no need to use a dc-link capacitor to smooth it. This feature enables the employment of any low-cost PWM generator like Arduino. The switching action of the transistors alternatively non-inverts and inverts the input at the output continuously to get variable output frequency. This characteristic improves the power quality and power factor of the input current. The use of a small inductor at the dc link level avoids the possible shoot-through issues of the switching transistors of the second stage inverter operated in a complementary fashion.

The arrangement of this article includes the basic circuit topology and its mode of operation in Section 2. Section 3 supports the topology's effectiveness through its comparison with the existing topologies implemented with a similar approach. Section 4 validates effective operation through the results obtained in the simulation-based platform and practically observed results obtained by developing a hardware setup. The conclusion is concluded in Section 5 of this research article.

## 2. Proposed Circuit Arrangement

The block diagram of the developed circuit arrangement is shown in Figure 4a. The role of the first stage full-wave diode rectifier is to convert the sinusoidal input (both positive and negative half-cycles) to absolute value at its output that may be mathematically formulated as:

$$
v_{o}(\omega t)=\left\{\begin{align*}
&+V_{m} \operatorname{Sin}(\omega t) 0 \leq \omega t \leq \pi  \tag{1}\\
&-V_{m} \operatorname{Sin}(\omega t) \pi \leq \omega t \leq 2 \pi
\end{align*}\right.
$$

The voltage at the upper terminal of the H-bridge inverter is always positive with respect to any polarity of the input voltage. This feature eliminates the use of a polarity sensing circuit of the input voltage. There is no need for the synchronization of the control inputs $s_{1}\left(s_{2}\right)$ and $s_{3}\left(s_{4}\right)$ with the input voltage. These control signals are the outputs of the four separate gate driving circuits. The input of each gate driving circuit may be generated with any low-cost digital or analog controller as they are generated without sensing the input voltage. Here two control signals $a_{1}$ and $a_{2}$ are generated with Arduino as a PWM generator. A small value inductor at the intermediate power converting stage eliminates possible shoot-through of the switching transistors operated in complementary mode. This requires a small overlapping interval in the two switching signals, as seen in Figure 4b, to avoid the current interruption issue due to the inherent mismatching of the switching transistor in both legs of the high-frequency H-bridge inverter. The two switching signals generated by the Arduino are complementary except for a small overlapping time ( $t_{o v}$ ) required to avoid the current interruption problem of the inductor. In this period, all switching transistors conduct. The total conduction period of any switching signal is $t_{p r,}$ and $t_{\text {con }}$ is the non-overlapping interval. The whole conduction interval is the sum of overlapping and non-overlapping intervals.

$$
\begin{equation*}
t_{p r}=t_{o v}+t_{c o n} \tag{2}
\end{equation*}
$$

Figure 5 illustrates the circuit arrangement of the proposed circuit. The input side of this circuit arrangement consists of four diodes employed to obtain pulsating dc from the sinusoidal ac input voltage $\left(v_{s}\right)$. The other side of this circuit arrangement is a full-wave H-bridge inverter consisting of four high-frequency switching transistors that convert the
low-frequency input voltage to high-frequency output voltage $\left(v_{o}\right)$. The rms values of the output voltage $\left(v_{0}\right)$ and input voltage $\left(v_{s}\right)$ are almost equal except for some voltage drops in the switching devices. Therefore, the rms value of the output current $\left(i_{0}\right)$ and input current $\left(i_{s}\right)$ are also the same. The detail of the operation of the proposed circuit is discussed with the help of its operating modes.


Figure 4. (a) Block diagram of the suggested converter topology; (b) gating signals.


Figure 5. Circuit arrangement of the proposed topology.
Mode of Operation: The discussion of operating modes of the suggested circuit is divided into its voltage non-inverting and inverting behavior for any polarity of the source voltage. Details are discussed below.

### 2.1. Non-Inverting Behavior

This mode explains the voltage in phase operation of the proposed topology by ensuring the phase difference between the output and input voltage is zero that is why it is treated as voltage in-phase operation. The detail of this operation is depicted and highlighted in power transfer loops of Figure $6 \mathrm{a}, \mathrm{b}$ for positive and negative input voltage, respectively. During the positive input voltage, the anode voltage of the diode $D_{1}$ is at a higher potential with respect to the anode voltage of the diode $D_{3}$. The diode $D_{1}$ conducts as the cathode voltage of $D_{1}$ and $D_{3}$ are equal because they are connected to the same point. In the same way, the anode of the diodes $D_{2}$ and $D_{4}$ are equal as they are connected to the same point. The cathode voltage of diode $D_{4}$ is positive, so it ensures the forward biasing of diode $D_{2}$ as it has low cathode potential. The turning on of the switching transistor $Q_{1}$ and $Q_{2}$ transfers the input power to output through the highlighted loop, as shown in Figure 6a. Here, the output voltage is in phase with the input voltage.


Figure 6. Power transfer loops for operation; ( $\mathbf{a}, \mathbf{b}$ ) voltage in phase; ( $\mathbf{c}, \mathbf{d}$ ) voltage out of phase.
In the same way, once the input voltage is negative, the anode voltage of diode $D_{3}$ and cathode voltage of $D_{2}$ is positive that ensures the forward biasing of the diodes $D_{3}$ and $D_{4}$. The highlighted power transfer loop of Figure 6 b in which the switching transistor $Q_{3}$ and $Q_{4}$ are on validates the negative output voltage or voltage in-phase operation. This behavior can also be validated by employing the concept of the volt-second product of the inductor.

The value of inductor voltage during the overlapping interval $\left(t_{o v}\right)$ and non-overlapping interval ( $t_{c o n}$ ) can be realized in Equations (3) and (4), respectively.

$$
\begin{gather*}
v_{L}(t)=v_{s}  \tag{3}\\
v_{L}(t)=\left(v_{s}-v_{0}\right) \tag{4}
\end{gather*}
$$

These values may be treated as constant as switching frequency is chosen much higher than the frequency of the input source. In a steady-state, the inductor current value at the start and end of the switching intervals becomes equal. Therefore, the average value of the inductor voltage in one switching interval should be zero that may be written as:

$$
\begin{gather*}
v_{s} \cdot t_{o v}+t_{c o n} \cdot\left(v_{s}-v_{o}\right)=0  \tag{5}\\
\frac{v_{0}}{v_{s}}=\frac{t_{o v}+t_{c o n}}{t_{c o n}} \simeq 1 \tag{6}
\end{gather*}
$$

This ensures the voltage in phase operation with either polarity of the input voltage, that is to say:

$$
\begin{equation*}
v_{o}(\omega t)=V_{m} \sin (\omega t) \tag{7}
\end{equation*}
$$

### 2.2. Inverting Behavior

In inverting mode of operation, the polarity of the output voltage is always apposite with respect to the polarity of the input voltage. It means that output voltage is always out of phase with respect to the input voltage. There is no change in the voltage at the output of the first converter either there is a non-inverting or inverting mode, this voltage always remains in pulsating dc form (absolute value of the input voltage). The behavior of the output voltage is governed by the switching scheme of the transistors of the second converting stage. For example, during the interval in which input voltage is positive, the turning on of the switching transistors $Q_{3}$ and $Q_{4}$ realized negative (inverting) output. It is demonstrated in the highlighted power transfer loop of Figure 6 c .

Similarly, the turning on of the switching transistors $Q_{1}$ and $Q_{2}$ is responsible for positive output once the input voltage is negative. The power transfer loop for inverting output during the negative input is highlighted in Figure 6d. Inverting output predicts the negative voltage gain that can be evaluated with the help of inductor voltage second product phenomena.

The value of inductor voltage during the overlapping interval is the same as computed for non-inverting operation.

$$
\begin{equation*}
v_{L}(t)=v_{s} \tag{8}
\end{equation*}
$$

However, the value of inductor voltage during the non-overlapping interval is larger as it is computed for non-inverting operation. Because in inverting mode, the inductor voltage is the sum of the input and output voltage as the output is always inverted with respect to the input.

$$
\begin{equation*}
v_{L}(t)=v_{s}+v_{0} \tag{9}
\end{equation*}
$$

The average value of the inductor voltage should be zero during any switching interval that may be formulated as:

$$
\begin{gather*}
v_{s} \cdot t_{o v}+t_{c o n} \cdot\left(v_{s}+v_{o}\right)=0  \tag{10}\\
\frac{v_{0}}{v_{s}}=-\frac{t_{o v}+t_{c o n}}{t_{c o n}} \simeq-1 \tag{11}
\end{gather*}
$$

This result validates the inverting operation for any polarity of the input voltage, as can be seen as:

$$
\begin{equation*}
v_{o}(\omega t)=-V_{m} \sin (\omega t) \tag{12}
\end{equation*}
$$

The summary of the operating modes (inverting and non-inverting) with either polarity of the input voltage is explored in Table 1 by detailing the operating states of all the solid-state devices employed in the proposed topology.

Table 1. Operating states of solid-state devices for output in-phase and output of phase operation.

| Non-Inverting Output |  |  |  |  |  |  |  | Inverting Output |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Positive Input Voltage |  |  |  | Negative Input Voltage |  |  |  | Positive Input Voltage |  |  |  | Negative Input Voltage |  |  |  |
| $Q_{1}$ | on | $D_{1}$ | on | $Q_{1}$ | off | $D_{1}$ | off | $Q_{1}$ | off | $D_{1}$ | on | $Q_{1}$ | on | $D_{1}$ | off |
| $Q_{2}$ | on | $\mathrm{D}_{2}$ | on | $Q_{2}$ | off | $D_{2}$ | off | $Q_{2}$ | off | $\mathrm{D}_{2}$ | on | $Q_{2}$ | on | $D_{2}$ | off |
| $Q_{3}$ | off | $D_{3}$ | off | $Q_{3}$ | on | $D_{3}$ | on | $Q_{3}$ | on | $D_{3}$ | off | $Q_{3}$ | off | $D_{3}$ | on |
|  | off | $\mathrm{D}_{4}$ | off | $Q_{4}$ | on | $D_{4}$ | on | $Q_{4}$ | on | $D_{4}$ | off | $Q_{4}$ | off | $D_{4}$ | on |

It can be observed that there is no change in the operating states of the diodes once the voltage at the output is changed from non-inverting to inverting and vice versa. However, the operating states of the transistor's pairs $Q_{1}-Q_{2}$ and $Q_{3}-Q_{4}$ are changed. For example, during positive input voltage, the switching transistors $Q_{1}-Q_{2}$ are on and off for noninverting and inverting operations, respectively. In addition, there is the conduction of two transistors and two diodes that realized the output in any desired operating mode (non-inverting or inverting).

## 3. Comparison with Existing Schemes

The attractive feature of the proposed circuit arrangement includes a reduction in the solid-state devices compared to the topologies realized with a similar approach. This reduction not only reduces the size and cost but also lowers the control and circuit complexity. Turning on and off of a switching transistor requires the use of a gate driving circuit and a separate isolated dc supply. A large number of devices and components are to be employed in the development of gate driving and dc supply circuit. Therefore, their size and cost are much larger than the cost and size of a switching transistor. The number of switching transistors employed in the suggested circuit is four, so only four gate driving circuits and four dc supplied are required. The switching transistors and diodes employed in [17] and [18] are eight and six, respectively. Therefore, there is a need for eight and six gate driving and dc supply circuits, respectively. The cost against reducing the switching transistors in [19] is paid with an additional bulky low-frequency center tap transformer. The current and voltage rating of all operating diodes and transistors in the proposed circuit and converter in [17-19] equals load rms voltage and load rms current. The power losses caused by the solid-state devices are switching, conduction, and leakage losses. The leakage losses are off-state losses that are normally ignorable as leakage current is negligible. The conduction losses of an operating transistor and diode in a high-frequency PWM interval ( $t_{s w}$ ) with output current ( $i_{o}$, diode forward voltage $\left(v_{f}\right)$, diode on resistor $\left(R_{f}\right)$, and transistor on resistors $\left(R_{t r}\right)$ are calculated in Equation (13) as realized in [21].

$$
\begin{gather*}
P_{c o n d}(t r)=\frac{1}{t_{s w}} \int_{0}^{t_{s w}} i_{o}^{2} R_{t r} d t  \tag{13}\\
P_{\text {cond }}(t r)=R_{t r} I_{o(\mathrm{rms})}^{2}  \tag{14}\\
P_{\text {cond }}(d)=\frac{1}{t_{s w}} \int_{0}^{t_{s w}} v_{f} i_{o}+i_{o}^{2} R_{f} d t  \tag{15}\\
P_{\text {cond }}(d)=v_{f} I_{o(a v g)}+R_{f} I_{o(\mathrm{rms})}^{2} \tag{16}
\end{gather*}
$$

The switching losses of a transistor depend on the switching frequency $\left(f_{s}\right)$, operating voltage $\left(V_{o}\right)$, operating current $\left(I_{o}\right)$, tun-on time $\left(t_{o n}\right)$, and turn-off time $\left(t_{o f f}\right)$. Here the operating voltage and current are considered quasi dc as the switching frequency is much
higher than the source frequency. The switching losses of a transistor are realized with a similar approach employed in [21].

$$
\begin{equation*}
P_{s w}(t r)=\frac{1}{2} V_{o} I_{o} f_{s}\left(t_{o n}+t_{o f f}\right) \tag{17}
\end{equation*}
$$

The switching losses of a diode are directly associated with reverse recovery transition. Therefore, they depend on the reverse recovery charge $\left(Q_{r r}\right)$ and are computed with a similar approach [21].

$$
\begin{equation*}
P_{s w}(d) \approx V_{o} f_{s} Q_{r r} \tag{18}
\end{equation*}
$$

The conduction of two transistors and two diodes in the proposed topology and converters in [17-19] helps realize the operation in any operating mode. Therefore, the total conduction losses of two transistors and two diodes in one PWM switching transition are realized as:

$$
\begin{equation*}
P_{c o n d}=2 v_{f} I_{o(a v g)}+2 I_{o(\mathrm{rms})}^{2}\left(R_{f}+R_{t r}\right) \tag{19}
\end{equation*}
$$

The switching losses of the two transistors and diodes of converters reported in [17-19] are computed as:

$$
\begin{equation*}
P_{s w([17-19])}=V_{o} I_{o} f_{s}\left(t_{o n}+t_{o f f}\right)+2 f_{s} V_{o} Q_{r r} \tag{20}
\end{equation*}
$$

The switching losses of diodes of the proposed topology are negligible as they operate in low frequency (input frequency), so here switching losses only come from switching transistors and are computed as:

$$
\begin{equation*}
P_{s w(\text { Proposed })}=V_{o} I_{o} f_{s}\left(t_{o n}+t_{o f f}\right) \tag{21}
\end{equation*}
$$

In summary, the comparison of the suggested circuit with the existing circuits is given in Table 2.

Table 2. Comparative analysis of the suggested and the recently-developed topologies.

| Number of Components or Devices | Proposed Topology | Topology in [17] | Topology in [18] | Topology in [19] |
| :---: | :---: | :---: | :---: | :---: |
| Transistors | 4 | 8 | 6 | 2 |
| Diodes | 4 | 8 | 6 | 4 |
| Driving circuits | 4 | 8 | 6 | 2 |
| DC supplies | 4 | 8 | 6 | 2 |
| Voltage sensing circuits | 0 | 1 | 0 | 0 |
| Center tap transformer | 0 | 0 | 0 | 1 |
| Shoot-through issue | No | No | No | Yes |
| Output voltage gain | Bipolar | Bipolar | Bipolar | Bipolar |
| RMS voltage rating of the diodes and transistors | $V_{o}$ | $V_{0}$ | $V_{0}$ | $V_{0}$ |
| RMS current rating of the diodes and transistors | $I_{o}$ | $I_{o}$ | $I_{o}$ | $I_{0}$ |
| Conduction losses | $\begin{gathered} 2 v_{f} I_{o(a v g)}+ \\ 2 I_{o(r m s)}^{2}\left(R_{f}+R_{t r}\right) \end{gathered}$ | $\begin{gathered} 2 v_{f} I_{o(a v g)}+ \\ 2 I_{o(r m s)}^{2}\left(R_{f}+R_{t r}\right) \end{gathered}$ | $\begin{gathered} 2 v_{f} I_{o(a v g)}+ \\ 2 I_{o(r m s)}^{2}\left(R_{f}+R_{t r}\right) \end{gathered}$ | $\begin{gathered} 2 v_{f} I_{o(a v g)}+ \\ 2 I_{o(r m s)}^{2}\left(R_{f}+R_{t r}\right) \end{gathered}$ |
| Switching losses | $V_{o} I_{o} f_{s}\left(t_{o n}+t_{o f f}\right)$ | $\begin{gathered} V_{o} I_{o} f_{s}\left(t_{o n}+t_{o f f}\right) \\ +2 f_{s} V_{o} Q_{r r} \end{gathered}$ | $\begin{gathered} V_{o} I_{o} f_{s}\left(t_{o n}+t_{o f f}\right) \\ +2 f_{s} V_{o} Q_{r r} \end{gathered}$ | $\begin{gathered} V_{o} I_{o} f_{s}\left(t_{o n}+t_{o f f}\right) \\ \quad+2 f_{s} V_{o} Q_{r r} \end{gathered}$ |

This comparison validates the effectiveness of the proposed circuit topology as it requires fewer switching transistors, gate driving circuits, isolated dc supplies, and simple control schemes.

## 4. Validation of the Suggested Circuit

The effectiveness and validity of the proposed circuit topology are verified through the result obtained in the Simulink-based platform and practically obtained results by developing a test circuit.

### 4.1. Results Obtained with Simulink Based Environment

MATLAB/Simulink is one of the modern power tools employed for the analysis of the switching converter. That is why this platform is selected for simulation purposes. In this analysis, the peak value of the input voltage is taken as 150 V with an input frequency of 50 Hz . The load impedance value is $80 \Omega$, and the switching frequency for high-frequency transistors is selected at 25 kHz . The internal resistances of the switching transistor and diode are set to $0.08 \Omega$ and $0.006 \Omega$, respectively. The forward voltage of the diodes is assumed to be 1 V . A small value inductor of $500 \mu \mathrm{H}$ is inserted between the two converting blocks to avoid the possible shoot-through concern that may arise due to the inherent turn-off delay of the switching transistors operated in a complementary way. In summary, these parameters are also represented in Table 3.

Table 3. Parameters employed for simulation results.

| Parameter | Value |
| :---: | :---: |
| Input peak voltage | 150 V |
| Input frequency | 50 Hz |
| Internal resistance of transistor | $80 \mathrm{~m} \Omega$ |
| Internal resistance of diode | $6 \mathrm{~m} \Omega$ |
| Forward voltage of diode | 1 V |
| Series inductance | $500 \mu \mathrm{H}$ |
| Load impedance | $80 \Omega$ |
| Switching frequency | 25 kHz |

According to the control scheme as depicted in Figure 4, one signal controls the operating states of the two transistors, and the second switching signal that is in complementary form of the first signal controls the operating states of the other two transistors. These switching signals govern the operating states of the transistors in such a way that if the conduction of two transistors non-invert the input at the output, then the conduction of the other two transistors inverts the input voltage at the output as shown in Figure 7a. It depicts that the input voltage at the output is alternatively non-inverted and inverted during the positive and negative half cycles of the input voltage. The frequency at which output is changed from non-inverting state to inverting state and vice versa depend upon the switching frequency of the operating transistors. This sort of output and the corresponding load current is demonstrated in Figure 7b,d, respectively.

On the other hand, the input current is almost continuous, as shown in Figure 7c, because it is conducted through two transistors and two diodes in all operating modes. This characteristic of the input current depicts the improved power quality that may be evaluated in terms of power factor, harmonic factor, and total demand factor. The determination of the power quality concern of the input current is carried out in Simulink based environment by taking its FFT as shown in Figure 8. It can be observed that low distortion of the input current results in a high value of its fundamental component compared to the harmonics or unwanted components. The power factor can be approximated directly from the harmonic factor as the distortion level of the input voltage is negligible. In the proposed circuit topology, a $1 \mu \mathrm{~F}$ capacitor is connected across the input source to tackle the unwanted distortion in the input voltage that may be caused by the utility power quality problem or some switching harmonics that may be generated due to high switching
operation of the switching transistors. The following mathematical form explores the effect on the power factor with respect to the variation in the harmonic factor of the input current.

$$
\begin{equation*}
p \cdot f=\sqrt{\frac{1}{1+H F_{\text {current }}^{2}}}=0.99 \text { lag } \tag{22}
\end{equation*}
$$



Figure 7. Simulated waveforms: (a) input voltage $\left(v_{s}\right) ;(\mathbf{b})$ output voltage $\left(v_{o}\right) ;(\mathbf{c})$ input current $\left(i_{s}\right) ;(\mathbf{d})$ output current $\left(i_{o}\right)$.


Figure 8. Validation for power quality of the input current.
It can be observed that the true power factor is approximately unity as there is a very low harmonic factor $(0.82 \%)$ of the input current.

### 4.2. Results Obtained with Practical Setup

The validation of simulation results requires practical values or results that are obtained by developing a practical setup as shown in Figure 9. This realization of the front stage bridge rectifier circuit is ensured by using four diodes (RHRG3040) that have abrupt reverse recovery characteristics. They are employed to lower the switching losses as their reverse recovery charge or time very is low. The high-frequency H-bridge inverter is constructed with four high switching frequency transistors (IRF840). Their voltage and current rating are almost 500 V and 5 A , respectively. Four gate driving circuits are realized with gate driving chips (EXB840) and four isolated dc supplies. An input capacitor of $1 \mu \mathrm{~F}$ filters any abrupt variation in the incoming input voltage. An inductor of $500 \mu \mathrm{H}$ is employed at the intermediate stage to tackle the problem of possible shoot-through that may arise due to the switching action of the complementary operated switching transistors. Arduino controller is employed as a PWM generator, and the generated control signals need not to synchronize with the polarity of the input voltage. Therefore, a few lines of code generate these control signals.


Figure 9. Practical setup.
In summary, solid-state devices and passive components employed in practical setup are also represented Table 4.

Table 4. Design parameters and components employed for real results.

| Device/Component Name | Number/Value |
| :---: | :---: |
| Diode | RHRG3040 |
| Transistor | IRF840 |
| Gate driver | EXB840 |
| Input capacitance | $1 \mu \mathrm{~F}$ |
| Series inductance | $500 \mu \mathrm{H}$ |
| Load impedance | $80 \Omega$ |
| Switching frequency | 25 kHz |
| Arduino | UNO |

The main target of this developed laboratory prototype is to confirm the power quality concern of the input current and generation of high-frequency output voltage. These results
or targets are ensured by setting the switching frequency for switching transistors to 25 kHz with a $50 \%$ duty cycle. This duty cycle ensures that output is non-inverted and inverted alternatively for $50 \%$ of the switching interval with any polarity of the input voltage as can be viewed from Figure 10a. The output current also follows a similar behavior that can be viewed in Figure 10b with the reference of output voltage. Figure 10c shows the output voltage and output current in a magnified form around the peak value of the input voltage. Here it can be observed that for the switching period of $40 \mu \mathrm{~s}$, the output is positive for $20 \mu \mathrm{~s}$, and then it is negative for $20 \mu \mathrm{~s}$ interval. The current conduction path of the input current is always non-interrupted, so the input current is continuous with low distortion, as can be viewed from Figure 10d. Here input current is being represented in the red color waveform with respect to the input voltage (blue color waveform). This depicts the improved power quality of the input current.


Figure 10. Practically recorded waveforms: (a) output voltage; (b) output voltage (blue) and output current (red); (c) output voltage (blue) and output current (red) in magnified form; (d) input voltage (blue) and input current (red).

## 5. Conclusions

The proposed circuit topology for a high-frequency induction heating system reduces the cost, overall size, and circuit complexity by reducing the number of solid-state switching devices. The suggested topology is realized with cascading of full-bridge diode rectifier circuit and full-wave H -bride inverter. The first stage rectifier converts the ac input voltage into its absolute value, while the second stage inverter converts it into high-frequency ac voltage. Therefore, the proposed circuit topology only requires four diodes and four transistors less than the existing topologies implemented with a similar principle. The reduction in switching transistors also lowers the use of many gate driving circuits. The overall impact of reducing solid-state switching devices and gate driving circuits is the reduction in overall size and circuit cost. There is no requirement to synchronize the gating
signals with an ac input voltage that lowers the control effort of the PWM generator. As only two control signals are required for the realization of the overall operation so a simple control scheme can be generated with any low-cost PWM controller. The validation of the suggested circuit is carried out by simulating this topology in Simulink based platform and through the practical results obtained by developing a practical prototype.

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