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Integrated Electromagnetic-Thermal Approach to Simulate a GaN-Based Monolithic Half-Bridge for Automotive DC-DC Converter

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Abstract: New technological and packaging solutions are more and more being employed for power semiconductor switches in an automotive environment, especially the SiC- and GaN-based ones. In this framework, new front-end and back-end solutions have been developed, and many more are in the design stage. New and more integrated power devices are useful to guarantee the performances in electric vehicles, in terms of thermal management, size reduction, and low power losses. In this paper, a GaN-based system in package solution is simulated to assess the structure temperature submitted to a Joule heating power loss. The monolithic package solution involves a half-bridge topology, as well as a driver logic. A novel integrated electromagnetic and thermal method, based on finite element simulations, is proposed in this work. More specifically, dynamic electric power losses of the copper interconnections are computed in the first simulation stage, by an electromagnetic model. In the second stage, the obtained losses' geometrical map is imported in the finite element thermal simulation, and it is considered as the input. Hence, the temperature distribution of the package's copper traces is computed. The simulation model verifies the proper design of copper traces. The obtained temperature swing avoids any thermal-related reliability bottleneck.

Keywords: automotive; gallium nitride; power devices; integrated package; finite element simulation; electromagnetic simulation; thermal simulation; half-bridge

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1. Introduction

Power Electronics plays a key role in emerging technologies that require any possible electrical power conversion, from DC to AC or vice versa, or to change the voltage level in electronics equipment. Hence, in the automotive field, hybrid and full-electric vehicles power electronics are massively employed. However, converters and power devices must withstand more stringent requirements, in terms of performance and reliability, especially in harsh environments [1,2].

Wide band-gap (WBG) materials, such as gallium nitride (GaN) and silicon carbide (SiC) [3], are those which can satisfy the application's requirements [4,5]. SiC and GaN-based devices are being more and more employed in converters for the automotive environment [6–19] thanks to their superior electrical and thermal performances in comparison to that of silicon (Si). SiC devices are more indicated for high-voltage and high-power, while GaN-based ones are more prone to low- and medium-power high-frequency applications with low and medium voltages. High-efficiency converters are possible, when GaN devices are employed, which have higher breakdown electric field and low on-state resistance. Some possible GaN structures are reported in [7]. Nowadays, ultra-wide-bandgap materials such as gallium oxide (Ga₂O₃) [8–10], diamond, and aluminium nitride (AlN), have also been gaining attention in the power electronics field, even if at a more infant stage. A review of Ga₂O₃-based power MOSFETs can be found in [11].

GaN-based power devices are intrinsically normally-on: they have a 2DEG channel as the conduction zone [12,17]. However, this can be a problem, especially for safety reasons in real-world applications. Therefore, in most cases, a normally-off device is constructed by means of various techniques. In the GaN framework, there exist both radio-frequency and power devices: the latter will be the object of this work. High electron mobility transistors (HEMTs) are currently being employed on the market. From a physics point of view, GaN-on-Si technology, that is, with GaN on a silicon substrate, is today industrially mature [18]. Another important feature of GaN HEMT devices is the absence of the body diode; however, they can conduct in both directions, and reverse recovery losses are not present [20]. The physical characteristics of GaN-based switches are far from the topics discussed in this paper; however, the structure of a typical lateral GaN device is showed in Figure 1 [21]. With reference to the voltage classes, in the context of power devices, both high voltage (HV, until 650 V) and low-voltage (LV, under 100 V) switches do exist today.

Figure 1. GaN-on-Si power device lateral structure. Image from [21].

Miniaturization can be possible because there is a low contribution in parasitic elements, such as intrinsic device capacitances, that results in lower heating, and, as a consequence, a smaller die and occupied area by the package. This also results in low power losses. In the GaN framework, new LV and HV power devices are important, among the others, for the following applications: DC-DC converters, onboard chargers, adapters, wireless charging, class D amplifiers, flyback SMPS, boost converters, and LiDAR [22]. In Figure 2, the possible applications of Si, SiC, and GaN devices, in terms of output power and operating frequency, are depicted [23]. For LV applications, GaN devices are commonly employed in monolithic packages, because they dissipate lower switching and conduction losses.

Figure 2. Application framework, based on output power and operating frequency, for Si-based IGBTs and MOSFETs, and SiC- and GaN-based power devices. Image from [23].

The principal challenges currently present in the design and application of GaN-based power devices mainly rely on thermal management [24], parasitic contributions with high switching frequency (high dv/dt and di/dt slew rates coupled with parasitic elements) [25], reliability [26], and dynamic on-state resistance. The last topic is the increase in drain-source resistance, as a consequence of trapping phenomena during the transition between off and on states [27–30]. A parametric analysis of the impact of parameters, such as off voltage and time, frequency, current, and temperature, based on the available literature, is presented in [31]. High-frequency operation would reduce the passive components requirements; however, the interaction between parasitic inductances and capacitances, and dv/dt and di/dt , can produce more losses [32], switching oscillations [33,34], and false turn on [35]. Related to this issue, there exists a more general topic regarding the power losses, in terms of both models and experimental methodologies [36–39]. Moreover, the hysteretic losses related to the output capacitance must also be taken into account, especially in soft-switching applications (i.e., where there is not a hard intersection between the drain-source voltage and drain current at the transient stage) [40].

From the back-end side [41], integrated packaging solutions for WBG-based devices are gaining attention [42–44], because they can furtherly reduce the occupied area and, as a consequence, the power density. Nevertheless, the package integrity must be assured, also from a structural point of view [45]. In this paper, a system in package (SiP) GaN-based power device is considered [22]. In general, monolithic integration solutions usually comprise half- or full-bridge topologies, the driver, the protection, and the control logic [46].

GaN-based power switches are usually surface-mounted devices (SMDs), i.e., they are directly soldered on the printed circuit board (PCB). Regarding the cooling, traditionally, the SMDs have been bottom-side cooled. There exist, in this case, several solutions to cool the device in the application, among them: PCB thermal vias, copper pads beneath the device, heatsink (if present) attached to the PCB bottom. Nowadays, double side cooled power SMDs are spreading. They have the exposed pad on the top of the package. In such a way, this solution is more advantageous because the heatsink can be directly attached to the top of the package, thus ensuring a more pronounced heat exchange. Then, also another heatsink would be present on the bottom side of the PCB. Regardless of the cooling systems used on the package and at the applications level, the heat removal from the GaN power device is critical, either for the die and for copper traces dissipation inside the package [24,47–49].

Numerical simulations are today commonly used in industry frameworks, also in order to validate various design proposals, without spending time and cost on releasing many prototypes. These techniques are nowadays also widespread for power electronics [50,51].

However, to the best of our knowledge, an integrated simulation approach, using finite element model (FEM)-based software packages, starting from electromagnetic output to calculate the temperature of interconnects, has not been proposed for power devices. The aim of the study is to calculate the copper traces temperature, induced by package electromagnetic self-heating by means of an integrated simulation. This approach is made by electromagnetic and thermal FEM. The electromagnetic FEM calculates the spatial distribution of power losses due to a dynamic current input at 500 kHz. The power losses geometrical output map is indeed exported in the post-process of electromagnetic FEM and imported in the pre-process of thermal FEM. The copper traces temperature is finally calculated considering the imported power losses' map as simulation input. This can be possible if an integration among the two physical environments is accomplished. The test vehicle considered in the paper is a GaN-based 2SPAK SiP, from STMicroelectronics. The rest of the paper is organized as follows: in the following section, the integrated simulation methodology is outlined, while in Sections 3 and 4, respectively, the electromagnetic and thermal simulation setups and results are shown and discussed. In the end, some conclusions are drawn.

2. Package Description and Integrated Simulation Methodology

2.1. Integrated GaN Package Description

A brief outline of the innovative package will be made in the following [46,52]. As it was stated in Section 1, these solutions are becoming increasingly used in industry, for Si- and WBG-based power devices [43,53–58]. The SiP solution, from STMicroelectronics, presented in this paper has a 100 V breakdown voltage, and it is used in a 48 V–12 V DC-DC converter application. The package has been named 2SPAK and comprises a half-bridge and the control logic. It allows, if the layout design is carefully addressed, a more compact solution, reducing the contribution of parasitic elements. In this case, vias connect GaN metals directly to the pads, reducing parasitic contribution and improving the thermal performance [52]. In addition, the PCB must also be designed in order to minimize parasitic elements, again, for EMI issues [59]. 2SPAK permits a bulk capacitor position, in PCB, a reduction of length interconnections [52]. In general, oscillations and overshoots must be minimized [60].

The package analyzed in this work is a bond-wire free one in order to improve thermal performances and reduce parasitic losses. It has an exposed slug on the top. Therefore, top side cooling helps the heat exchange, thereby making it possible to lower the system's thermal resistance or reducing the heatsink size.

2.2. Simulation Methodology Outline

In this section, a description of the method proposed in this work is given. FEM-based tools are used for both the steps considered in the analysis.

In the first phase, the computer-aided design (CAD) package geometry is used to make an electromagnetic finite element simulation using Ansys Q3D, thereby obtaining the current and voltage maps, and the output power map, as will be explained in more detail in Section 3. The last map represents the losses due to the Joule heating phenomenon in copper traces. It is the link between electromagnetic and thermal simulation due to the fact that such a geometrical map represents the output of electromagnetic FEM and the input of thermal FEM employed with COMSOL Multiphysics. Then, the same geometry is employed to thermally simulate the system, by imposing appropriate thermal boundary conditions, i.e., the power losses' geometrical map and as discussed in-depth in Section 4. In Figure 3, a scheme of the proposed flow is depicted.

Figure 3. Workflow of the proposed method.

3. Electromagnetic Simulation

The used software for the electromagnetic simulation is Q3D Extractor, from Ansys, designed for those calculation types. In particular, by using this tool, it is possible to compute the current and voltage inside the package, as well as the parasitic resistive and

inductive contributions at the chosen frequency. More specifically, Q3D Extractor allows to find out the equivalent resistance, inductance, capacitance and conductance network of a specific electronics product, that can be then exported to a like-SPICE environment. This software usually supports the design of electronics packages and connectors, thus permitting optimizing the electric performances [61].

3.1. Q3D Extractor Theory

Q3D Extractor solver considers the quasi-static approximations for Maxwell's equations. It can be assumed that when one of the first-order time derivatives of electric and magnetic induction fields (but not both) is different from zero, the other one is negligible. The main consequence of this technique is that electromagnetic signals cannot propagate and the scalar fields at time t in a certain point P are only dependent on the electromagnetic sources' values at time t . This formulation can be used if it is established that the system length is much smaller in comparison to the wavelength associated with the maximum operating switching frequency of the power device. A general indication is that the structure dimension should be less than 1/10 of a wavelength that is inversely proportional to frequency. Considering that the simulations are carried out at a frequency f equal to 500 kHz and assuming c equal to the speed of the light in vacuum, the wavelength $\lambda = \frac{c}{f} \cong 0.6$ km is higher (much more than 10 times) than the maximum package dimension (approximately 10 mm), confirming the validity of the quasi-static hypothesis.

Moreover, the Q3D extractor solver distinguishes between "DC" and "AC" analysis [61]. In the case of DC analysis, both resistance and inductance are quite constant with the frequency. Quasi-static electric solver is employed for DC calculation. When AC analysis is considered, inductance decreases in comparison to DC value remaining not dependent by frequency. On the contrary, resistance increases with the root square of frequency and the quasi-static magnetic solver is considered. The physical reason is the eventual occurrence of the skin effect that reduces the effective cross-section for current flow, resulting in increased resistance and decreased magnetic field. A remarkable difference between DC and AC analysis is relative to the mesh. In the case of DC analysis, a three-dimensional tetrahedral mesh is needed to account for the current distribution for the DC case, meanwhile, a two-dimensional triangular mesh is considered for the AC problem to model the whole current distributed on the conductor skin. Q3D software automatically chooses between DC and AC analysis. Fixing the frequency, if the conductor thickness is enough large (i.e., three times the skin depth) AC analysis should be carried out. Otherwise, if conductor thickness is lower than the skin depth, as in the specific case study, DC analysis results are most appropriate [61].

3.2. Electromagnetic Simulation Setup

The considered power dissipation is related only to copper traces losses. According to this, the device (die) is shorted, and it is modelled with conductive copper elements in this simulation. Hence, no Si and GaN die contributions have been considered in this simulation because the focus is on the interconnections. In Table 1, the material data, retrieved from suppliers, used in the electromagnetic simulation, have been reported.

Table 1. Material properties used for electromagnetic simulation.

Material	Simulated Objects	Relative Permittivity	Relative Permeability	Bulk Conductivity [S/m]	Dielectric Loss Tangent
Copper	Traces, vias, die	1	0.999991	58×10^6	0.02
Copper-CuFe ₂ P	Lead-frame	1	0.999991	39×10^6	0.02
Sinter paste	Solder	1	0.99998	3.3×10^6	0
Encapsulant	Case	5	1	0	0.02

Figure 4 shows the considered package's ports. In yellow, depicted are the seven ground ports in parallel, and in green the switch ports in parallel. As previously mentioned,

the simulation is performed in DC at a frequency equal to 500 kHz and fixing current at 90 A. As imposed by boundary conditions, the current travels from ground to switch ports. This condition, which is very stressful in terms of current, will be considered as the case study for the import of power losses in the thermal simulation in the next section. The copper trace thickness is equal to 32 μm . According to the DC regime, as explained in Section 3.1, a three-dimensional tetrahedral mesh with adaptive refinement has been implemented.

Figure 4. Electromagnetic simulation setup. In yellow, depicted are the ground ports in parallel and in green the switch ports in parallel.

3.3. Electromagnetic Simulation Results

Figures 5 and 6 show, respectively, the voltage map (V) and the surface current density (A/m^2), while Figure 7 depicts the volumetric loss density (W/m^3). Regarding the voltage map, it is possible to see the voltage drop between the two poles of the conductive path, while from Figure 6 there are no particular current crowding phenomena. The most relevant power losses concentration is at the edges of copper pads due to geometry discontinuities in such places. Specifically, the volumetric loss density will be the input of the following thermal simulation. Then, the power loss geometrical map is exported in the thermal simulation, which has an identical geometry, point by point. The total amount of power losses is 0.46 W

Figure 5. Voltage map, with a current equal to 90 A at 500 kHz as input.

Figure 6. Surface current density, with a current equal to 90 A at 500 kHz as input.

Figure 7. Volume loss density, with a current equal to 90 A at 500 kHz as input.

4. Thermal Simulation

4.1. Thermal Resistance Calibration and Model Simplification

As it was stated in Section 2.2, surface power loss has been imported in the thermal simulation environment from the output of the electromagnetic simulation. More specifically, power losses have been mapped onto the geometrical xyz coordinates. This obtained association has been exported in a dedicated text file that has been imported in the thermal simulation. The CAD model geometry must be exactly the same as the previous electromagnetic stage in order to ensure the proper power loss mapping in both simulation environments. It is performed a steady-state simulation, by using the FEM-based COMSOL software, in order to obtain the temperature field inside the package. In the first instance, thermal resistance $R_{th,j-a}$ at steady-state between junction (i.e., the chip) and ambient was calculated [24]. It was considered to place the package on a 1.6 mm-thick PCB with four copper layers, as depicted in Figure 8; a 100 μm -thick solder was interleaved between the

PCB and the package. Convective heat flux was implemented as a boundary condition, with a convective coefficient equal to $10 \text{ W/m}^2\text{K}$ that reproduces the heat exchange with still air at 20°C . Heat power (1 W) was forced on the top junction surface. $R_{\text{th,j-a}}$ was finally calculated as the difference between the average junction temperature and air temperature (20°C) and results equal to 40°C/W .

Figure 8. Implemented geometry for $R_{\text{th,j-a}}$ computation with printed circuit board and package.

In the following, and in the framework of the presented integrated electromagnetic-thermal approach, a simplified thermal FEM has been developed. In this last thermal model, PCB was not modeled in order to make the simulation simpler and quicker. An equivalent heat transfer coefficient has been searched for to be applied on the SiP-exposed pad in order to fit the $R_{\text{th,j-a}}$ found in the previous and more detailed (i.e., with PCB) simulation (40°C/W). The obtained equivalent heat transfer coefficient was $750 \text{ W/(m}^2\text{ K)}$, not representative of real heat exchange with the air, being only a fitting parameter. Three-dimensional tetrahedral mesh is considered. In Table 2, the material properties or the simulated objects, retrieved from suppliers, are shown.

Table 2. Material properties used for thermal simulation.

Material	Simulated Objects	Thermal Conductivity [W/(m K)]	Density [kg/m ³]	Heat Capacity at Constant Pressure [J/(kg K)]
Copper	Traces, vias, die	398	8960	385
Copper-CuFe ₂ P	Lead-frame	262	8920	385
Sinter paste	Solder	75	9520	460
Encapsulant	Case	0.79	2000	880

4.2. Thermal Simulation Results

Copper traces temperature map is the output of this simulation. Temperature and temperature swing are important parameters in the power device's and converter's operation. In fact, a safe thermal operation must be ensured for reliability needs. More specifically, the temperature swing is of paramount importance in this regard, and it must be kept at low values. Considering that the starting temperature is 20°C , the temperature swing is equal to around 19°C ; in fact, the maximum temperature reached is equal to around 39°C . A first-order check, to estimate the likelihood of the model, has been performed to calculate the $R_{\text{th,j-a}}$ obtained by dividing the temperature swing induced by electromagnetic losses (19°C) with the total dissipated power (0.46 W). The so-obtained $R_{\text{th,j-a}}$ is $\sim 41^\circ\text{C/W}$, quite aligned with the case in which a 1 W power dissipation occurs in the device. A thermal map of the internal part of the package is depicted in Figure 9. These temperature values are due to package surface losses, and they can assure the targeted SiP lifetime. Furthermore, there is quite a uniform temperature distribution in the paper, and there are no critical hotspots in any part of the structure. This could be explained by the fact that copper traces

are well spatially distributed inside the SiP. In the end, it can be possible to say that this current load is not critical for the thermal behavior of the copper interconnections in this GaN-based SiP.

Figure 9. Temperature distribution inside the package. Temperature swing is equal to around 20 °C.

5. Conclusions

In this paper, an integrated methodology, in order to study both electromagnetically and thermally an LV GaN SiP, called 2SPAK, is presented. The methodology considers only finite element-based simulations. The first stage of the flow relies on electromagnetic computation, which is aimed to obtain the surface power loss. Then, in the second stage, a thermal simulation has been performed with, as power input, the power losses' map calculated by the first electromagnetic simulation. The temperature swing due to copper losses is below 20 °C and does not represent an issue for package reliability, considering the elastic regime deformation of the copper layer, without any fatigue lifetime consumption. In future work, this methodology will be further exploited and extended in its capabilities, e.g., including die self-heating in the simulation.

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