



Article A Potentiostat Readout Circuit with a Low-Noise and Mismatch-Tolerant Current Mirror Using Chopper Stabilization and Dynamic Element Matching for Electrochemical Sensors

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Abstract: This paper presents a potentiostat readout circuit with low-noise and mismatch-tolerant current mirror using chopper stabilization and dynamic element matching (DEM) for electrochemical sensors. Current-mode electrochemical sensors are widely used to detect the blood glucose and viruses in the diagnosis of various diseases such as diabetes, hyperlipidemia, and the H5N1 avian influenza virus (AIV). Low-noise and mismatch-tolerant characteristics are essential for sensing applications that require high reliability and high sensitivity. To achieve these characteristics, a proposed potentiostat readout circuit is implemented using the chopper stabilization scheme and the DEM technique. The proposed potentiostat readout circuit consists of a chopper-stabilized programmable gain transimpedance amplifier (TIA), gain-boosted cascode current mirror, and a control amplifier (CA). The chopper scheme, which is implemented in the TIA and CA, can reduce low frequency noise components, such as 1/f noise, and can obtain low-noise levels. The mismatch offsets of the cascode current mirror can be reduced by the DEM operation. The proposed current-mirror-based potentiostat readout circuit is designed using a standard 0.18 μ m CMOS process and can measure the sensor current from 350 nA to 2.8 μ A. The input-referred noise integrated from 0.1 Hz to 1 kHz is 21.7 pA_{RMS}, and the power consumption was 287.9 μ W with a 1.8 V power supply.

Keywords: low-noise; mismatch-tolerant; electrochemical sensor; current mirror; chopper stabilization; dynamic element matching (DEM)

1. Introduction

Current-mode electrochemical sensors have been widely used to detect the blood glucose and viruses in the diagnosis of various diseases such as diabetes, hyperlipidemia, and the H5N1 avian influenza virus (AIV) [1–3]. The early diagnosis of highly pathogenic viruses such as H5N1 AIV is significant for preventing their rapid spread. A current-mode sensing technique using an aptamer-based field-effect transistor with an extended gate was previously introduced to detect AIV [3]. In addition, blood glucose sensing based on the electrochemical current-mode sensors with a potentiostat biasing circuit was reported in [1,2].

A general sensing mechanism with a three-electrode potentiostat electrochemical current-mode sensor is shown in Figure 1a [4]. For electrochemical current-mode sensors for blood glucose sensing, the level of diabetes can be detected by sensing the current generated through various potential differences according to the change in the concentration of glucose [4,5].

Glucose or virus concentrations are generally measured using an amperometric electrochemical sensor. A three-electrode structure with a potentiostat consisting of a working electrode (WE), reference electrode (RE), and counter electrode (CE) can measure the current generated by the electrochemical reaction [6,7]. When we assume a very small voltage drop across the current meter, the voltage difference between the WE and RE can be kept



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). constant by the feedback error amplifier [8]. The current generated by the electrochemical reaction flows from the CE to the WE, and this current is measured by the current meter. Therefore, the potentiostat sensor converts the solution concentration into a current. This characteristic of the sensor is suitable for bio-sensing applications such as blood glucose and virus analyses [9–11].



Figure 1. (a) Three-electrode potentiostat electrochemical sensor; (b) Conventional structure of the current mirror based potentiostat readout circuit.

The conventional circuit of the current mirror based potentiostat readout circuit is shown in Figure 1b. The M_0 and the control amplifier (CA) generate a feedback loop, and the V_{REF} between WE and RE, which is V_{DD} - V_{DAC} , is stabilized. The current from the electrochemical sensor, I_{SEN} , is copied by the current mirror, M_1 and M_2 . In this architecture, however, the mismatch between the current mirror transistors due to the process variations and channel-length modulation deteriorates the sensing accuracy. Moreover, the 1/f noise components generated in M_1 and M_2 act as the main noise contributors. Therefore, designing a current mirror with low-noise [12,13] and mismatch-tolerant characteristics is critical [14,15].

In this study, a potentiostat sensing circuit with a low-noise and mismatch-tolerant current mirror is proposed. The chopper stabilization scheme and dynamic element matching (DEM) technique are integrated to reduce the low-frequency noise and mismatch in the current mirror. The gain-boosted cascode scheme is also applied to the current mirror to reduce the mismatch between the drain-source voltages (V_{DS}) of the current mirror. The mirrored electrochemical current is converted to the output voltage by a low-noise chopper-stabilized transimpedance amplifier (TIA).

In previous studies [16,17], a different chopper frequency and DEM frequency are used, and this may introduce performance degradation due to the intermodulation distortion (IMD) between the chopper and DEM frequencies [18]. The low DEM frequency also requires the lower cut-off frequency of LPF, which consumes a large circuit area.

Because the square waveform has odd-harmonics, if the DEM clock and the chopper clock are operated at different frequencies, the interaction between these harmonics can generate IMD, which can degrade the signal quality.

As a result, the proposed readout circuit used the same frequency for the chopper and the DEM, therefore minimizing the IMD between the chopper and DEM. Moreover, the relatively higher operating frequency of the chopper and the DEM can relax the area consumption of the LPF.

The remainder of the paper is organized as follows. Section 2 presents the circuit implementation of the proposed current-mirror-based potentiostat readout circuit. Section 3

presents the simulation results of the proposed readout circuit. Finally, Section 4 concludes the paper with a performance summary and comparison.

2. Proposed Current-Mirror-Based Potentiostat Readout Circuit

A block diagram of the proposed potentiostat readout circuit is shown in Figure 2. The proposed circuit consists of potentiostat biasing, current mirror, and TIA stages. In the potentiostat biasing stage, the voltage potential between the WE and RE is maintained by the feedback loop. In the current mirror stage, the current from the CE is copied by the low-noise and mismatch-tolerant current mirror. In the TIA stage, the current from the current from the current mirror stage is converted to a voltage signal. This voltage signal can be converted to a digital code using an analog-to-digital converter (ADC).



Figure 2. Block diagram of the proposed potentiostat readout circuit.

The top architecture of the proposed current-mirror-based potentiostat readout circuit is shown in Figure 3. The input stage of the readout circuit consists of a sensor and CA. The CA generates a feedback loop with an M_5 . It maintains a constant V_{REF} between RE and WE. The V_{REF} is calculated as

$$V_{REF} = V_{WE} - V_{RE} = V_{DD} - V_{B1}$$
(1)



Figure 3. Top architecture of proposed current mirror based potentiostat readout circuit.

The current from the CE is mirrored by the gain-boosted cascode current mirror stage. The mirrored current is converted to the voltage through the TIA stage. Here, the transimpedance gain is programmable to adjust the gain. The low-pass filter (LPF) filters out the unwanted high-frequency components, and also acts as an antialiasing filter before a 12-bit successive approximation register (SAR) ADC. The internal operating parameters,

including the clock timing, transimpedance gain, V_{B1} voltage, and chopper frequency are programmable, through a serial peripheral interface (SPI).

The architecture of the proposed current mirror is shown in Figure 4a. The current input, I_{IN} , is mirrored to the output current, I_{OUT} . To increase the output resistance of the current mirror and to reduce the number of errors due to the channel-length modulation, a gain-boosted cascode scheme is adopted. The W/L ratio between M_a and M_b determines the current ratio between I_{IN} and I_{OUT} . Thus, the mismatch derived from the process variation between M_a and M_b directly affects the accuracy of the current mirror. The I_{IN} is converted to the gate voltage by the diode-connection between the drain of M_c and the gate of M_a , and the gate voltage is converted to the I_{OUT} by the transconductance of M_b ; thus, the flicker noises from M_a and M_b largely contribute to the overall noise. In addition, the flicker noise from the gain-boosting amplifier acts as the main noise contributor. In this design, these mismatches and low-frequency noise components can be cancelled by the four-phase combinations of the chapter and DEM.



Figure 4. (a) Architecture of the proposed current mirror; (b) timing diagram of the chopper with current mirror using the DEM technique.

In Figure 4b, the current mirror is operated in four phases as a combination of three switching signals, *CLK* 1, *CLK* 2, and *CLK S*. The connections between the mirror transistors and amplifier are altered periodically as P_1 , P_2 , P_3 , and P_4 . The mismatches between the elements can be averaged out. In this current mirror, the chopper operation and dynamic element matching operation are merged into four phases. The low-frequency noise of the current mirror and amplifier are up-modulated by the chopper operation. The mismatch between the transistors in the current mirror and the amplifier is averaged, and thus a highly accurate current mirror operation with low noise is achieved.

The circuit configuration of the proposed current mirror as the phases of the combined chopper and DEM operations are illustrated in Figure 5. At the point of the connection around M_3 , in Phase 1, the source of M_3 is connected to the drain of M_2 , and the gate of M_3 is connected to the negative output of the amplifier. In Phase 2, the source of M_3 remains connected to the drain of M_2 ; however, the gate of M_3 is connected to the positive output of the amplifier. In Phase 3, the source of M_3 is connected to the drain of M_1 , and the gate of the M_3 is connected to the drain of M_1 , and the gate of M_3 is connected to the negative output of the amplifier. In Phase 3, the source of M_3 is connected to the negative output of the amplifier. In Phase 4, the source of M_3 is connected to the drain of M_1 , and the gate of M_3 is connected to the negative output of the amplifier. Using these four-phase combinations of the chopper and DEM techniques, the mismatches and the low-frequency noise components can be averaged out.



Dynamic Element Matching (DEM) Configuration

Figure 5. Operation principles of chopper and DEM technique.

Figure 6 shows the single-ended chopper operational amplifiers used in the implementation of the CA and the TIA. The amplifier adopts complementary input stages of the PMOS and NMOS differential pairs for the rail-to-rail input common-mode range. The intermediate stage is implemented using a folded-cascode topology with class-AB biasing, and the output stage is implemented in class-AB. The choppers in front of both the input stage and common-gate stages are implemented, as shown in Figure 6. The individual switch in the chopper is implemented using the CMOS transmission gate, and the chopping frequency of this circuit is 125 kHz having non-overlapping clock. Non-overlapping clock have 10 ns duration.



Figure 6. Schematic of the single-ended chopper amplifier.

The chopper amplifier modulates the input signal to the high chopping frequency band to avoid the low-frequency flicker noise. The modulated signal is amplified and demodulated to the baseband using an output chopper. Here, the offset and the low-frequency noise are up-modulated by the output chopper, and is attenuated by the following LPF. Thus, a thermal-noise-limited signal-to-noise ratio (SNR) can be achieved using the chopper operation.

Figure 7 shows the fully differential amplifier used for gain boosting of the current mirror. A general two-stage folded-cascode Miller-compensated topology with common mode feedback (CMFB) is adopted. In this gain-boosted current mirror, because the input common mode level is low (approximately 100–200 mV), and the PMOS input stage is exploited, two source followers are added to the CMFB circuit to reduce the resistive loading for common mode detection.



Figure 7. Schematic of the fully-differential amplifier.

3. Results and Discussions

A three-port electrochemical sensor was modeled using a voltage controlled resistor, as shown in Figure 8 [19–21]. The resistance between the RE and CE is modeled as a constant resistor at 10 k Ω . The typical voltage difference between the WE and RE was set to be 700 mV. In this circuit, the WE was forced by the VDD supply (1.8 V). The RE is typically indirectly biased to 1.1 V by the virtual short between the feedback amplifier input nodes. The current change due to the electrochemical reaction is modeled using a voltage-controlled resistor, which varies from 250 to 2250 k Ω , and is implemented using Verilog-A. Since the chip is under fabricate, post layout simulation was performed using parasitic extraction (PEX).



Figure 8. Configuration of the equivalent sensor model using a voltage-controlled resistor.

Figure 9 shows the layout of the circuit. The circuit was implemented using a 0.18-um CMOS process with an active area of 1.073 mm². The overall current consumption was 287.9 μ W.



Figure 9. Layout of proposed readout circuit.

Figure 10a shows the input-output characteristics of the proposed current mirror between the input current ($I_{SEN.IN}$) and output current ($I_{SEN.OUT}$). The maximum error from 0 to 4.5 µA for the input current is 1.129%FSO (full scale output).



Figure 10. (a) Linearity simulation result of the sensing current; (b) linearity simulation result of the TIA.

Figure 10b shows the transimpedance of the TIA was simulated to be 300 k Ω with a maximum nonlinearity of 0.793% in the current range of 3.83 μ A.

Figure 11 shows the transient simulation results of the proposed potentiostat readout circuit. The resistance between the WE and RE varied from 250 to 2250 k Ω , and the V_{BIAS} was set to 500 mV. The transimpedance of the TIA was set to 300 k Ω and feedback capacitance of 10 pF. Because the output current is inversely proportional to the sinusoidal input resistance change of the electrochemical sensor, the red line (I_{SEN}) and blue line (V_{OUT}) have the waveform shapes of 1/[1 + sin (x)].



Figure 11. Output voltage simulation results of the current mirror and TIA.

Figure 12 shows the stability simulation results of the TIA with the feedback transimpedance resistance of 300 k Ω and feedback capacitance of 10 pF. The open-loop gain (OLG) is 117 dB, the unit gain bandwidth (UGBW) is 2.211 MHz, and the phase margin is 84.67 deg. This result shows stability at high-speed performance and can be setting the variable gain setup.



Figure 12. Stability simulation result of proposed TIA.

The input referred noise simulation results are shown in Figure 13. The input referred current noise at 1 Hz is reduced from 13.2775 pA/ \sqrt{Hz} to 936 fA/ \sqrt{Hz} by the chopper operation. The input-referred noise density and the integrated input-referred noise from 0.1 Hz to 1 kHz are 21.7 pA_{RMS}, respectively.



Figure 13. Input-referred noise simulation results of the readout circuit.

Table 1 shows noise contributors of readout circuit. When the chopper is disabled, the flicker noise components in the current mirror, $M_{1,2}$, form about 72% of the total noise. When the chopper is enabled, the main contributors are changed to the thermal noise of $M_{1,2}$.

Transistor	Noise Source	Total Noise Chopper Disable (%)	Total Noise Chopper Enable (%)	
$M_{1,2}$ (current mirror)	Flicker	71.52	12.44	
$M_{1,2}$ (current mirror)	Thermal	8.03	31.02	
<i>PM</i> _{2,3} (TIA input pair)	Flicker	4.06	1.40	
NM _{2,3} (TIA input pair)	Flicker	3.62	1.38	
$PM_{4,5}$ (TIA cascode load)	Flicker	3.53	0.18	
$NM_{4,5}$ (TIA cascode load)	Flicker	2.8	0.10	
<i>NM</i> _{6,7} (TIA cascode)	Flicker	0.18	2.78	

Table 1. Simulated noise contributors.

Figure 14 show the Monte-Carlo simulation results with N = 200. The input current, V_{BIAS} and R_f , were fixed to 1 μ A, 500 mV, and 300 k Ω , respectively. The desired nominal output of the TIA was 800 mV. In the simulation, the standard deviation of the TIA output was reduced from 2.49 to 0.12 mV by the DEM operation in Figure 14d.



Figure 14. Mismatch simulation results when the chopper and DEM were (**a**) disabled; used different frequency (**b**) $f_{ch} = 125$ kHz, DEM clock = 100 kHz; (**c**) $f_{ch} = 125$ kHz, DEM clock = 150 kHz; used same frequency (**d**) $f_{ch} = DEM$ clock = 125 kHz.

As shown in Figure 14b,c, the standard deviation of the TIA output was 0.75 to 0.68 mV. The different chopper frequency and DEM frequency were used, and this may introduce performance degradation due to the IDM between the chopper and DEM frequencies. In Figure 14d, the same frequency for the chopper and the DEM is used, thus IMD between the chopper and DEM can be minimized.

Table 2 summarizes the performances of the proposed potentiostat readout circuit with those of previous studies [4,16,17,22–24]. The simulation results of this circuit achieve the wide input range, low noise, and mismatch-tolerant characteristics.

	This Work (Simulated)	TBCAS 2013 [22]	TCAS-I 2009 [4]	Sensors 2017 [23]	IEEE Access 2020 [24]	ISCAS 2012 [16] TCAS-I 2013 [17]
Process(µm)	0.18	0.35	0.18	0.18	0.065	0.13
Architecture	Current mirror	CC ¹	Current mirror	FDDA ²	1st-order delta-sigma converter	CC
Chopper	Y (125 kHz)	Ν	Ν	Ν	Ν	Y (10 kHz)
DEM O/X	Y (125 kHz)	Ν	Ν	Ν	Ν	Y (500 Hz)
Output format	Voltage	Digital codes	Frequency	Voltage	Digital codes	Current
Supply voltage (V)	1.8	3.3	1.8	1.8	1.2	1.2
Power consumption (µW)	287.9	188	50	53	15–25 (0.1–1.5 μA)	4
Input current range (A)	100 n–3.83 μ	24 p–350 n	1 n–1 μ	100 u–840 u	100 n–1.5 μ	8.6 p–350 n
Input-referred noise (pA _{RMS})	21.7 (0.1 Hz~1 kHz) (simulated)	24 (100 Hz BW) (measured)	N/A	N/A	168.3 ³ (1 Hz BW) (measured)	20.31 ⁴ (0.01 Hz ~1 kHz) (measured)

Table 2. Performance summary comparison between the proposed potentiostat readout circuit and previous studies.

¹ Current conveyer; ² Fully differential difference amplifier; ³ Output digital code is limited to 10 bits; ⁴ Standard deviation (1 σ) of output current with 100 pA input current.

4. Conclusions

This paper proposes a potentiostat readout circuit with a low-noise and mismatchtolerant current mirror using chopper stabilization and dynamic element matching (DEM) for electrochemical sensors. The potentiostat electrochemical current-mode sensors convert potential differences into current signals according to the concentration of the solution, and the readout circuit converts current signals into voltage signals.

The proposed potentiostat readout circuit consists of a potentiostat biasing stage using CA, a gain-boosted cascode current mirror, TIA, I/V reference, SPI, oscillator, and a timing generator. In order to detect small changes in current, the proposed readout circuit with mismatch-tolerant and low-noise characteristics is essential. For this purpose, a chopper was adopted for the input and output stages of the CA, current mirror, and TIA. The DEM technique was applied to make it mismatch-tolerant. Thus, the clock generator for chopping, along with the DEM and an SPI for communication to the digital circuits, were integrated into a single chip.

The proposed readout circuit was under fabricate by implementing a 0.18-µm CMOS process with an active area of 1.073 mm². It consumed 287.9 µW of power at a 1.8 V supply voltage. The input-referred current noise was reduced to 936 fA/ \sqrt{Hz} at 1 Hz, and the input-referred noise from 0.1 Hz to 1 kHz was 21.7 pA_{RMS}. The input current range was in the range of 100 nA to 3.83 µA (maximum nonlinearity < 1%). The standard deviation of the TIA output was reduced from 2.49 mV to 0.12 mV by the DEM operation. These results suggest that the readout circuit proposed in this paper is suitable as an electrochemical sensor using a potentiostat.

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