



Article Improved Modulation Strategy Based on Minimum Energy Storage Principle for Electrolytic-Capacitor-Less Six-Switch Converter

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Abstract: An improved modulation strategy based on minimum energy storage for DC-link capacitance reduction in a six-switch AC-AC converter is proposed. The proposed modulation strategy enables the energy on the capacitor to accumulate and release twice each in a complete switching cycle, achieving the effect of "fast charging and discharging". Meanwhile, the inversion and rectification are modulated synchronously. Hence, there is minimum energy stored in the DC-link capacitor. Then, the time average modeling analysis is presented to take insight analysis. When there is the same voltage ripples constraint on the DC side for the conventional and improved modulation strategies, the six-switch converter under the improved modulation strategy has the much less capacitance value of the storage capacitor and even realizes non-electrolytic capacitance. Therefore, improving the system efficiency, power density, and output waveform quality and extending the system life can be achieved. The operation principle and modulation strategy are discussed in detail. Finally, the simulation model and experimental prototype are built to verify effectiveness of the topology and correctness of the proposed six-switch AC-AC converter modulation strategy.

Keywords: six-switch converter; electrolytic capacitor-less; ripple reduction

1. Introduction

Single-phase AC-DC-AC converters with the same input/output frequencies can be found in multi-electric aircraft [1], such as power interface units, standby power supplies, uninterruptible power supplier, etc. Large DC-link energy storage capacitors are usually used to adsorb pulsating power, which is harmful to the system, but the presence of the large electrolytic capacitor will lead to larger volume, heavier weight, and higher price [2]. So, a great deal of research is devoted to reducing DC-link capacitor size and mitigating second-order power in the single-phase converter.

At present, non-electrolytic capacitive methods can be divided into two categories: active methods and passive methods [3]. The main idea of the passive methods is to use passive components or passive networks instead of large electrolytic capacitors for energy storage. The simplest passive method is to replace the large electrolytic capacitor with multiple small-capacity non-electrolytic capacitors (such as film capacitors) in parallel, but its obvious disadvantages such as low withstand voltage, large volume, and high price limit its practical applications. In [4–8], a resonance unit is used to replace the traditional DC energy storage unit, eliminating large-capacity energy storage components, while also realizing soft-switching, and the dynamic performance of the system is also improved. However, due to the shortcomings of the resonant unit itself, the circuit will generate higher voltage and current stress, and the conduction loss will also increase. In addition, this passive method also has the disadvantages of large volume and heavy weight.

The active methods mainly can be grouped into reducing or transferring the instantaneous power difference. Some control strategies are proposed in [9,10]. The instantaneous



Citation: Tan, Q.; He, L. Improved Modulation Strategy Based on Minimum Energy Storage Principle for Electrolytic-Capacitor-Less Six-Switch Converter. *Appl. Sci.* 2021, *11*, 5901. https://doi.org/10.3390/ app11135901

Academic Editor: Daniel Villanueva Torres

Received: 7 April 2021 Accepted: 7 May 2021 Published: 25 June 2021

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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). power difference between AC and DC sides is narrowed by injecting third and fifth harmonics actively into the AC side. However, this kind of method is at the cost of reducing the power factor of the power converter, so it is only suitable for occasions where the power factor requirement is not high. Another way to directly reduce the instantaneous power difference is to allow greater pulsation of the output current, which has been studied a lot in [11,12]. The pulsation of the output power also increases and when the instantaneous input and output power are similar, a smaller non-electrolytic capacitor can be used to balance the energy difference. This kind of method is mostly used for light-emitting diode (LED) driving, which may cause flicker, and the system efficiency is low. It is only suitable for occasions where the DC side load is not sensitive to pulsating current. The second active method that achieves the transfer of pulsating power through additional circuits is described in [13–15]. The basic idea is to transfer the instantaneous power difference to an additional non-DC-link energy storage capacitor through an external circuit to achieve DC bus power decoupling, but it adds additional hardware cost and control cost, and it also increases the system loss. A method that only changed the control algorithm without adding auxiliary circuits is proposed in [16–18]. However, this method is only designed for specific circuit, and huge calculation workload is needed to obtain its control algorithm by analyzing the switching states of each circuit.

The six-switch converter adopting the idea of components multiplexing instead of the traditional single-phase back-to-back converter is used to solve the above issues in this paper. On this basis, a non-electrolytic capacitance method without changing the circuit structure or adding auxiliary circuits is proposed. This method improves the traditional modulation strategy based on the principle of minimum energy storage. While ensuring the stable operation of the converter, it not only reduces the fluctuation of the DC bus capacitor voltage in the line frequency cycle, but also improves the quality of the output waveform. Compared with the traditional single-phase eight-switch converter, the proposed converter can achieve the same effect with fewer switches and smaller DC-link capacitors. The improved modulation strategy of the six-switch converter also has some guiding effects on the optimization of the nine-switch converter.

The paper is organized as follows. The topology description and operation principles are introduced in Section 2. Then, the analysis of improved modulation strategy and the comparison with the traditional one are explained in detail by means of mathematical derivation in Section 3. A prototype is implemented to verify the performance of the proposed converter in Section 4. Finally, this paper is concluded in Section 5.

2. The Topology and Modulation Principle of Six-Switch Converter

The topology of the six-switch converter is shown in Figure 1. Each bridge arm is composed of three switches in series, and there are two sets of input and output. Compared with the traditional single-phase back-to-back AC-DC-AC converter, the proposed converter reduces two switches. In the proposed six-switch converter, the switch in the middle of each bridge arm is shared by the rectifier and inverter, and the voltage v_{XN} is no greater than v_{AN} at any time. As shown in Table 1, each bridge arm of the six-switch converter has three switching states.

In order to meet the switching constraint requirements of the six-switch converter, the modified carrier-based PWM method is applied, and the modulation reference of the upper rectifier and the modulation reference of the lower inverter are compared with a common triangular carrier, respectively, as shown in Figure 2.

The instantaneous value of the upper reference must be no less than the lower reference. The PWM signal of switch ST_1 (ST_3) is generated by comparing the upper (lower) reference and the triangular carrier, and the PWM signal of switch ST_2 is generated by logic operation.

$$ST_{2} = (ST_{1})XOR(ST_{3})$$

$$ST_{1} = \begin{cases} 1, & v_{rA} \ge v_{cw}, ST_{3} = \begin{cases} 1, & v_{rX} \le v_{cw} \\ 0, & v_{rA} < v_{cw}, \end{cases} ST_{3} = \begin{cases} 1, & v_{rX} \le v_{cw} \\ 0, & v_{rY} > v_{cw} \end{cases}$$
(1)

where v_{cw} is the common triangular carrier, v_{rA} and v_{rX} are the upper and the lower modulation references, respectively.



Figure 1. The six-switch converter topology.

Table 1. Switching status of the six-switch converter.

Switching Status	ST_1	ST_2	ST ₃	v_{AN}	v_{XN}
1	1	1	0	v_d	v_d
2	0	1	1	0	0
3	1	0	1	v_d	0



Figure 2. Generation of the single bridge arm PWM signal.

Figure 3 shows the modulation references of ST_1 , ST_3 , ST_4 , ST_6 in a six-switch converter. It can be observed that due to the relative position changes of the four references in one line frequency cycle, the switching signals of the six switches also change. Therefore, the relative position in a line frequency cycle can be divided into four states (two for the first half cycle and two for the second half cycle) for analysis. Take the first half line frequency cycle of the modulation reference as an example to analyze the working states of the circuit.



Figure 3. Reference modulated waves of *ST*₁, *ST*₃, *ST*₄, *ST*₆.

There are four working states of the six-switch converter, which are introduced as follows. The rectification state (abbreviated as RS) is shown in Figure 4a, the inversion state (abbreviated as IS) is shown in Figure 4b, the freewheeling state (abbreviated as FS) is shown in Figure 4c, and the both-way state (abbreviated as BS) is shown in Figure 4d. When the relative positions of four modulation references are shown as state A in Figure 3, the six-switch converter has the first three working states in one switching cycle. When the relative positions of four modulation references are shown as state B in Figure 3, the six-switch converter has all four working states in one switching cycle.



Figure 4. Four working states of the six-switch converter: (**a**) rectification state; (**b**) inversion state; (**c**) freewheeling state; (**d**) both-way state.

From the aforementioned six-switch converter modulation method, a schematic diagram of six switching states in one switching cycle can be achieved, as shown in Figure 5. The state A in Figure 5a corresponds to the state A in Figure 3, which means the relative positions of the modulation references are consistent. State B in Figure 5b corresponds to state B in Figure 3.



Figure 5. Schematic diagram of the switching state: (a) state A; (b) state B.

 v_{cw} , v_{rA} , and v_{rX} were previously defined on paper, and v_{rB} and v_{rY} are the modulation references of the upper switch and the modulation references of the lower switch of the second bridge arm, respectively. d_1 , d_3 , d_4 , and d_6 denote the duty ratios of ST_1 , ST_3 , ST_4 , ST_6 , and T_5 is the switching period. From Figure 5a, it can be concluded that when the switching states of $ST_1 \sim ST_6$ are {101011}, the six-switch converter is in RS, and the state duration is $(d_1-d_4)T_5$. When the switching states of $ST_1 \sim ST_6$ are {110101}, the six-switch converter is in IS, and the state duration is $(d_6-d_3)T_5$. The rest of the switching states are in FS, and the state duration is $(1 - d_1 + d_3 + d_4 - d_6)T_5$.

3. Improved Modulation Strategy Analysis of Six-Switch Converter Based on Time Average Modulation

It is assumed the inversion and rectification have the same power factor. Under the traditional six-switch converter control strategy, one switching cycle includes eight working states, followed by FS, RS, FS (BS in state B), IS, FS, IS, FS (BS in state B), RS. Two RS (or IS) are too close, and there is only one FS between them, so that the DC side capacitor is continuously charged (or discharged). A large capacitor is required, which greatly limits practical applications of the six-switch converter. The key point of the proposed improved modulation method is to exchange rectification state and inversion state in the second half of the switching cycle by logic control, so that the order of the eight states in a cycle becomes FS, RS, FS (BS in state B), IS, FS, RS, FS (BS in state B), IS. Therefore, the energy on the capacitor can quickly accumulate and release in a complete switching cycle, achieving the effect of 'fast charging and discharging'. Figure 6 shows a larger version of the DC side capacitor voltage v_d under two modulation strategies. Each linear section in the curve corresponds to FS, RS, IS, and BS, respectively.



Figure 6. Partially enlarged view of v_d in switching period.

According to the input/output power balance theory and supposing $V_S \approx V_{AB} \approx V_{XY}$, the Equation (2) can be obtained by vector relations. Where X_1 is the input impedance

and X_2 is the output impedance. θ_1 represents the phase angle of rectification modulation reference and θ_0 is the power factor angle of inverter load. When the radio of X_1/X_2 is about 0.2, the unit input power factor can be ensured.

$$V_{AB}I_{S}\cos\theta_{1} = V_{XY}I_{0}\cos\theta_{0}$$

$$\Rightarrow \theta_{1} = -\sin^{-1}\left(\frac{X_{1}}{X_{2}}\cos\theta_{0}\right)$$
(2)

The voltage fluctuation of the DC side capacitor is caused by the fluctuating current flowing through the capacitor, as shown in Equation (3). When the amplitude of i_c becomes smaller, the capacitor which used to keep v_d relatively stable also decreases. In order to verify the effectiveness of the improved six-switch converter modulation strategy, the i_c under the traditional and improved modulation strategies are calculated and compared respectively.

$$v_d(t) = \frac{1}{C_d} \int_0^t i_c(t) dt + V_d$$
(3)

The equation of Kirchhoff's Current Law at point P of six-switch converter in Figure 1 is:

$$i_c(t) = i_1(t) - i_4(t)$$
 (4)

In (4), $i_1(t)$ and $i_4(t)$ are currents flowing through switch ST_1 and ST_4 based on the predefined reference direction. The average value of current $i_1(t)$ can be calculated according to the switching state of the six-switch converter. When the switching states of ST_1 , ST_2 , ST_3 are {011}, $i_1(t) = 0$; when the switching states becomes {101}, $i_1(t) = i_s(t)$ with the duration of $(d_1 + d_3 - 1)T_s$; when the switching states are {110}, $i_1(t) = i_s(t) - i_o(t)$ with the duration of $(1 - d_3)T_s$. Therefore, the average current $i_1(t)$ can be written as:

$$i_1(t) = i_s(t)(d_1 + d_3 - 1) + (i_s(t) - i_o(t))(1 - d_3)$$
(5)

Similarly, when the switching states of ST_4 , ST_5 , ST_6 are {011}, $i_4(t) = 0$; when the switching states are {101}, $i_4(t) = i_5(t)$ with the duration of $(d_4 + d_6 - 1)T_5$; when the switching states are {110}, $i_4(t) = i_5(t) - i_0(t)$ with the duration of $(1 - d_6)T_5$. So, the average current $i_4(t)$ can be written as:

$$i_4(t) = i_s(t)(d_4 + d_6 - 1) + (i_s(t) - i_o(t))(1 - d_6)$$
(6)

Substitute (5) and (6) into (4), average current i_c can be figured out as:

$$i_c(t) = (d_1 - d_4)i_s(t) - (d_6 - d_3)i_o(t)$$
(7)

Modulation reference for rectifier is defined as:

$$v_{rA}(t) = m_r \sin(\omega t + \theta_1) + (1 - m_r) \tag{8}$$

Modulation reference for inverter is defined as:

$$v_{rX}(t) = m_i \sin(\omega t + \theta_1 + \varphi) - (1 - m_i)$$
(9)

where m_r and m_i are modulation indices for the rectifier and inverter, respectively. Assuming unity input power factor operation condition, φ is phase angle difference between rectifier reference and inverter reference.

Duty radios d_1 , d_3 , d_4 , d_6 can be calculated through similar triangle theory:

$$\frac{d_1 T_s}{T_s} = \frac{1 + m_r \sin(\omega t + \theta_1) + (1 - m_r)}{2} \tag{10}$$

$$d_1 = \frac{1 + m_r \sin(\omega t + \theta_1)}{2} + d_{off1}$$
(11)

Similarly,

$$d_4 = \frac{1 - m_r \sin(\omega t + \theta_1)}{2} + d_{off1}$$
(12)

$$d_{3} = \frac{1 - m_{i}\sin(\omega t + \theta_{1} + \varphi)}{2} - d_{off2}$$
(13)

$$d_{6} = \frac{1 + m_{i}\sin(\omega t + \theta_{1} + \varphi)}{2} - d_{off2}$$
(14)

Parameters d_{off1} and d_{off2} are offset values utilized for moving up/down modulation reference of rectifier/inverter.

Finally, substitute d_1 , d_3 , d_4 and d_6 into Equation (7):

$$i_{c}(t) = m_{r} \sin(\omega t + \theta_{1})i_{s}(t) - m_{i} \sin(\omega t + \theta_{1} + \varphi)i_{o}(t)$$

$$= m_{r} \sin(\omega t + \theta_{1})I_{s} \sin \omega t$$

$$-m_{i} \sin(\omega t + \theta_{1} + \varphi)I_{o} \sin(\omega t + \theta_{1} + \varphi - \theta_{o})$$

$$= (\frac{1}{2}m_{r}I_{s} \cos \theta_{1} - \frac{1}{2}m_{i}I_{o} \cos \theta_{o})$$

$$+ \frac{1}{2}m_{i}I_{o} \cos(2\omega t + 2\theta_{1} + 2\varphi - \theta_{o})$$

$$- \frac{1}{2}m_{r}I_{s} \cos(2\omega t + \theta_{1})$$
(15)

where $i_s(t)$ is expressed as $I_s \sin w t$, the phase angle of inversion modulation reference is $(wt + \theta_1 + \varphi)$, so the output voltage v_{xy} is also $(wt + \theta_1 + \varphi)$. Since the output current i_o lags behind the inversion output voltage v_{xy} , the output current's phase angle is $(wt + \theta_1 + \varphi - \theta_o)$. θ_o is the power factor angle of inverter load, thus $i_o(t)$ can be expressed as $I_o \sin(wt + \theta_1 + \varphi - \theta_o)$. The angle relationship of proposed converter is shown below.

$$v_s \stackrel{0}{\longleftrightarrow} i_s \stackrel{\theta_1}{\longleftrightarrow} v_{AB} \stackrel{\varphi}{\longleftrightarrow} v_{XY} \stackrel{\theta_o}{\longleftrightarrow} i_o$$

The constant term in Equation (15) is identical to zero based on the assumptions of no switching or capacitor loss.

$$i_c(t) = \frac{1}{2}m_i I_o \cos(2\omega t + 2\theta_1 + 2\varphi - \theta_o) -\frac{1}{2}m_r I_s \cos(2\omega t + \theta_1)$$
(16)

Amplitude of current i_c can be gotten as below through expansion of (16).

$$I_{c} = \sqrt{\frac{1}{4}m_{i}^{2}I_{o}^{2} + \frac{1}{4}m_{r}^{2}I_{s}^{2} - \frac{1}{2}m_{i}m_{r}I_{o}I_{s}\cos(2\varphi - \theta_{o} + \theta_{1})}$$
(17)

It is observed from (17) that when phase angle φ reaches $(\theta_o - \theta_1)/2$, minimization of AC power variation can be achieved in DC-link voltage. Therefore, φ is equal to $(\theta_o - \theta_1)/2$ in this paper and modulation indices for rectifier and inverter are supposed to be approximately the same $(m_r = m_i = m)$. I_{cmin} under traditional control can be written as:

$$I_{cmin} = \frac{1}{2}m|I_0 - I_s|$$
(18)

 I_c' under improved control can be attained in the same way. When the switching states of ST_1 , ST_2 , ST_3 are {011}, $i_1'(t) = 0$; when the switching states are {101}, $i_1'(t) = i_s(t)$ with the duration of $((d_1 + d_3 + d_4 + d_6)/2 - 1)T_s$; when the switching states are {110}, $i_1'(t) = i_s(t) - i_o(t)$ with the duration of $((d_1 - d_3 - d_4 - d_6)/2 + 1)T_s$. Therefore, the average current $i_1'(t)$ can be written as:

$$i_1'(t) = d_1 i_s(t) - \frac{d_1 - d_3 - d_4 - d_6 + 2}{2} i_o(t)$$
⁽¹⁹⁾

Similarly, when the switching states of ST_4 , ST_5 , ST_6 are {011}, $i_4'(t) = 0$; when the switching states are {101}, $i_4'(t) = i_s(t)$ with the duration of $((d_1 + d_3 + d_4 + d_6)/2 - 1)T_s$; when the switching states are {110}, $i_4'(t) = i_s(t) - i_o(t)$ with the duration of $(1 - d_6)T_s$. So, the average current $i_4'(t)$ can be written as:

$$i_4'(t) = \frac{d_1 + d_3 + d_4 - d_6}{2}i_s(t) - (1 - d_6)i_o(t)$$
⁽²⁰⁾

$$i_c'(t) = \frac{d_1 - d_3 - d_4 + d_6}{2} (i_s(t) - i_o(t))$$
(21)

Substituting d_1 , d_3 , d_4 and d_6 into Equation (20), it yields:

$$i'_{c}(t) = \frac{1}{4} \{ [m_{r}I_{s}\cos\theta_{1} - m_{r}I_{o}\cos(\theta_{o} - \varphi) + m_{i}I_{s}\cos(\varphi - \theta_{1}) - m_{i}I_{o}\cos\theta_{o}] + [-m_{r}I_{s}\cos(2\omega t + \theta_{1}) + m_{r}I_{o}\cos(2\omega t + 2\theta_{1} - \theta_{o} + \varphi) - m_{i}I_{s}\cos(2\omega t + \theta_{1} + \varphi) + m_{i}I_{o}\cos(2\omega t + 2\theta_{1} - \theta_{o} + 2\varphi)] \}$$

$$(22)$$

The constant term in Equation (22) is identical to zero based on the assumptions that no switching or capacitor loss.

$$i'_{c}(t) = \frac{1}{4} [-m_{r}I_{s}\cos(2\omega t + \theta_{1}) +m_{r}I_{o}\cos(2\omega t + 2\theta_{1} - \theta_{o} + \varphi) -m_{i}I_{s}\cos(2\omega t + \theta_{1} + \varphi) + m_{i}I_{o}\cos(2\omega t + 2\theta_{1} - \theta_{o} + 2\varphi)]$$

$$(23)$$

Amplitude of current i_c can be got as below through expansion of (23).

$$I_{c}' = \frac{1}{4}m\sqrt{2(1+\cos\varphi)(I_{o}^{2}+I_{s}^{2}-2I_{o}I_{s}\cos(\varphi+\theta_{1}-\theta_{o}))}$$
(24)

 I_c can reach its minimum when $\varphi = \theta_o - \theta_1$:

$$I'_{\rm cmin} = \frac{1}{4}m|I_o - I_s|\sqrt{2(1 + \cos(\theta_o - \theta_1))}$$
(25)

The above has been obtained $I_{cmin} = 0.5m | I_o - I_s |$. Subtracting Equation (18) from (25) to compare the amplitude, it yields:

$$I_{cmin} - I'_{cmin} = \frac{1}{4}m|I_o - I_s| \left(2 - \sqrt{2(1 + \cos(\theta_o - \theta_1))}\right) > 0$$
(26)

It can be known $I_{cmin} > I_c'_{min}$ from (26). The calculation result shows that improved modulation strategy reduces the amplitude of I_c and the DC side voltage fluctuation. Therefore, a smaller capacitor C_d can be used to maintain the relative stability of the DC voltage v_d , thereby achieving the purpose of reducing the capacitance.

The derivations of I_{cmin} and $I_{c'min}$ have already reflected the difference of modulation strategy. Therefore, whether the improved modulation strategy is effective can be judged by observing the fluctuation of DC side capacitor voltage under the line frequency cycle.

4. Simulation and Experimental Results

In order to further verify the feasibility and correctness of the proposed modulation strategy, a linear-load typical system with unity input power factor is built on the Matlab/Simulink platform. The simulation results based on traditional and improved modulation strategy, respectively, are compared to prove the validity of the improved strategy. Simulation parameters are shown in Table 2.

Components	Specifications	Components	Specifications
Input inductance (L_1)	3 mH	Input/output frequencies	50 Hz
Input inductor resistance (R_1)	0.1Ω	Switching frequency	10 kHz
Output filter inductance (L_2)	0.43 mH	Output load resistance (R_L)	5 Ω
Filter inductor resistance (R_2)	0.3 Ω	Modulation index(m)	0.8
Output filter capacitor (C_2)	140 uF	phase angle (θ_1)	-11°
DC-link capacitor (C_d)	470 uF	phase angle difference (φ)	0.4°
Input voltage amplitude	36 V	phase angle difference (φ /)	0.8°

Table 2. Simulation parameters.

Figure 7 shows the waveforms of input/output voltage, current, and DC-link voltage under traditional control when φ is equal to 0.4. The percentage of DC-link voltage variation is limited into 2.71% (1.24 V/45.81 V = 2.71%), and total harmonic distortion (THD) of the output voltage v_c is 1.39%.



Figure 7. Waveforms under traditional modulation strategy.

Figure 8 shows the waveforms of input/output voltage, current, and DC-link voltage under improved control when φ' is equal to 0.8. The percentage of DC-link voltage variation is limited to 0.56% (0.225 V/45.28 V = 0.56%), and total harmonic distortion (THD) of the output voltage v_c is 0.22%.



Figure 8. Waveforms under improved modulation strategy.

Seen from the simulation results, the proposed modulation strategy can reduce DC-link voltage variation under the line frequency. Therefore, DC-link voltage v_d can remain relatively stable with a smaller capacitor. At the same time, the THD of improved output voltage drops significantly and the waveform is better.

Through (17) and (24) in the previous section, $I_c = I_c'$ can be attained when phase angle difference is equal to zero. At this point, it should be observed that the DC-link voltage fluctuations are equal under the line frequency cycle, regardless of which modulation strategy is adopted, as shown in Figure 9.



Figure 9. Capacitor voltage waveforms under traditional modulation strategy and improved modulation strategy when $\varphi = \varphi' = 0^{\circ}$.

Seen from the above figure, the voltage fluctuations of the DC side under the line frequency cycle are equal. Comparing the ripples under the switching cycle, clearly, the ripple under the traditional modulation strategy is larger than the ripple under the improved modulation strategy (the yellow envelope is thicker than the green one in the figure above), which demonstrates again the effectiveness of improved modulation strategy under switching period scale.

When only the DC-link capacitance C_d is changed, the DC-link ripple coefficient, amplitude and THD of output voltage under traditional modulation strategy and improved modulation strategy are shown in Tables 3 and 4.

	<i>C</i> _d (μF)	Ripple Coefficient (%)	<i>V_c</i> (V)	THD
1	20	8.99	34.24	0.78%
2	100	2.88	34.21	1.09%
3	200	3.04	34.33	1.50%
4	300	3.16	34.52	1.62%
5	400	2.86	34.66	1.51%
6	500	2.53	34.74	1.34%
7	600	2.01	34.79	1.21%

Table 3. Parameters under traditional modulation strategy.

Table 4. Parameters under improved modulation strategy.

	<i>C</i> _d (μF)	Ripple Coefficient (%)	<i>V_c</i> (V)	THD
1	20	4.26	34.01	0.13%
2	100	0.91	34.01	0.14%
3	200	0.51	34.03	0.20%
4	300	0.50	34.05	0.22%
5	400	0.44	34.07	0.22%
6	500	0.45	34.09	0.23%
7	600	0.53	34.09	0.39%

Figure 10 intuitively depicts the trends of ripple coefficient changing with C_d under two modulation strategies, respectively. As C_d increases, the DC-link voltage fluctuation should reduce. However, when the capacitor is small, DC-link voltage waveform under the line frequency cycle is mainly caused by the oscillation under the switching cycle. In fact, the magnitude of voltage fluctuation under the switching cycle still shows a decline trend.



Figure 10. DC voltage ripple coefficient under traditional and improved modulation strategies.

In order to further prove the theoretical analysis of the proposed converter, an experimental prototype is made in laboratory. Specifications of the prototype are the same as Table 2. The prototype block diagram, experimental setup, and the top-view of the proposed converter are shown in Figure 11a–c, respectively. Notice that the converter is operated in an open loop and the driving signal is generated by RCP and FPGA EP4CE10F17C8.



Figure 11. (a) Block diagram of the experimental system; (b) Experimental set up; (c) Top-view of prototype.

The switching control signals of the upper, middle, and lower switches on the same bridge arm generated by RCP and FPGA are shown in Figure 12.



Figure 12. Control signal of ST_1 , ST_2 , ST_3 : (a) traditional modulation strategy; (b) improved modulation strategy.



Figure 12 shows that the switch sequence is consistent with the theoretical analysis and simulation results. The final output waveforms are shown in Figure 13.

Figure 13. Output waveforms: (a) traditional modulation strategy; (b) improved modulation strategy.

Seen from Figure 13, the percentage of DC-link voltage variation is 3.49% (1.6 V/45.9 V = 3.49%) under the traditional modulation strategy while the percentage of DC-link voltage variation is 2.20% (1 V/45.4 V = 2.20%) with the improved modulation strategy.

Compared with the experimental results, the improved modulation strategy can reduce the DC-link voltage fluctuation greatly under the line frequency, which once again verifies the effectiveness of the proposed modulation strategy.

Fourier analysis of v_c under the traditional modulation strategy and the improved modulation strategy are shown in Figure 14a,b, respectively.



Figure 14. FFT Analysis of v_c : (a) traditional modulation strategy; (b) improved modulation strategy.

The THD of the output voltage under the traditional modulation strategy is 1.38%, and correspondingly, the value under the improved modulation strategy is 0.92%, which proves that the proposed modulation strategy can reduce the DC side voltage ripple coefficient under the line frequency, thereby improving the output voltage waveform.

When the phase angle φ equals to zero, according to theoretical derivation, the ripple coefficients under the traditional and improved modulation strategies should be equal. The experimental results are shown in Figure 15.

In Figure 15a,b, the position and spacing of cursors A and B are equal. It can be observed that the voltage fluctuations under the traditional and improved modulation strategies are almost the same (the delay of the controller itself cannot be ignored).

The stable operation of the system can be strictly ensured when the ripple coefficient is less than 2%. When the ripple factors under traditional strategy and improved strategy are both about 2%, the required DC-link capacitors are shown in Figure 16.



Figure 15. Capacitor voltage waveforms in line frequency cycle when $\varphi = 0^\circ$: (**a**) traditional modulation strategy; (**b**) improved modulation strategy.



Figure 16. The capacitance voltage waveforms when the voltage ripples are about 2%: (**a**) traditional modulation strategy; (**b**) improved modulation strategy.

It can be observed from Figure 16 that when the voltage ripple is about 2%, the sixswitch converter adopting the traditional modulation strategy requires capacitance value of 1800 μ F, while the improved one requires capacitance value of 500 μ F. The capacitance value is greatly reduced, and long-life film capacitors can be used to replace the large electrolytic capacitors to realize the electrolytic capacitor-less solution of the six-switch converter.

5. Conclusions

This paper presents an improved modulation strategy for a compact single-phase six-switch AC-AC converter which effectively reduces the number of switches. The proposed modulation strategy allows the six-switch converter to achieve 'fast charging and discharging' in a complete switching cycle. The energy on the DC-link capacitor obtained through the rectifier can be quickly output to the load through the inverter to achieve minimum energy storage. Therefore, under the same DC-link voltage ripple constraint, the capacitance value can be reduced and the system power density can be improved. Based on the time average modeling analysis, the effectiveness of the proposed strategy is fully proved in theory. Finally, the experimental results show that ripple factor drops to 2.20% from 3.49% while THD reduces from 1.38% to 0.92% under improved modulation strategy. The improved converter requires only one-third of the capacitance required by the traditional modulation strategy when the ripple factor is limited to 2%.

Under RL load, there may be different factors for inversion and rectification, the input power and output power will become synchronous and bring about twice frequency power in the DC-link capacitor. Next work will be focused on.

Author Contributions: Conceptualization, L.H.; Data curation, Q.T.; Formal analysis, Q.T.; Funding acquisition, L.H.; Investigation, Q.T.; Project administration, L.H.; Resources, L.H.; Software, Q.T.;

Validation, L.H.; Visualization, L.H.; Writing—original draft, Q.T.; Writing—review & editing, L.H. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Guangdong Province Natural Science Foundation under Grant 2021A1515011710, in part by the Natural Science Foundation of China under Grant 62071406 and in part by the Xiamen University Nanqiang Young Top Talents Program.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

References

- 1. Zhang, G. Research on DC/DC phase-shifted full-bridge converter system identification. J. Eng. 2018, 2018, 406–410. [CrossRef]
- He, L.; Cheng, C. A Bridge Modular Switched-Capacitor-Based Multilevel Inverter with Optimized SPWM Control Method And Enhanced Power-Decoupling Ability. *IEEE Trans. Ind. Electron.* 2018, 65, 6140–6149. [CrossRef]
- Vitorino, M.A.; Alves, L.F.S.; Wang, R.; Correa, M.B.D.R. Low-Frequency Power Decoupling in Single-Phase Applications: A Comprehensive Overview. *IEEE Trans. Power Electron.* 2017, *32*, 2892–2912. [CrossRef]
- 4. Alonso, J.M.; Calleja, A.J. High-power-factor light-emitting diode lamp power supply without electrolytic capacitors for high-pressure-sodium lamp retrofit applications. *IET Power Electron.* **2013**, *6*, 1502–1515. [CrossRef]
- Vasiladiotis, M.; Rufer, A. Dynamic Analysis and State Feedback Voltage Control of Single-Phase Active Rectifiers with DC-Link Resonant Filters. *IEEE Trans. Power Electron.* 2014, 29, 5620–5633. [CrossRef]
- Mellincovsky, M.; Yuhimenko, V.; Peretz, M.M.; Kuperman, A. Low-Frequency DC-Link Ripple Elimination in Power Converters With Reduced Capacitance by Multiresonant Direct Voltage Regulation. *IEEE Trans. Ind. Electron.* 2017, 64, 2015–2023. [CrossRef]
- Liu, X.; Li, H. An Electrolytic-Capacitor-Free Single-Phase High-Power Fuel Cell Converter with Direct Double-Frequency Ripple Current Control. *IEEE Trans. Ind. Appl.* 2014, 51, 297–308. [CrossRef]
- 8. Liu, J.; Tian, H.; Liang, G.; Zeng, J. A Bridgeless Electrolytic Capacitor-Free LED Driver Based on Series Resonant Converter with Constant Frequency Control. *IEEE Trans. Power Electron.* 2018, *34*, 2712–2725. [CrossRef]
- 9. Zhao, C.; Hu, Y.; Luan, K.; Xu, F.; Li, Z.; Wang, P.; Li, Y. Energy Storage Requirements Optimization of Full-Bridge MMC With Third-Order Harmonic Voltage Injection. *IEEE Trans. Power Electron.* **2019**, *34*, 11661–11678. [CrossRef]
- Hu, Y.; Zhang, X.; Mao, W.; Zhao, T.; Wang, F.; Dai, Z. An Optimized Third Harmonic Injection Method for Reducing DC-Link Voltage Fluctuation and Alleviating Power Imbalance of Three-Phase Cascaded H-Bridge Photovoltaic Inverter. *IEEE Trans. Ind. Electron.* 2019, 67, 2488–2498. [CrossRef]
- 11. Jana, S.; Srinivas, S. An Approach to Mitigate Line Frequency Harmonics in a Single-Phase PV-Micro inverter System. *IEEE Trans. Power Electron.* **2019**, *34*, 11521–11525. [CrossRef]
- 12. Zhang, F.; Ni, J.; Yu, Y. High Power Factor AC–DC LED Driver with Film Capacitors. *IEEE Trans. Power Electron.* 2012, 28, 4831–4840. [CrossRef]
- 13. Ming, W.; Zhong, Q.; Zhang, X. A Single-Phase Four-Switch Rectifier WITH Significantly Reduced Capacitance. *IEEE Trans. Power Electron.* **2016**, *31*, 1618–1632. [CrossRef]
- 14. Shan, Z.; Chen, X.; Jatskevich, J.; Tse, C.K. AC–DC LED Driver with an Additional Active Rectifier and a Unidirectional Auxiliary Circuit for AC Power Ripple Isolation. *IEEE Trans. Power Electron.* **2019**, *34*, 685–699. [CrossRef]
- 15. Nguyen, H.V.; Lee, D.-C. Reducing the dc-Link Capacitance: A Bridgeless PFC Boost Rectifier That Reduces the Second-Order Power Ripple at the dc Output. *IEEE Ind. Appl. Mag.* **2018**, *24*, 23–34. [CrossRef]
- 16. Zhu, G.-R.; Tan, S.-C.; Chen, Y.; Tse, C.K. Mitigation of Low-Frequency Current Ripple in Fuel-Cell Inverter Systems through Waveform Control. *IEEE Trans. Power Electron.* **2012**, *28*, 779–792. [CrossRef]
- 17. Kim, S.-M.; Won, I.J.; Kim, J.; Lee, K.-B. DC-Link Ripple Current Reduction Method for Three-Level Inverters with Optimal Switching Pattern. *IEEE Trans. Ind. Electron.* **2018**, *65*, 9204–9214. [CrossRef]
- 18. Zhong, Q.-C.; Ming, W.-L.; Cao, X.; Krstic, M. Control of Ripple Eliminators to Improve the Power Quality of DC Systems and Reduce the Usage of Electrolytic Capacitors. *IEEE Access* **2016**, *4*, 2177–2187. [CrossRef]