

Review

HVdc Circuit Breakers: Prospects and Challenges

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Abstract: The integration of offshore wind farms has revitalized the interest in multi-terminal high voltage direct current (M–HVdc) transmission grids. HVdc breakers' importance has increased as M–HVdc grids are now a commercial truth. Several HVdc circuit breaker technologies have been developed, published, and appeared as prototypes for HVdc networks. This paper summarizes the HVdc breaker technologies from the last two decades, distributed mainly in literature. A comparison of various state-of-the-art HVdc breakers is presented. Further, areas are identified where further research and development are required. The goal is to provide primary challenges and prospects in the HVdc breaker field.



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1. Introduction

The successful and reliable maneuver of multi-terminal high voltage direct current (M–HVdc) systems will impose the evolution of efficient dc grid protection and flexible control infrastructures. This will compel the power electronics and power systems operators to evolve appropriate protection schemes with HVdc breakers and control approaches to enhance the dc grid operation efficiency and reliability [1–3]. Since 1950, almost 200 point-to-point HVdc transmission grids have already been installed worldwide [4]. During the last two decades, few two-terminal HVdc applications have been evolved to acquire functional multi-terminal HVdc (M–HVdc) grids [5,6]. The M–HVdc systems consisting of multiple voltage source converters (VSCs) stations have become a promising solution because of recent development and the increased accessibility to high power VSCs from multiple vendors [6].

Considerable advantages and application ideas have been recognized and proposed regarding the M–HVdc system/grid [7–9]. The M–HVdc systems can serve as the most promising solution for integrating harvested offshore wind energy into ac mainland grids [10]. Several ideas for the European dc super grid have been scrutinized, like the European Wind Energy Association (EWEA) [11]. DESERTEC EUMENA's will develop co-operation between three continents; Europe, the Middle East, and North Africa. In [12–14], M–HVdc connections are proposed for DESERTEC and EWEA visions. The M–HVdc grid can also find its applications for the interconnection of multiple non-synchronous ac areas [15–17]. However, the main obstacle in realizing M–HVdc networks on a large scale is their high vulnerability to dc faults. The rising fault current rate is high because of

the small inductance, which demands fast interruption technology [18]. Thus, the recognition of the M–HVdc grid as a reliable and efficient network is forcefully subjected to the disposal of HVdc circuit breakers (DCCBs), making them one of the keys empowering technology [19–23].

There is a substantial difference between the needs and necessities of dc and ac breakers. Mainly because of the unavailability of natural zero crossings in dc systems. The DCCBs would interrupt dc fault currents swiftly and dissipate vast amounts of energy stored in the dc grid's inductances. Today, only transfer and load switches are in use for the HVdc applications. However, DCCBs are available for low and medium–range dc applications. HVdc CBs are not commonly available, or proposed DCCBs have minimal current breaking capability. Numerous DCCB designs have been proposed based on parallel and series connections of classical ac interrupters, charging units, semiconductors, resonance circuits, and varistors—each concept associated with certain drawbacks and advantages. Most of the ideas investigated only a single or few aspect of many design requirements, but no literature has given an overall picture.

The objective of this paper is to provide a comprehensive overview of HVdc circuit breaker technologies, including recent significant attempts in the development of modern HVdc circuit breakers, and, by this, to revive the discussion on this very topic. HVdc breakers from technology giants like ABB, Siemens, GE, etc. are assessed and a detailed performance–based comparison is provided, not available in the literature. Functional analysis of each technology is presented. Additionally, different technologies based on derived information from literature are compared. Finally, recommendations for the improvement of circuit breakers are presented.

2. High Voltage Direct Current Networks

The first commercial installation of HVdc transmission technology is seen in 1954 [24]. HVdc technology is not only feasible and attractive from a technical point of view but also is economical. Typically, HVdc systems are employed for two reasons: (i) To transfer bulk power over large distances via long transmission lines; (ii) to connect unsynchronized ac networks and networks operating at different frequencies (back–back). The dc transmission has low losses than ac for long transmission lines. Mainly, HVdc converter technology can be divided into two: Classical technology—Thyristors–based line commutated converters (LCC) and recent technology—insulated gate bipolar transistors (IGBTs)–based (self–commutated converters) voltage source converters (VSCs) [25–29].

Power flow in LCC–HVdc is regulated by adjusting the firing and extinction time of gate signals before commutation to the next valve, as the thyristor is only a turn–on device. The flow of power is unidirectional; thereby, LCC is sometimes called a current source converter (CSC) [30]. Thus, the change in power flow direction would be problematic, as it requires a polarity change. Reactive power (Q) is consumed at both inverter and rectifier sides, which has to supply via filters and extra capacitors from the ac side. The LCC–HVdc substation produces less than 1% losses at rated current, of which 50% comes from the converter station transformer [31]. However, LCC technology is continuously advancing (e.g., capacitor commutated conversion consumes relatively less reactive power [32,33]), and the filter size is also compromised by employing tuned active dc and ac filters [25,32–34]. The recently installed LCC–HVdc transmission links are provided in Table 1. LCC has the highest power and voltage rating in HVdc converter topologies, blocking voltage of 10 kV with a current rating up to 6250 A [35–37].

Constant dc–link voltage is obtained from self–commutated voltage source converters, where large capacitors are used. Real power (P) is transmitted softly in both directions and can provide reactive power at both receiving (inverters) and sending ends, which reduces the filter size considerably. Filter size is also reduced as only high–frequency harmonics are present because of pulse width modulation (PWM) due to the availability of high power IGBTs. However, a VSC station contributes to losses by 1.6% [31,38,39], of which 70% comes from converter valves. Five terminal VSC–HVdc Zhoushan link is installed in 2014

with ± 200 kV [38]. Each station's transmission capacity is 100, 400, 100, 300, and 100 MW, respectively. Details of some prominent VSC–HVdc transmission links are given in Table 2.

Table 1. Point–point LCC–HVdc transmission link.

Country	Project Name	Specifications			
		Year	Length (km)	Rating (MW)	Dc–Link (kV)
China	Jinpin Sunan	2012	2093	7200	± 800
Brazil	Rio Madeira	2013	2375	2×3150	± 600
India	Biswanath Agra	2014	1728	6000	± 800
China	Xiluodu Zhejiang	2014	1688	8000	± 800
China	Zhundong Sichuan	2015	2600	10,000	± 1100

Table 2. VSC–HVdc transmission systems.

Country	Project Name	Specifications			
		Year	Length (km)	Rating (MW)	Dc–Link (kV)
China	Nan'ao	2013	09 subsea	200	± 160
China	Dalian city	2013	43 subsea	1000	± 320
Namibia	Caprivi link	2010	951	300	± 350
Norway	Skagerrak 4	2014	244	700	± 500
France	Inelfe	2013	65	1000	± 320

In the event of dc fault, anti–parallel diodes to IGBTs start acting as an uncontrolled rectifier. A high rate of dc fault current is experienced due to the small dc inductance of the system. Furthermore, dc capacitors discharge and aid the fault current [40,41]. VSCs are no longer well–regulated, and thus the fault current is only restricted by the ac breakers [28]. Here, the DCCBs should be doing the same, but HVdc CBs are not available.

Table 3 summarizes the dissimilarities between LCC–HVdc and VSC–HVdc transmission technologies. Significant differences concerning the DCCB are; loss of VSC control in dc fault and different sizes of the inductances and capacitances (result in a different rate of rising dc fault current).

Table 3. An evaluation between VSC–HVdc and LCC–HVdc Transmission Systems.

Property	LCC–HVdc	VSC–HVdc
Basic building block	Thyristor	IGBT
Control of dc grid in the event of dc fault	Control phase angle	Converter control is lost due to diodes
Harmonics	Strong low order harmonics	Weak high order harmonics
P/Q	Unidirectional, consume a large amount of reactive power	Fully controlled P and Q in both directions
Available power ratings	800 kV, 6400 MW	400–800 MW, 300 kV
Power flow direction	Reversal of poles voltage	Stiff voltage achieved by adjusting PWM
Black start	No	Yes
The dc inductors	Large	Small
The dc capacitors	Small	Large
The dc fault current	The rate of increasing a fault current is low and controllable	The rate of growth of a fault current is very high and uncontrollable

VSC technology is rapidly advancing. New topologies are proposed to reduce converter losses ($<1\%$), harmonics contents, and capability to extinguish the dc fault current [40–45]. R. Marquardt proposed a multi–modular converter (MMC) topology, an advanced form of VSC–HVdc circuits [46,47]. This topology is based on the cascaded connections of several sub–modules of two IGBTs and a parallel capacitor. Sub–modules arrangements may use full–bridge (FB) or half–bridge (HB) cascaded connections. FB–MMC can override the overcurrent fault condition of HB–MMC. Thus, dc fault reverse blocking is

realized by blocking the flow of current through the switches during the dc fault [45,48,49] at the expense of high switching losses, which develops the need for fast-acting DCCB.

Most of today's HVdc interconnections are two terminals. A factual M–HVdc system consists of several onshore and offshore VSC's positioned in different topographical locations. Thus, control, operation, and energy management are more complex and challenging. In the event of dc fault, to ensure the reliable and smooth operation of M–HVdc systems, it must be possible to isolate the faulty portion/system from a healthy system. The ac breakers can interrupt full/complete short circuit current, while HVdc circuit breakers have only limited ratings. The DCCBs are expensive and larger than ac CBs of the same rating. Thus, new methods are developed to extinguish the fault from today's point–point dc–link based on; control [50] or by installing the ac CBs on the ac side to de–energize the system [51]. Such a protection scheme operation may take a few 100 ms [52–54] to a few seconds [53], but only suited to two terminals HVdc systems. De–energization of complete HVdc system is also suggested in [40,55–57] but limited to three to four terminals [58].

For reliable operation of the M–HVdc grid, the availability of dc circuit breakers would be vital. The first parallel M–HVdc system was anticipated, and a debate started in 1963 [59–61], whereas the series M–HVdc grid was discussed in 1965 [62]. However, major interest in M–HVdc emerges in 1980s [22,56,58], and [63–65].

More recent studies suggest VSC–based multi–terminal HVdc systems for integration of offshore wind farms [64–67]. Numerous challenges need to be dealt with before M–HVdc grid becomes a reality, which are: Communication between converter stations [64–68], control [69,70], and primary and back–up protection schemes [40–53,71–73].

It is challenging to decide unambiguously whether the HVdc link should be based on LCC or VSC as both technologies offer specific benefits and demerits. Table 4 gives the pros and cons of the M–HVdc grid based on LCC and VSC, respectively. LCC–HVdc is mature and well established and shows fewer losses. However, in the event of a fault on the ac side, commutation failure is experienced, leading to dc–link's ultimate devastation. Conversely, VSC–HVdc technology is vulnerable to dc faults, as explained earlier.

Table 4. Advantages and disadvantages of constructing an M–HVdc system based on LCC or VSC technology.

	Benefits	Demerits
LCC–HVdc	High power and voltage ratings Fewer losses Low rate of rising a fault current	dc–link collapse due to commutation failure Large consumption of reactive power Vulnerable to ac side faults
VSC–HVdc	Suitable for cables than overhead lines Soft power reversal No need for voltage polarity reversal Stiff dc–link voltage	Vulnerable to dc side faults The high rate of rising a fault current Higher losses Low power and voltage ratings

HVdc technology is principally vital for DCCBs as it defines the needs for HVdc CB, which could be different for both technologies. For instance, in VSC–based technology, CB needs to be fast and must have a capacity to interrupt high fault currents. The needs of the breaker for both technologies are discussed in the subsequent section.

3. HVdc Circuit Breakers

A neutral bus switch (NBS), ground return transfer breaker (GRTB), neutral bus ground switch (NBGS), high–speed bypass switch (HSBS) for parallel line switching, metal return transfer breaker (MRTB), and isolation switches [74,75] are the dc interrupters commonly used for various switching techniques in the present point–point topology of HVDC transmission networks. The dc interrupters have only been available in limited rating and number, which is merely approaching 1.6 times the nominal rating to interrupt the short circuit current. The maximum available rating is 500 kV, 4 kA, or 250 kV, 8 kA. In addition, dc breakers are comparatively expensive and bulky than ac breakers of the

same rating. So, initially ac breakers and isolators were employed on ac side of converters as substitute of dc breakers in point–point HVdc configuration [76]. In a medium or low voltage dc applications, various techniques based on solid–state switches or switching arcs have been developed to interrupt the short circuit current [73].

The major problem encountered in the development of DCCBs is the absence of the usual zero–crossing phenomenon in the dc system [77–79]. The basic requirements which must be accomplished by the breakers are;

1. Develop a zero–crossing current to interrupt the fault current
2. Must dissipate the stored energy of the inductance
3. Able to hold the voltage profile of the system after the interruption of fault current

The first two conditions form the dc circuit breaker basis, and the third particular attribute distinguishes them from ac breakers. Secondary requirements of the dc breaker in addition to the features mentioned above are as follows [80];

1. The dc breaker must interrupt the fault current, as mentioned earlier, in the VSC–based M–HVdc system.
2. The maximum voltage produced across the breaker must be within safe limits to coordinate with the system’s insulation. This is of prime importance when the system operates at a nominal voltage to switch heavy load currents.

Excessive developments and researches are being conducted on HVdc breakers from six decades [57–59], but interest in DCCBs is dropped significantly after 1985 due to no success in developing a fast and short interruption mechanism. However, new studies on DCCB appeared [80–83] recently boomed the interest in HVdc grids. Developments are made in technologies, which ultimately improve the DCCB design and configuration [84,85]. This paper focuses on the more recent dc breaker field developments, special attention to the latest VSC/MMC–based M–HVdc grids.

Distinctiveness of HVdc Breakers

DC limiting reactor is a major component of an HVdc circuit breaker. It is an inherently bulky element of the breaker that is expected to handle maximum dc fault current without getting itself damaged. When the limiting reactor is connected in an M–HVdc grid, the line impedance, as well as the grid stability is considerably affected. Moreover, an increase in transient voltage is observed at the breaker terminals. Apart from this, the fault current may face an initial rate of rising for both external as well as internal faults. The series impedance between the fault location and the converter is lower in an external fault as compared to an internal fault. Initially, for the first few milliseconds, an internal fault might give a higher fault current than an external fault. As for the protection of dc transmission lines, the external fault is considered outside of the protection zone defined by the dc reactor’s boundary. That is why, the impact of external fault is mitigated due to the inductor’s boundary effect and a smaller fault current is noticed under external fault as compared to an internal fault [86,87]. However, after several milliseconds of fault inception, due to lower series impedance, there will be a higher rise in the current level in case of an external fault than an internal fault. The HVdc breakers are designed to interrupt the fault current in the first few milliseconds only. An aggregated model of dc breaker is shown in Figure 1.

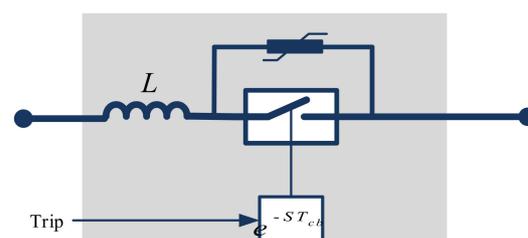


Figure 1. An aggregated model for the HVdc breaker.

4. HVdc Circuit Breaker Topologies

Three kinds of HVdc breakers are reviewed in this paper: Solid-state, electro-mechanical, and hybrid HVdc circuit breakers.

4.1. Electro-Mechanical HVdc Breakers

Electro-mechanical dc breakers are divided into active and passive resonance DCCBs as this type of breaker works on resonance phenomena.

4.1.1. Electro-Mechanical Passive Resonance HVdc Breakers

The passive DCCB is an obsolete technology that was developed for the LCC-HVDC system [88]. These breakers have a slow response time and are bulky, massive, larger in size, thus interest is dropped to use this breaker for dc grid protection. But these breakers have comparatively low power losses than all other dc breakers. A passive resonance DCCB is shown in Figure 2.

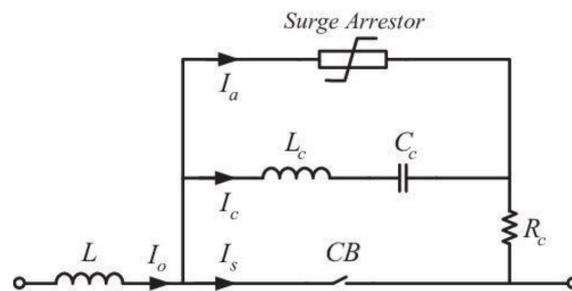


Figure 2. Electro-mechanical passive resonance HVdc breakers.

The nominal current path is shown in Figure 2. Rated current (I_s) flows through this path when the switch (CB) is closed under normal operation. Normally, interrupting circuits are developed with the air blast circuit breaker. Condition of zero-crossings is established with a series resonant circuit connected to an inductor and a capacitor, this forming a commutation path. This condition is necessary for breaker interruption [89]. Energy is absorbed by the surge arrester during the fault. The current oscillation between the nominal and the commutation path is enabled by the interruption. This interruption works at the natural frequency. When the amplitude of the oscillating current is greater than the input current, zero-crossings occur. At this stage, the switch stops the flow of current in the nominal path [18,74].

As a result, the capacitor will be charged by the flow of current (I_o). Consider the capacitor voltage exceeds a dc breaker’s voltage capability. Surge arrester will respond, an ideal zero point will be created on the decrease of current. This will help in the interruption of current. The maximum voltage value is 500 kV for passive electro-mechanical HVdc breakers, being employed for many years. This breaker clears the 5 kA fault current within a fault clearing time of 60–100 ms [90]. However, the development of semiconductor technology has reduced the attraction of electromechanical breakers for short circuit faults in multi-terminal HVdc systems [91].

The interruption process can be clearly understood by the analysis of the current equation. The differential equation during fault interruption is [89]:

$$L_c \frac{d^2 i_s}{dt^2} + \left(R_c + \frac{\partial u_{arc}}{\partial i_s} \right) \frac{d i_s}{dt} + \frac{1}{C_s} i_s = \frac{I_o}{C_c} \tag{1}$$

$$i_s = I_o \left(1 + e^{\frac{1}{2L} (R_c + \frac{\partial u_{arc}}{\partial i_s}) \cdot t} \cdot \sin \omega_c t \right) \tag{2}$$

where $\omega_c = \sqrt{\frac{1}{L_c \cdot C_c}}$ and if $R_c + \frac{\partial u_{arc}}{\partial i_s} < 0$; then “ i_s ” is oscillating with growing amplitude. In this scenario, the first zero-crossing of current would be enough for the breaker to interrupt the dc fault.

4.1.2. Electro-Mechanical Active Resonance HVdc Breakers

In this mode, a current oscillation supported by the pre-charged commutation capacitor C_c would increase instantly. It will rise to oppose the main CB's current when the current is commutated to the LC branch. This topology is also presented as a hybrid interruption technique. Typically, a thyristor is employed as a disconnecter and commutator in this type of breaker. This notion is also termed a two-stage interruption method. As this concept has various variants, the two main topologies are introduced in [92,93]. The first variant of electro-mechanical active resonance CB is depicted in Figure 3 [94,95].

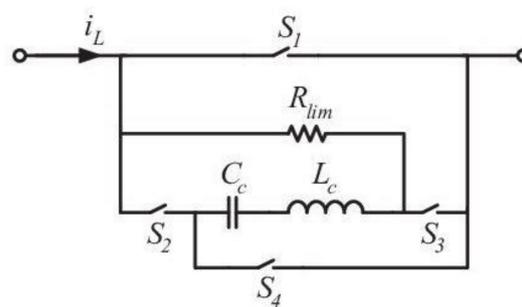


Figure 3. Electro-mechanical active resonance HVdc breakers: Variant-1 [89].

Under a steady-state condition in this first variant, the breaker switches S_2 , S_3 , and S_4 are open while the only main breaker switch S_1 is closed. The capacitor C_c is pre-charged with a negative initial voltage V_{c0} . When fault current is encountered, S_1 is opened, while S_2 and S_3 would close simultaneously. Then the fault current is opposed by the reverse current rising through the LC branch, and a zero-crossing will occur, and thus the current is commutated to parallel branches. Whence the C_c is charged, S_2 opens, and the current through it will reduce to zero. Subsequently, the switch S_4 will close, and discharging of C_c will happen in the loop C_c - S_4 - S_3 - L_c - C_c . When a current-zero happened in S_3 , it turns off, and the main breaker current again commutates into the loop R_{lim} - L_c - C_c - S_4 . However, S_4 opens upon current-zero creation, resulting in a new power equilibrium in which the capacitor is completely charged.

In the second variant of active resonance dc breakers, current interruption is realized by closing the switch S_3 only, as shown in Figure 4. When a fault is detected in the second variant, S_3 is closed, and S_1 is opened simultaneously to generate a current-zero in the main breaker. Eventually, S_3 will open when the capacitor is completely charged [94].

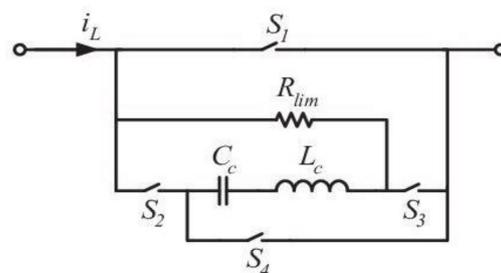


Figure 4. Electro-mechanical active resonance HVdc breakers: Variant-2 [89].

4.2. Solid State HVdc Breakers

The solid-state circuit breakers (SSCBs) are lighter, simpler to repair and maintain, and have a faster operating time than electro-mechanical dc breakers. SSCB is a dynamic era

of research and the latest contribution is presented in [96,97]. Two topologies of SSCB are implemented and summarized in [96]. In the first topology, CB is connected in parallel with a surge arrester, as shown in Figure 5. In contrast, in the second topology, a free-wheeling diode is connected, as shown in Figure 6.

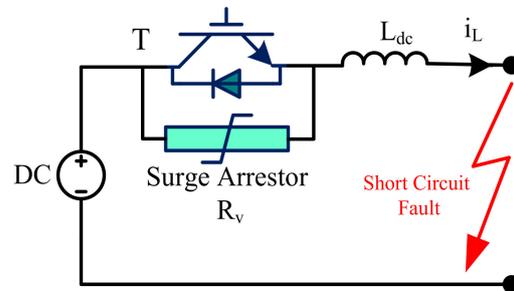


Figure 5. Solid-state HVdc breakers with parallel surge arrestors [95].

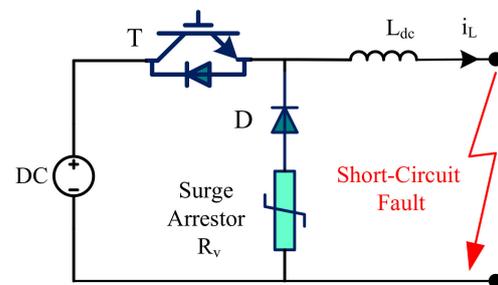


Figure 6. Solid-state HVdc breakers with free-wheeling diode [95].

4.2.1. Solid State HVdc Breakers Employing Surge Arrestors (SA)

Under the steady-state condition, the current flows from the dc source to the load through IGBTs (*T*) in SS-based HVdc breakers employing SA, as shown in Figure 5 [95,97]. However, the semiconductor switch turns-off when a fault is detected. This results in a rapid rise in voltage until the surge arrester starts to conduct. The surge arrester is designed so that any voltage greater than the grid voltage is choked/blocked, leading to the de-energization of the line inductance [97]. Then the load current is commutated to the surge arrester. The IGBT voltage is quite limited to the surge arrester’s clamping voltage and is assumed to be $V_{dc} + V_{margin}$. The impedance at the fault point is also supposed to be small when IGBT turns-off at time $t = 0$.

V_{margin} is applied across L_{dc} and the inductor current is calculated as [89]:

$$i_L = I_o - \frac{V_{Margin}}{L_{dc}} t \tag{3}$$

where I_o is the amplitude of the fault current at $t = 0$. The time to turn off the fault current T_{open} is derived as follows:

$$T_{open} = \frac{L_{dc}}{V_{margin}} I_o \tag{4}$$

The energy absorbed by the surge arrester can be given by:

$$W_R = \left(\frac{V_{dc}}{V_{margin}} + 1 \right) \frac{1}{2} L_{dc} I_o^2 \tag{5}$$

W_R is giving total energy being absorbed and suppressed by the surge arrester at the time of fault clearance, I_o^2 shows the short circuit current, and LC signifies the system’s

inductance. In a high voltage system, larger values of V_{dc} than V_{margin} are used to suppress the voltage across IGBT and reduce the conduction losses. In such a scenario, the term in the bracket of (5) becomes large which means W_R is enough higher than the stored energy in L_{dc} at $t = 0$, $\frac{1}{2}L_{dc}I_0^2$. Thus, surge arrester's high capacity is required to accommodate IGBT's more suppressed energy. The more is voltage suppressed across the IGBT, the higher the capacity surge arrester required [97].

4.2.2. Solid State HVdc Breakers Employing Free-Wheeling Diode

The second variant of SSCB employs a free-wheeling diode in parallel with the IGBT to bypass any reverse voltage impulse and protect the IGBT against the voltage spikes, as shown in Figure 6. A surge arrester is also used to absorb the dissipated heat during the fault. This quick action of dissipation and absorption of generated heat improves CB's reliability.

During normal operating conditions, IGBT (T) is on, and load current i_L passes through it. However, on fault detection at $t = 0$, the fault current is commutated to D as T turns-off. So, the inductance L_{dc} is gradually demagnetized by the R_v , thus the fault current starts reducing. If V_v expresses the clamping voltage of R_v , the surge voltage across T will be $V_{dc} + V_v$. As no power flow through T after turning off, thus energy absorbed in this breaker during turn-off operation is equal to $\frac{1}{2}L_{dc}I_0^2$. Thus, the energy W_R is:

$$W_R = \frac{1}{2}L_{dc}I_0^2 \quad (6)$$

Small values of W_R in (6) than (5) suggest the small rating and volume of surge arrester in the second topology with the reduced suppressed voltage across IGBT [94,95].

Several benefits are evolved for solid-state breakers compared to other circuit breaker technologies. The absence of mechanical structures improves the SSCB's response time, resulting in lower turn-off time. Additionally, the higher voltage across the inductor allows the demagnetization process to be performed faster [98]. The fast turn-off method of SSCB reduces the peak current to a limited level compared to other breaker technologies. Thus, the solid-state breaker has a lower power loss for the same grid voltage. Therefore, it may be assumed that an SSCB is an optimal choice due to lower turn-off time, reduced component cost, and lower peak current irrespective of cable length and grid voltage.

However, this is not the case because of one substantial shortcoming; the high on-state losses. It can be concluded from comparison graphs (grid voltage vs. time and grid voltage vs. maximum current) provided in [98,99] that for low to medium grid voltages, low turn-off time and low peak voltage are not quite enough to counter the power losses during the on-state. However, in high voltage grids, solid-state topology shows an advantage since the power saved per circuit breaker is sufficient to make them more economical than the other circuit breakers, even when the on-state losses are considered.

4.3. Hybrid HVdc Circuit Breakers

This type of circuit CB opens new prospects for fast switching and extinguishing the arc. They employ solid-state devices and mechanical switches for switching operations, as suggested by its name, hybrid dc breakers. The hybrid circuit breaker theory is suggested to overcome the shortcomings of solid-state and electro-mechanical breakers. The use of electronic components that are sensitive to short-circuit faults makes the hybrid DCCB expensive. The steady-state reliability of hybrid DCCB is fairly high, but the failure rate is much greater than that of a similar voltage rating of ac breaker. The structure of a hybrid dc breaker is very complicated as it contains electronic devices and mechanical components that lead to a high failure rate, and the electronic components are also comparatively fragile [100]. However, the breaker's failure to timely isolates the fault can be harmful to both human beings and the protected component. Hybrid DCCB continues to attract a lot of attention, as recently witnessed in [101]. Moreover, Alstom [102] and ABB [80] have established hybrid dc circuit breaker prototypes with significant enhancement in

recent research [103–105]. There are many available topologies of hybrid DCCB at various development stages, but only two attract more attention. Figure 7 shows the basic idea of hybrid DCCB [94,95]. The operation of hybrid CB is similar to that of SSCB but with the only difference that the hybrid breaker has additional sets of solid-state switches connected in parallel. Compared to other breakers, hybrid CB has low losses, and because of the solid-state switches, it is faster and reliable.

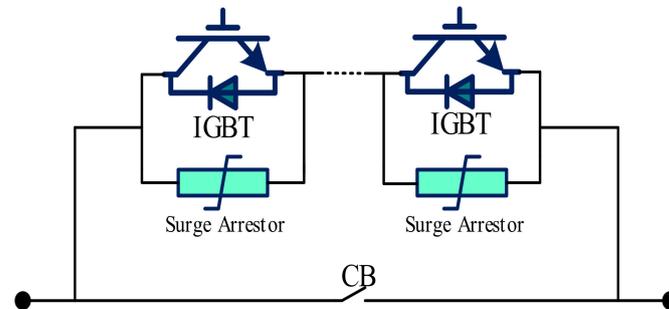


Figure 7. Hybrid HVdc breaker [89].

5. Comparison

A comparison of different dc breaker technologies in terms of power loss, current rating, voltage rating, and interruption time is presented in Table 5.

Table 5. Summary of comparison of various HVdc breaker technologies.

Types of CB	Interruption Time	Power Losses	Voltage Rating	Current Rating	Cost [105]	Maintenance	Life Span
Electro-mechanical	~60 ms	0.001%	Max. 550 kV	Up to 4–8 kA	High	Required—High	Longest
Solid state	<1 ms	30%	120–320 kV	16 kA	Low	Required—Low	Long
Hybrid	2–30 ms	0.1%	800 kV exp.	9–16 kA	Medium	Required—Medium	Longer

5.1. Interruption Time

Electro-mechanical dc breakers have a grumpy switching response up to 100 ms while the fault current interruption time of solid-state DCCB is less than 1 ms. However, hybrid dc breaker's operating time is, between the two topologies, 2–30 ms, an attractive attribute for high power systems applications [106–113].

5.2. Power Losses

Electro-mechanical and hybrid dc breakers with no semiconductor switch in the main current path show low power loss than all the topologies. The reason for this is the low voltage drop across the metal contacts of the main breaker. Even a hybrid dc breaker configuration having a low rating semiconductor switch in the main current path shows reasonable power loss, no more than 0.1% of VSC station power loss. On the contrary, solid-state dc breakers suffer from high power losses as the number of IGBT or other semiconductor switches is installed in the main current path, which is why relatively high voltage drop across the CB. Power loss for SSCB reaches up to 30% compared to the VSC station.

5.3. Voltage Rating

Electro-mechanical dc breakers of 550 kV voltage ratings are available, while hybrid DCCBs are tested experimentally for 120 kV. However, SS dc breakers are not available for high voltage applications, only been designed and executed for medium voltage levels. But SSCB of 800 kV voltage rating can be realizable by looking at the development in semiconductor devices [106–113].

5.4. Current Rating

Electro-mechanical breakers can interrupt up to 8 and 4 kA currents with active resonance and passive resonance circuits, respectively. On the other hand, the current interruption of 9 kA is experimentally proved for hybrid DCCB, while interruption of 16 kA is discussed in simulations [114]. Considering HVdc SSCBs, the current interruption rating of 5 kA is achievable.

6. More Recent Activities and HVdc Breaker Related Technologies

6.1. Combined Optimization of HVdc Breaker's Topology and Control

Most studies on M-HVdc system topologies and HVdc breakers only focus on a specific distinct aspect. Sometimes, it is assumed that the dc breaker is known, and the network controller is designed, while the system control activities are set; other times, as per the requirements of the DCCB, and the breaker is designed. No comprehensive combined efforts are reported in the literature to optimize the entire system. It is advised to regulate the control structure to ease the needs of the dc breakers. The rise of the dc short circuit current can be reduced by adding additional inductance to the VSC station's dc side, but it would slow down the system's normal operation. On the other hand, the dc short circuit current can also be limited by employing high grounding impedance for a line-to-ground fault. Focusing on just one aspect is most probable, not the best solution as only a collective optimization can only achieve the globally optimal solution. Multi-modular converters are an example of combined optimization [115–117]. The voltage level inside the valve is a fragment of the total dc-link voltage, and, in principle, it can be interrupted at these levels. Thus, the corresponding dc breaker has a lesser rated voltage, but the valve scheme needs to be remodeled to include a dc circuit breaker. Thus, the satisfying results may be achieved by the dc breaker and valve design's joint efforts.

6.2. Standardization

In the future, more than one manufacturer's components are expected to be used to design and build a multi-terminal HVdc grid. M-HVdc grid norms and standards are discussed in [118,119]. This is particularly important for the dc breakers and their interaction with the protection systems and networks [120].

6.3. Fault Current Limiters

Most of the concepts used to accomplish the basic requirements of dc breakers, as discussed earlier, are applicable to fault current limiters (FCL) in both dc and ac systems. FCLs are deployed to limit the fault current in power systems, as the name infers. Thus, FCL would increase the impedance of the system either self-triggered or externally triggered. Further, FCL has to handle a large amount of dissipated energy during the limitation. Additionally, some FCL can interrupt the fault currents. However, sometimes, a load break switch in series of FCL is placed to interrupt the fault current if alone FCL cannot do so. Interested readers are recommended to see the literature on FCL in [121,122], as no detailed discussion on FCL is repeated in this article.

Solid-state current limiters (SSFLs) [123,124], and hybrid FCL using fast mechanical switches [125] are two important topologies but both circuits have not been realized for high voltages so far. However, medium voltage FCLs (fuses) are self-triggered with interruption ability but are one-shot devices, need to replace manually, and widely available up to 10–20 kV [126,127]. Superconducting FCLs of resistive type use an intrinsic physical property of superconductors to lose its zero resistance above a critical current density. Such FCLs have low conduction losses, resettable and fast, but extensive cooling is required to acquire a superconducting state.

Mostly, FCLs are designed and deployed on distribution levels (36 kV). However, only resonance links and limiting reactors with capacitors are being used for high voltage applications; transmission and sub-transmission lines [122]. Researchers are working to

develop high voltage FCLS [128,129]. Any progress in this field would also benefit the HVdc breaker activities.

6.4. Testing, Only HVdc Breakers Are Tested So Far

The dc breaker, along with its auxiliary components, should be tested for functionality during development. Direct testing is not applicable for high power ratings; thus, synthetic testing techniques to be employed [130,131]. Contrary to ac breaker testing, the dc breaker strongly interacts with the dc-grid and requires actual energy levels to apply stress to the breaker properly. This is quite challenging, expensive, and leads to excessive heating (e.g., the energy dissipating elements). Specific test models have been designed and employed to test the components [132]. The individual component test can be performed and interpreted through power-hardware-in-the-loop methods. In this technique, only the component under consideration is the actual physical device, while all other parts are interfaced with the test object through a real-time simulator [133–136]. It could mean that the interaction of the DCCB with the network and the energy dissipation is simulated. The associated current through the dc breaker is calculated and driven by a flexible current source.

7. Available HVdc Breakers from Tech Giants

7.1. ABB's Hybrid HVdc Breaker

ABB proposed a hybrid dc breaker comprised of the main branch and an extra branch as shown in Figure 8 [136,137]. The control strategy for fault current interruption of this hybrid HVdc breaker is given in Figure 9 [138]. A shunt path is designed by an ultra-fast mechanical disconnecter in series with a semiconductor-based load commutation switch. This semiconductor-based dc breaker is divided into various units with independent arrester banks designed for rated current and voltage breaking capability. In contrast, the energy capability and lower voltage are matched by the load commutation switch. Residual current is interrupted by an isolating breaker after fault clearance, and the arrester bank of hybrid CB is protected from thermal overload by isolating the faulty line from the dc-grid [139].

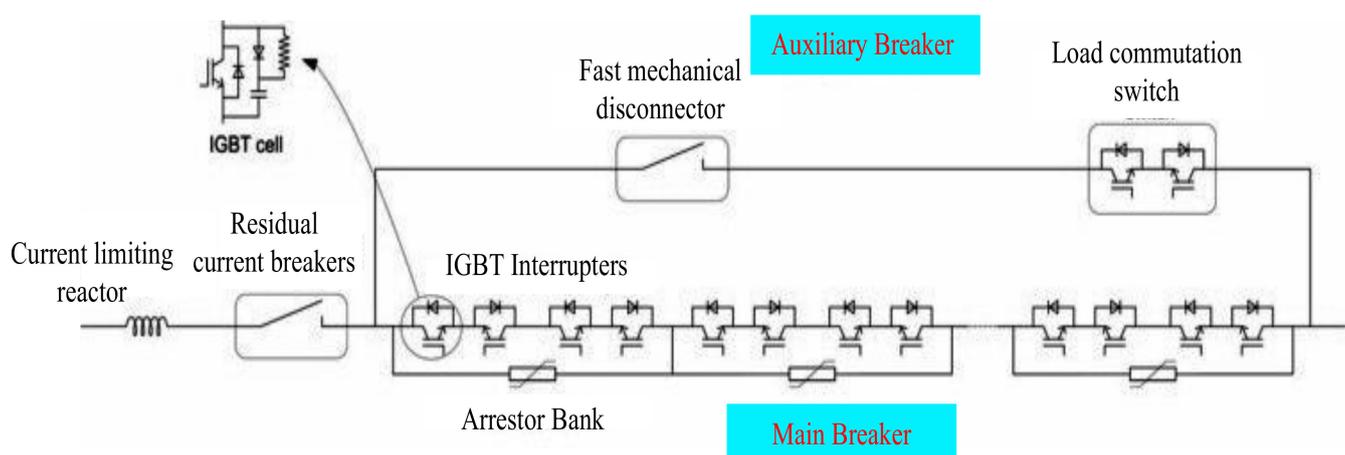


Figure 8. Proactive hybrid HVdc breaker, proposed by ABB [136].

During steady-state and normal operation, the current in the main breaker is zero, and the only path for the current is through the shunt. In case of dc fault, the load commutation switch instantaneously commutates the current to the main breaker, and the ultra-fast mechanical disconnecter opens. The main breaker interrupts the current with a mechanical disconnecter in an open condition.

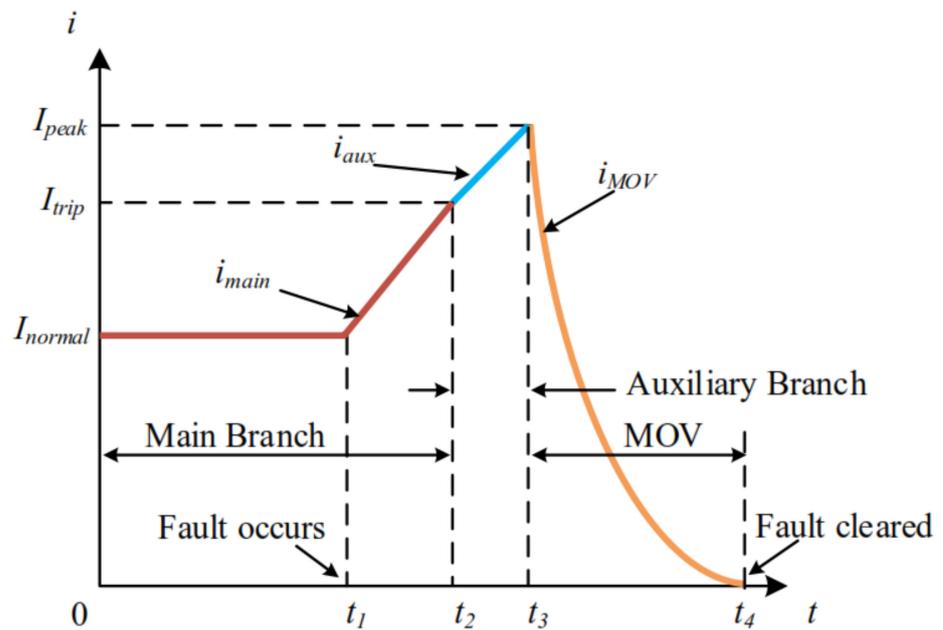


Figure 9. Control strategy for fault current interruption of hybrid HVdc Breaker, proposed by ABB [137].

7.2. Alstom’s Hybrid HVdc Breaker

A hybrid dc breaker from Alstom Grid is a combination of a semiconductor breaker and a mechanical HVdc switch. Figure 10 depicts the structure of this circuit breaker [102]. Besides mechanical contact, the core branch also includes a low voltage switch. Alstom dc breaker has two extra branches: (i) energy absorption and (ii) commutation branch (or arming branch). The control strategy for fault current interruption of this kind of hybrid breaker is shown in Figure 11.

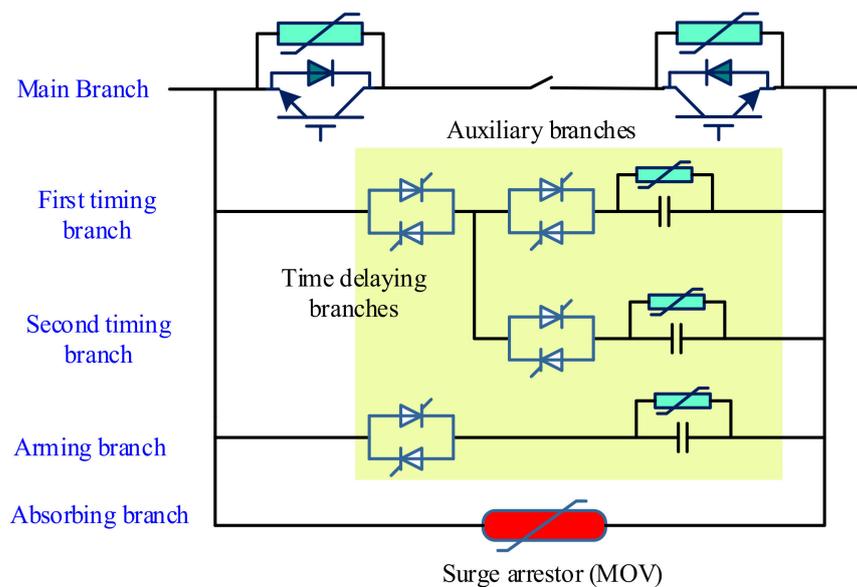


Figure 10. Hybrid HVdc breaker, proposed by Alstom grid [102].

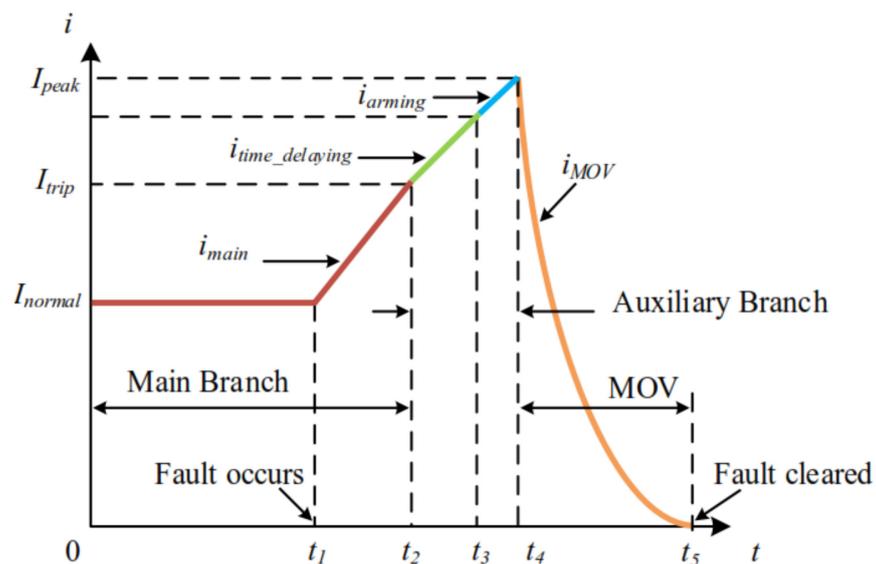


Figure 11. Control strategy for fault current interruption of hybrid HVdc Breaker, proposed by Alstom grid [137].

During steady-state and normal operation, the current will pass through the main branch. The low voltage switch produces low power losses and the contact voltage is also zero. Several components are connected in parallel for current rating and series for voltage rating. In the event of a fault, a huge amount of fault current will flow through the main branch. As soon as the fault is detected, the commutation branch will be closed, and the low voltage switch will be opened. Most of the fault current will commute through the commutation branch at this moment. The mechanical switch may open without any arcing across its terminals until the fault current flow through the main branch is mitigated to nearly zero. When the commutation branch is turned off, the fault current is forced to pass in the energy absorption unit. The voltage developed across the energy absorption unit must be larger than the source voltage to decrease the fault current and reduce the breakdown voltage of the mechanical switch. The total time to current extinction and the rate of fault current is determined by the difference of voltage developed across the energy absorption unit and the source in an inductive circuit [102].

7.3. General Electric's Superfast Medium Voltage HVdc Breaker/Switch

Existing dc circuit breakers developed for point-to-point applications are generally costly, too big, and too slow for use in a medium-voltage dc (MVdc) distribution grid. The energy department of Advanced Research Projects Agency-Energy (ARPA-E), United States recently awarded a research grant of \$5.8 M to a team of engineers at General Electric (GE) to develop a superfast MVdc breaker [140,141]. The GE research team proposes to use gas plasma to construct a superfast switch. Timothy Sommerer, the chief investigator on the ARPA-E grant, says a typical HVdc breaker requires an air-conditioned building, measures $10 \times 10 \times 25$ feet, and costs between \$5 M to \$10 M. A dc breaker made of power semiconductor switches commutates the current in a few milliseconds, which gives time to operate a main mechanical breaker. Such a topology would be very much expensive to set up an MVdc grid.

The GE research team is designing a breaker that uses plasma or charged gas to operate between the two electrodes. A small current flowing through a mesh wire employed within the two electrodes is used to operate the switch. Their goal is to build a dc breaker of rating 100 kV in the next three years, which is reflected as a boundary between high and medium dc voltage.

Plasma switches have the benefit of a smaller size. Semiconductor switches can also operate rapidly, but the cooling requirement demands more space to apart the switches

to stay cool. Hence, the equipment size increases. As plasma switches can work at very high temperatures, they can operate close together and adjusted in confined space of smaller footprints.

A comparison is provided in Table 6 of anticipating commercial HVdc breakers from Tech giants.

Table 6. Comparison of anticipating commercial HVdc breakers.

Type of CB	Alstom	ABB	GE
Size	Large	Medium	Reduced
Cooling	Required	Required	Not required
On-state losses	Low	High (0.01% of transmitted Power (>Alstom))	Reduced
Interruption speed	Medium	High (few ms > Alstom)	High
Auxiliary branch	Thyristor stacks in series with a capacitor	IGBT switch with ultra fast disconnecter	—
Cost	Lower for HVDC	Lower for MVDC	Reduced
Interruption capability	Uni-directional	Bi-directional	—
Suitability	High voltage dc/LCC	MVdc/VSC	MVdc

8. Summary and Future Research Needs

In the previous sections of this article, several technical areas were identified and discussed related to the HVdc breakers. Summary of the conversed literature and future research directions are discussed in the following [72]:

- i. Improvements in the existing dc breaker topology can be fetched by optimizing the size of components such as; inductors, capacitors, varistors, etc. The goal is to reduce interruption time, size, and cost.
- ii. The switching arc's oscillation growth and interruption capability can be optimized by studying the arc characteristics in detail under various vacuum and gas breaker conditions. Verification and derivation of the constraints are in mathematical arc models.
- iii. Comsol Multiphysics[®] simulations of dc arcs are recommended for high oscillatory current and during the interruption.
- iv. Medium-voltage dc breakers can be employed for high-voltage levels by enhancing the technology, series connections, or by smearing dc breakers across the medium-voltage levels in multilevel converter topologies.
- v. The use of hybrid dc breakers is recommended. As it can have features of both mechanical and solid-state breakers with reduced ratings of switches. Thus, size, cost, and interruption time are reduced.
- vi. Fast mechanical disconnectors with low on-state losses and high recovery of withstand voltage have sufficient arcing voltage for swift commutation. Such switches can be deployed in hybrid dc breakers for fast actions.
- vii. The use of new wide-bandgap power semiconductor devices (e.g., SiC or GaN) is recommended to have negligible on-state losses.
- viii. Active gate driving technologies that may improve the performance of semiconductor switches in a pure solid-state circuit breaker are recommended.
- ix. Integrated optimization of the whole M-HVdc system should be done to comply with the necessities of breaker-control protection.
- x. The standards and norms for the operation of multi-terminal HVdc systems must be defined to develop the proper dc-grid protection.
- xi. New testing methods for the dc breaker or its components should be designed. As dc breakers have strong network interaction, power-hardware-in-the-loop techniques would be advantageous.
- xii. GE Plasma switches that may operate at high temperature, more economical, and are adjusted in confined space of smaller footprints are recommended for medium dc voltage.

9. Conclusions

In this paper, prospects and challenges to HVdc breaker development are presented along with a review of the main concepts of HVdc breaker and different contenders. This topic has been evolved rapidly over the last two decades. The research and advancements in HVdc breaker technology certainly increase with the emergence of real-life multi-terminal HVdc grids. The best HVdc breaker candidate would have low cost, after achieving the required performance level.

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