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Capacitor Voltage Balancing with Online Controller Performance-Based Tuning for a Switch-Sharing-Based Multilevel Inverter

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Abstract: Switch-sharing-based multilevel inverters offer great advantages in terms of efficiency improvement and output quality enhancement for low-power photovoltaic (PV) applications. However, the capacitor voltage balancing issue may critically deteriorate the output voltages, and thus could nullify the aforementioned benefits. Hence, this paper proposes a capacitor voltage balancing solution based on a buck-boost converter with performance-based tuning controllers to address the issue. The proposed controllers are designed based on the proportional-integral (PI) configuration equipped with an online tuning mechanism. The main purpose of the online tuning mechanism is to fine tune the proportional gain according to the DC input voltage, based on the measured output current total harmonic distortion (THD) performance of the inverter, while at the same time preventing the controller from reaching a state of saturation. By using the actual measurement of current THD performance, online tuning accuracy can be improved since no ideal condition is assumed, and thus, the associated error can be minimized. Simulation and experimental results reveal that the capacitor voltages can be balanced at high modulation indexes with improved current harmonic performance able to be acquired at the inverter's output.

Keywords: buck-boost converter; capacitor voltage balancing; online tuning; switch-sharing-based multilevel inverter

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1. Introduction

Energy sustainability has gained increasing attention, which has brought about the reinforcement of numerous efforts to utilize renewable energy and improve energy efficiency. One of those efforts includes the application of multilevel inverters in solar PV systems. Multilevel inverters, which come from a family of power electronic converters, have the potential to play an important role. As the central component of a solar PV system, an inverter with high efficiency and good output quality is always favorable. In fact, the prospect of acquiring both high efficiency and high output quality would be better, especially when the inverter is of a multilevel type.

Since the last decades, the presence of multilevel inverters in various applications has grown tremendously as a result of their high power capability with increasing voltage levels [1]. There are at least three well-known classical multilevel inverters—diode-clamped multilevel inverters (DCMI), cascaded multilevel inverters and flying capacitor multilevel inverters [2–6]. These inverters offer several advantages in comparison to the traditional two-level inverters such as low THD and low electromagnetic interference (EMI) [4]. Owing to these advantages, they have been widely used not only in renewable energy systems but also in static compensators (STATCOM), variable speed motor drives, and high-voltage direct current transmission applications [7–11]. The circuit complexity of

a classical multilevel inverter typically increases as the number of levels increases. This contributes to reduction in the reliability as well as complicated control of the inverter. As a result, many new multilevel inverter topologies have been proposed [12,13] to overcome the problems encountered in the classical multilevel inverters, and one of them is the switch-sharing-based multilevel inverter.

Figure 1 presents the circuit topology of the three-phase five-level switch-sharing-based multilevel inverter [14]. The switch-sharing-based multilevel inverter is modified from the full-bridge configuration with a switch-sharing capability. The inverter offers advantages for low power solar PV applications including lower harmonic contents and enhanced output quality [15]. However, it has a shortcoming that is quite similar to that of the DCMI. The main problem is the unbalanced capacitor voltages at the DC-link, for voltage levels more than three [16]. This problem deteriorates as the number of levels increases. In a five-level switch-sharing-based multilevel inverter, four DC-link capacitors may experience unbalanced voltage across each of them when they are not charged and discharged accordingly. This voltage-drift phenomenon deteriorates the AC-side voltage waveforms and consequently results in an unsatisfactory performance. Therefore, finding a proper solution is paramount since this affects the operation and performance of the inverter.

Figure 1. Five-level switch-sharing-based multilevel inverter.

As for DCMI, there are two possible solutions that can be adopted to overcome the unbalanced voltage problem. One solution is via the modification of the pulsewidth modulation (PWM) switching pattern [17–21]. The switching pattern is normally selected from the redundant switching states. It is observed that many researchers prefer this method, so as to avoid extra cost since there is no additional circuit needed. However, the limitation of this method lies in the control complexity and the range of the modulation index allowed. Another solution is via the implementation of a voltage balancing circuit on the DC side of the inverter [22]. The use of the voltage balancing circuit based on a buck-boost converter is most commonly employed to balance the capacitor voltages [23,24]. A single-pulse control, which is regarded as one of the easiest methods, has been adopted. Multi-pulse control would also be another option when single-pulse control may seem inappropriate. Another auxiliary circuit is the three-level flying-capacitor-based chopper for a three-phase DCMI [25]. This circuit is well-recognized in reducing voltage stress across chopper switches and in improving reliability. Despite the advantages offered, the control philosophy of the chopper could become complicated and tedious owing to the high number of switches required. Meanwhile, [26] proposes a resonant switched-capacitor

converter (RSCC) for a new voltage balancing circuit with new phase shift control, in order to enhance the performance of voltage balancing. As compared to the buck-boost converter, RSCC can reduce the inductor to one tenth in volume. However, the increased number of switches used can be an issue. This would consequently turn the control system to a more complex capacitor voltage balancing scheme. In [27], a parallel switch-based chopper is proposed with the application of hysteresis control scheme. However, the main problem is the fact that additional components are needed, which would result in an increase in cost and circuit complexity.

Various control approaches have been proposed for the capacitor voltage balancing purpose. Among these approaches is the application of a fuzzy controller, model predictive controller and proportional-resonant controller. Fuzzy controller application with a self-tuning capability for capacitor voltage balancing has been revealed to be used with a PI controller to control DC bus voltage and capacitor unbalanced voltage in the three-level boost converter [28]. It is reported that the output capacitor balance voltage is guaranteed with a low quadratic error. In an input-series output-series (ISOS) modular DC-DC converter, a modified model predictive control (MPC) known as the duty cycle-based MPC (DC-MPC) has been proposed to address the capacitor voltage imbalance issue [29]. The difference between the proposed DC-MPC and the conventional MPC is the fact that the proposed DC-MPC optimizes duty cycles with a fixed switching frequency instead of employing optimized switching states with variable switching frequency. By predicting the effects on input voltage sharing (IVS) and output voltage sharing (OVS) of the constituent modules, the optimized duty cycles can be determined. With the optimized duty cycles, the proposed DC-MPC can quickly attempt to achieve IVS and OVS when imbalances exist among the input capacitor and output capacitor voltages of the ISOS converter. In another paper [30], the use of the quasi-proportional-resonant controller has been presented. The controller has been applied in an inter-arm balancing method that would guarantee an even distribution of capacitor voltages without affecting the input/output power quality.

As previously mentioned, the switch-sharing-based multilevel inverter would suffer from the capacitor voltage imbalance problem when no proper voltage balancing solution is put in place. Considering the fact that no such solutions have been properly presented for this type of multilevel inverter, to the best knowledge of the authors, it is the purpose of this paper to present a study on the capacitor voltage balancing solution based on an online tuning-controlled buck-boost converter for a five-level configuration of this type of multilevel inverter, taking into account the inverter's output performance.

The contributions of this paper can be summarized as follows:

- We propose a capacitor voltage balancing solution based on a buck-boost converter with performance-based-tuning controllers for a five-level switch-sharing-based inverter.
- The proposed controllers are based on the PI configuration that is integrated with an online tuning module to fine tune the proportional gain according to the DC input voltage.
- The online tuning mechanism uses the actual performance of the inverter based on the measured value of the output current THD to execute the tuning process.
- By using the actual measurement of current THD performance, online tuning accuracy can be improved since no ideal condition is assumed, and thus, the associated tuning error can be minimized.
- Both simulation and experimental results confirm that the proposed solution with the proposed controllers improve the step response and steady-state performances while ensuring the quality of the inverter's output current and the capacitor voltage ripples remain intact.
- Owing to the simplicity of the online tuning mechanism that is equipped in the proposed controllers, real-time implementation issues faced with other controllers such as high computational cost and infinite gain can be prevented, thus making the proposed solution attractive to fill in the gap for practical applications.

In Section 2, the details of the suggested voltage balancing circuit are described. Sections 3 and 4 present the proposed control strategy with an online tuning mechanism for the proposed PI controllers. Then, Sections 5 and 6 present the simulation studies of the controllers. Next, Section 7 discusses the experimental results and finally Section 8 provides the concluding remarks.

2. Two-Bidirectional Buck-Boost Converter for Capacitor Voltage Balancing

2.1. Capacitor Voltage Imbalance in a Five-Level Switch-Sharing-Based Multilevel Inverter

A topology of a three-phase five-level switch-sharing-based multilevel inverter is considered here and its circuit configuration is shown in Figure 1. It consists of 12 switches in which six bidirectional switches are used with four DC-link capacitors, wherein each capacitor voltage is equal to $V_{in}/4$. V_{in} is the total DC-link voltage across the four capacitors. To optimize the operation of bidirectional switches, each switch is shared among the three phases. In order to avoid a short circuit across the DC source, only one switch is allowed to be turned ON while the others are turned OFF. The details of the topology structure and operational principles of the inverter can be found in [14]. Due to unequal capacitance leakage currents and unequal delays in semiconductor devices, the inverter suffers from the capacitor voltage imbalance problem. In Figure 2, it can be observed that the outer capacitors (C_1 and C_4) continue to charge (i.e., V_1 and V_4 increase) and the inner capacitors (C_2 and C_3) continue to discharge (i.e., V_2 and V_3 decrease) when the DC source, V_{in} is set at 200 V and the modulation index is 0.9 during the period of no voltage balancing control in place. This will result in unbalanced voltages with a compromised quality to be observed in the inverter's output waveforms.

Figure 2. Unbalanced capacitor voltages in a five-level switch-sharing-based multilevel inverter when no voltage balancing control in place.

Considering that the switch-sharing-based multilevel inverter has some similarities to DCMI, it would be reasonable that somewhat similar solutions of capacitor voltage balancing in DCMI could be considered and applied in the switch-sharing-based multilevel

inverter. Since redundant switching states are not available for this inverter [14], modification of the PWM strategy is therefore not applicable. Hence, the proposed buck-boost converter is considered to serve the purpose of voltage balancing circuit in a five-level switch-sharing-based multilevel inverter. As mentioned in Section 1, the balancing circuit based on the parallel-switch-based chopper uses a smaller number of switches as compared to that of the buck-boost converter. However, a parallel-switch-based chopper is not suitable for the switch-sharing-based multilevel inverter since the simulation study shows that the chopper is not able to balance the capacitor voltages at high modulation indexes. Therefore, the buck-boost converter is considered for capacitor voltage balancing in the switch-sharing-based multilevel inverter.

2.2. Operation of the Buck-Boost Converter in Different Modes

In Figure 3, the circuit configuration of a two-bidirectional buck-boost converter proposed for capacitor voltage balancing in a five-level switch-sharing-based multilevel inverter is presented [24]. In general, the buck-boost converter circuit is the simplest topology, which requires four power switches (S_1 , S_2 , S_3 and S_4), and two inductors (L_1 and L_2) for connection to four DC-link capacitors (C_1 , C_2 , C_3 and C_4).

Figure 3. Different operating modes of the buck-boost converter. (a) Mode 1: (S_2 and S_3 ON, S_1 and S_4 OFF); (b) Mode 2: (S_1 and S_4 ON, S_2 and S_3 OFF); (c) Mode 3: (S_2 and S_4 ON, S_1 and S_3 OFF) and (d) Mode 4: (S_1 and S_3 ON, S_2 and S_4 OFF).

The circuit operates by transferring energy between the capacitors through the switches, inductors and diodes. In this work, the buck-boost converter circuit is divided into two separate parts which are the upper and the lower parts. The power switches in each part are switched ON or OFF in a complementary manner. This is to avoid a short circuit if all switches S_1 , S_2 , S_3 and S_4 are turned ON simultaneously. In the upper part of the circuit, S_1 and S_2 are complementary switches to allow energy transfer between capacitors C_1 and C_2 through diodes D_1 and D_2 and inductor L_1 . In the lower part of the circuit, S_3 and S_4 are also complementary switches. They are used to control the energy transfer between capacitors C_3 and C_4 through inductor L_2 and diodes D_3 and D_4 .

Figure 3 also presents different operating modes of the converter for charging and discharging the capacitors in both parts of the circuit. The paths of the current flow in all modes are shown in the figure. A controller controls switches S_1 , S_2 , S_3 , and S_4 accordingly so that four capacitor voltages can be equally balanced. Figure 3a shows that S_2 is turned ON to allow the charging of capacitor C_1 and the discharging of capacitor C_2 while S_1 is turned OFF. In the lower part of the circuit, S_3 is turned ON and S_4 is turned OFF so that capacitor C_4 is charging while capacitor C_3 is discharging.

As S_2 and S_3 are ON during mode 1, they will be OFF during mode 2. Capacitors C_2 and C_3 are starting to charge, while capacitors C_1 and C_4 automatically start to discharge. For mode 3, S_2 and S_4 are turned ON to allow the charging of capacitors C_1 and C_3 , and S_1 and S_3 are turned OFF as they are complementary to S_2 and S_4 . As a result, capacitor C_2 and C_4 are discharged. During mode 4, capacitors C_2 and C_4 will start charging when S_1 and S_3 are turned ON. Opposite to that, S_2 and S_4 are turned OFF to allow capacitors C_3 and C_1 to discharge. The processes of charging and discharging continue until the capacitors are fully charged and all the capacitor voltages are at their reference values.

3. Control Algorithm

The literature reveals that various controllers have been used for the purpose of capacitor voltage balancing. Examples include a fuzzy controller [28], model predictive controller [29] and proportional-resonant controller [30]. In this work, a PI controller is selected owing to its simple structure and robust performance that can be achieved in a wide range of operating conditions [31–33]. Another advantage is that the steady-state error can be reduced or eliminated altogether. Figure 4 presents the block diagram of the PI controllers. Four DC-link capacitors are connected between the converter and the inverter. The voltages across each of the capacitors are denoted by V_1 , V_2 , V_3 and V_4 . In order to achieve voltage balance, each capacitor is set to have a reference voltage of $V_{in}/4$. Since there are two separate parts in the converter circuit, two controllers are applied. Each PI controller is used to minimize the error between two capacitor voltages, which then leads to the derivation of the controller output. Here, $e_1(t)$ is the error obtained by subtracting V_2 from V_1 . Meanwhile, $e_2(t)$ is the error between two capacitor voltages, V_4 and V_3 . In the upper part of the circuit, upper proportional gain K_{pU} and upper integral gain K_{iU} are used to minimize $e_1(t)$, and for the lower part of the circuit, lower proportional gain K_{pL} and lower integral gain K_{iL} are used to minimize $e_2(t)$. Equations (1) and (2) define the controller outputs $y_U(t)$ and $y_L(t)$ for the upper and lower parts, respectively, which are obtained by summing the proportional and integral terms as follows:

$$y_U(t) = K_{pU}e_1(t) + K_{iU} \int e_1(t) dt \quad (1)$$

$$y_L(t) = K_{pL}e_2(t) + K_{iL} \int e_2(t) dt \quad (2)$$

Figure 4. Block diagram of the PI controller.

The power switches are switched ON or OFF based on the applied switching signals. Here, $y_U(t)$ and $y_L(t)$ are compared with the carrier signal in order to generate the switching signals or the gate signals as shown in Figure 4. The carrier waveform is generated according to certain frequency and amplitude so that the power switches can be properly switched ON or OFF. This is to ensure that the capacitor voltages are always directed to their respective references. The switching pattern depends on the need of either discharging or charging the capacitors. However, it is important to note that until there is an attainment of full charging of the capacitors, the discharging and charging processes would be continuously repeated.

4. Proposed PI Controllers with Online Tuning Mechanism

Assessment of each controller's performance is carried out under both the steady-state and dynamic conditions. For this purpose, a step change in V_{in} is introduced in order to investigate the controller's response. As an approach to improve this response, an online tuning mechanism has been suggested. A number of tuning methods have been proposed in the literature [34–36]. In this paper, a different tuning algorithm is proposed to add an online tuning feature to the PI controller. The proposed PI controller is basically modified based on the conventional PI controller described in Section 3. Two proposed PI controllers with the online tuning method are employed to control V_1 , V_2 , V_3 and V_4 , as portrayed in Figure 5. As compared to the conventional PI controller, the proposed PI controller consists of an additional component in its structure, which is the online tuning module. Here, V_{in} signal is required in the online tuning module, so that proper adjustment can be made according to the change in V_{in} . In this work, the tuning algorithm is designed to tune K_{pU} and K_{pL} . At the same time, K_{iU} and K_{iL} , and the anti-windup parameters for both parts remain unchanged. Then, $y_U(t)$ and $y_L(t)$ are compared with the carrier signal to produce the switching signals. As shown in Figure 5, the switching signals of S_1 and S_2 are complementary to each other. The same also goes for S_3 and S_4 .

Figure 6 presents the flowchart of the online tuning algorithm for the upper part of the buck-boost converter. Five equations are derived to generate a new K_{pU} . Derivation of these equations is made based on the correlation between K_{pU} and V_{in} that is established after a preliminary testing is carried out. In this testing phase, actual measurement of the output current THD of the inverter is used to build the aforementioned correlation so that tuning error due to the ideal-condition assumption can be minimized. Further details of the preliminary testing are provided in Section 7.

Figure 5. Block diagram of the proposed PI controllers with online tuning module. (a) Upper part of buck-boost converter. (b) Lower part of buck-boost converter.

Figure 6. Online tuning mechanism for the upper part of buck-boost converter.

Firstly, the present value of V_{in} is checked for whether it is similar to its previous value (stored in $V_{in,old}$). $V_{in,old}$ is updated to the present value if it is different from the previous value. The new K_{pU} is calculated based on the present value of V_{in} . Then, the previous value of K_{pU} , $K_{pU,old}$ is updated to the new K_{pU} . If V_{in} is between 0 V and 60 V, the new K_{pU} is calculated as below:

$$K_{pU} = 0.05 V_{in} - 1 \quad (3)$$

A new K_{pU} is constant at 2 if V_{in} is between 60 V and 80 V. If V_{in} is between 80 V and 100 V, the new K_{pU} is given by the equation below:

$$K_{pU} = 0.05 V_{in} - 2 \quad (4)$$

If V_{in} is between 100 V and 280 V, the new K_{pU} is constant at 3. The new K_{pU} is calculated as below if V_{in} is between 280 V and 300 V:

$$K_{pU} = -0.05 V_{in} + 17 \quad (5)$$

If V_{in} is the same as $V_{in,old}$, then K_{pU} is checked for whether it is within the allowable K_{pU} band. K_{pU} band is defined as the range between the maximum and minimum limits of K_{pU} . The reason K_{pU} must be within the defined range is to maintain capacitor voltages balanced while ensuring that the lowest output current THD can be achieved. If K_{pU} is higher than the maximum limit $K_{pU,high}$, the new K_{pU} is evaluated by the equation below:

$$K_{pU} = K_{pU,old} - 0.01 \quad (6)$$

Then, $K_{pU,old}$ is updated to the new value of K_{pU} . The same procedure applies for the case when K_{pU} is lower than the minimum limit $K_{pU,low}$. The new K_{pU} is calculated by increasing $K_{pU,old}$ as stated by the equation below:

$$K_{pU} = K_{pU,old} + 0.01 \quad (7)$$

These steps are repeated in the following iterations until K_{pU} lies within the K_{pU} band. For the case when V_{in} is the same as $V_{in,old}$ and K_{pU} is within the defined range, the controller will stop tuning. As for the lower part of the buck-boost converter, the tuning algorithm is presented in Figure 7. The flow of the tuning process for the lower part is the same as that of the upper part except for the different equations of K_{pL} . As previously stated, derivation of the equations is also based on the correlation between K_{pL} and V_{in} , resulting from the preliminary testing described in Section 7. There are five equations to calculate the new K_{pL} if V_{in} is not the same as $V_{in,old}$.

If V_{in} is between 0 V and 60 V, the new K_{pL} is calculated based on the equation below:

$$K_{pL} = 0.05 V_{in} - 1 \quad (8)$$

If V_{in} is between 60 V and 80 V, the new K_{pL} is updated at 2. The new K_{pL} is given by the equation below if V_{in} is between 80 V and 100 V.

$$K_{pL} = -0.05 V_{in} + 6 \quad (9)$$

K_{pL} is constant at 1 if V_{in} is between 100 V and 280 V. For V_{in} between 280 V and 300 V, new K_{pL} is calculated based on the equation below:

$$K_{pL} = 0.05 V_{in} - 13 \quad (10)$$

Then, $K_{pL,old}$ is updated to the new value of K_{pL} . For the case when V_{in} is similar to $V_{in,old}$, K_{pL} is checked for whether it is within the allowable K_{pL} band. If K_{pL} is higher than $K_{pL,high}$, K_{pL} is calculated by decreasing $K_{pL,old}$ by 0.01. The same step applies for the case when K_{pL} is lower than $K_{pL,low}$. The new K_{pL} is evaluated by increasing $K_{pL,old}$ by

0.01. Then, $K_{pL,old}$ is updated to the new K_{pL} . These steps continue until K_{pL} lies within the acceptable range.

Figure 7. Online tuning mechanism for the lower part of buck-boost converter.

5. Simulation Results

The simulation work was performed using MATLAB/SIMULINK in order to investigate the performance of the proposed and conventional PI controllers. A Y-connected RL load with $R = 120 \Omega$ and $L = 69 \text{ mH}$ was connected to the inverter. V_{in} was fixed at 200 V; thus, the reference voltage was 50 V (i.e., $V_{in}/4$), the inductors were set as $L_1 = L_2 = 12 \text{ mH}$, the capacitors were 2200 μF each, the modulation index used was 0.9 and the switching frequency was 5 kHz. The conventional PI controller is designed to have a constant K_{pU} and K_{pL} of 2, and a constant K_{iU} and K_{iL} of 0.001. The proposed PI controller has varying K_{pU} and K_{pL} that is tuned using the online tuning algorithm, while K_{iU} and K_{iL} are kept at 0.001. Step responses were investigated as a result of a change in V_{in} . This is to verify the effectiveness of the online tuning mechanism. V_{in} changes between 60 V and 200 V with a step response were set to occur at $t = 0.03 \text{ s}$. The time duration for the simulation was 0.1 s. The simulation results are presented in Figures 8 and 9 for without and with tuning, respectively. It can be seen that all capacitor voltages are able to be balanced even after a change in V_{in} . The inverter's output shows satisfactory results as the line-to-line voltage, V_{AB} , is able to produce nine voltage levels in the waveform. The output phase voltage, V_{AN} , and output current, I_A , indicate good results as well. It is observed that the capacitor voltage ripples with the application of the online tuning mechanism is estimated at 2 V, whereas the capacitor voltage ripples without online tuning is around 4 V. In addition, after V_{in} change, the output current THD is recorded to be lower when there is online tuning employed. The results show that only 3.09% THD when there is online tuning as compared to 3.42% for without online tuning. This verifies that the online tuning algorithm

contributes to the improvement made in the capacitor voltages ripples and the output current THD.

Figure 8. Simulation results without online tuning for a step response with V_{in} changes from 60 V to 200 V. (a) Capacitor voltages (V_1 , V_2 , V_3 , V_4) for step-up response. (b) Capacitor voltages (V_1 , V_2 , V_3 , V_4) for step-down response. (c) Line-to-line output voltage (V_{AB}), phase voltage (V_{AN}) and output current (I_A). (d) Output current harmonics.

(a)

(b)

(c)

(d)

Figure 9. Simulation results with online tuning for a step response with V_{in} changes from 60 V to 200 V. (a) Capacitor voltages (V_1 , V_2 , V_3 , V_4) for step-up response. (b) Capacitor voltages (V_1 , V_2 , V_3 , V_4) for step-down response. (c) Line-to-line output voltage (V_{AB}), phase voltage (V_{AN}) and output current (I_A). (d) Output current harmonic.

6. Analysis of Power Loss and Efficiency

Power loss and efficiency analysis is carried out in order to study the impact of the online tuning mechanism in reducing power loss, improving efficiency and contributing to a uniform distribution of power loss among switches. In order to properly evaluate the effectiveness of the tuning scheme, a comparison is made between the proposed PI controller and the conventional PI controller. Power loss is highlighted in the calculation of conduction loss and switching loss. In this analysis, the power switches chosen are IGBT model IRG4PC40UDPbF from International Rectifier. From the IGBT datasheet, relevant points are extracted to obtain several curves for the calculation of the losses. A MATLAB curve-fitting tool is used to derive the mathematical models for the IGBT as given below:

$$V_{CE} = 3.141e^{0.003496i(t)} - 2.296e^{-0.01392i(t)} \quad (11)$$

$$V_{FW} = 1.396e^{0.009157i(t)} - 0.5844e^{-0.1733i(t)} \quad (12)$$

$$E_{SL,IGBT} = 15.62(e^{0.009769i(t)} - e^{0.009764i(t)}) \quad (13)$$

Here, V_{FW} is the forward voltage drop, V_{CE} is the collector-to-emitter voltage, $E_{SL,IGBT}$ is the sum of the IGBT switching energy loss and $i(t)$ is the current flowing via the IGBT. In order to determine the conduction loss of the IGBT, the following equations are used:

$$P_{CL,Diode} = \frac{1}{T_{PO}} \int V_{FW} i(t) dt \quad (14)$$

$$P_{CL,IGBT} = \frac{1}{T_{PO}} \int V_{CE} i(t) dt \quad (15)$$

Here, $P_{CL,Diode}$ and $P_{CL,IGBT}$ are the conduction losses of diodes and IGBTs, respectively, and T_{PO} is the period for one cycle. The overall switching power loss of IGBTs, $P_{SL,IGBT}$ is given as follows:

$$P_{SL,IGBT} = \frac{1}{T_{PO}} \sum E_{SL,IGBT} \quad (16)$$

The switching loss of diode, $E_{SL,DIODE}$ is estimated by multiplying the reverse recovery time with the reverse recovery current as well as the reverse voltage drop resulting in:

$$E_{SL,DIODE} = (16.2e^{0.003252i(t)} - 10.4e^{-0.076497i(t)} - 1.815e^{-0.076441i(t)} + 1.166e^{-0.1562i(t)}) \times 10^{-6} \quad (17)$$

Consequently, the total switching power loss of diodes, $P_{SL,DIODE}$ is determined as below:

$$P_{SL,DIODE} = \frac{1}{T_{PO}} \sum E_{SL,DIODE} \quad (18)$$

The total power loss, P_L is the sum of conduction and switching losses, which is represented in the following:

$$P_L = P_{CL,DIODE} + P_{CL,IGBT} + P_{SL,DIODE} + P_{SL,IGBT} \quad (19)$$

The equation below is used to calculate the efficiency, η of the converter, in which P_O stands for the output power of the converter:

$$\eta = \frac{P_O}{P_O + P_L} \times 100\% \quad (20)$$

MATLAB/SIMULINK is utilized to conduct the power loss simulation with the same condition as presented in Section 5. Figure 10 displays the simulation results, which indicate that the higher the modulation index, then the higher the total power loss and efficiency become. The improvement in efficiency is contributed to the rise in the output

power, which is more than the increase in power loss. The highest power loss recorded for the proposed controller is 6.14 W at a modulation index of 1.0. This is lower than the power loss when the conventional controller is applied, namely 6.65 W that occurs at 0.9 modulation index. The highest efficiency achieved for the proposed controller is 96.9% at 1.0 modulation index, which is slightly higher than that when the conventional controller is employed. The distribution of the power loss among the power switches that are observed at 0.9 modulation index is shown in Figure 10c. The power loss for every power switch accounts for both conduction and switching losses of the IGBTs. With the application of the proposed controller, each switch records almost identical power loss compared to varying power loss which is observed when the conventional controller is used. In other words, uniform distribution of power loss among the switches can be successfully achieved with the use of the proposed controller.

Figure 10. Simulation results of power loss and efficiency with respect to modulation index. (a) Total power loss (b) Efficiency (c) Power distribution among the power switches at 0.9 modulation index.

7. Experimental Investigation

7.1. Hardware Setup

An experimental hardware setup has been built to validate the effectiveness of the voltage balancing circuit based on the buck-boost converter with the proposed controller. It basically consists of an inverter prototype, a buck-boost converter, load of RL type and a

single DC source as presented in Figures 11 and 12. Here, the PV source is represented by a single DC supply that provides V_{in} . Additionally, four DC-link capacitors are connected between the inverter and the converter, and each capacitor reference voltage is equal to $V_{in}/4$. The power circuit and the control unit are the two main parts in the hardware construction of the buck-boost converter. The main power circuit comprises the semiconductor power devices, dead band generators and gate drives. Four power switches (IGBT model IRG4PC40UD) are used. In order to prevent voltage surges during turning OFF, each IGBT is connected to an RC (resistive-capacitive) snubber. The value of the RC snubber used in this experiment is $10\ \Omega$ and $1\ \text{nF}$. To complete the power circuit, dead band generators and gate drives were added. The dead band generators produce a blanking time of $1\ \mu\text{s}$ to ensure that the power switches are not turned ON at the same time, thus avoiding a short circuit across the DC source. The gate drives provide isolation between the power circuit and the control unit for protection purposes, and also increase the voltage level of the switching signals to $+15\ \text{V}$ for the IGBTs to operate. To measure the voltages and currents for the control unit to use as inputs, voltage and current sensors of models LV25P and LA25-NP from LEM were used.

Figure 11. Block diagram of experimental setup for capacitor voltage balancing.

Figure 12. Photo of experimental setup to investigate capacitor voltage balancing performance.

The control unit is represented by the controller board eZdsp TMS320F2812. The control algorithm for the capacitor voltage balancing was implemented on a 32-bit fixed-point digital signal processor (DSP) for real-time application. The analogue-to-digital (ADC) module, event manager timers and general input/output ports are special features in eZdsp board, which are used for DSP programming.

To capture the results of the inverter output and capacitor voltages, oscilloscope is used. Table 1 shows the circuit components' values. The inverter load consisted of a three-phase load of 120 Ω and 69 mH per phase. The experiment was set at a modulation index of 0.9 so that nine voltage levels could be obtained in the line-to-line output voltage waveforms. A switching frequency of 5 kHz was applied.

Table 1. Values of circuit components.

Component	Values
DC-link capacitor	2200 μ F
Inductor of buck-boost converter	12 mH
R load	120 Ω
L load	69 mH

7.2. Results

The experiments are divided into two stages—preliminary testing and comparative testing. In the preliminary testing stage, experiments were conducted to derive the relationships between K_{pU} and V_{in} as well as K_{pL} and V_{in} for the online tuning module as described in Section 4. The selection of K_{pU} and K_{pL} was made in a manner that would balance the capacitor voltages at a given V_{in} that is adjusted between 0 V and 300 V. In order to carry out this selection, a trial-and-error method was adopted. This approach is preferred because it involves actual measurement of the output current THD using a power analyzer for a given V_{in} to derive the optimum values of K_{pU} and K_{pL} . The optimum values refer to K_{pU} and K_{pL} values that are associated with the lowest output current THD measured for every V_{in} . The use of actual measurement improves the accuracy and credibility of the K_{pU} and K_{pL} selected since no ideal condition is assumed, and thus, the error that is due to the assumptions and estimation made in an ideal condition can be minimized. In addition, when the optimum K_{pU} and K_{pL} are used, the controller is able to run at the optimum operating point, which in turn enables the best output performance of the inverter to be retained. This is critical since in most cases, changes in V_{in} would likely cause the controller to deviate from its optimum operating point since the reference voltages for the capacitors also change. As a result, the performance of the multilevel inverter may deteriorate. While the values of K_{pU} and K_{pL} are varied, the values of K_{iU} and K_{iL} are not required to be changed. This helps reduce complexity in the proposed tuning scheme. By using the MATLAB curve-fitting tool, the relationships between K_{pU} and V_{in} as well as K_{pL} and V_{in} are formed. Based on the established relationships, five equations are derived for K_{pU} in the upper part of the buck-boost converter at every V_{in} change between 0 V and 300 V, as explained in Section 4. A similar method applies to the lower part of the converter. Hence, with the application of online tuning mechanism, the proposed PI controller attempts to keep V_1 , V_2 , V_3 and V_4 balanced via the adjustment of the proportional gain only without modifying the integral gain and the anti-windup parameters.

In the comparative testing stage, the performance of the proposed controller and the conventional controller are analyzed and compared. Here, two experimental conditions have been assessed. In the first condition, experiments with the proposed controller were performed. On the other hand, the conventional controller was applied for the second condition. Similar parameters were used in both conditions, as displayed in Table 1. Figure 13 displays the step response and steady-state performances when the online tuning mechanism is applied. The results show that the proposed online tuning mechanism is able to maintain all capacitor voltages around their reference values between 15 V and 50 V when V_{in} changes between 60 V and 200 V. The rise time, peak time and settling

time are recorded as 6, 8 and 12 ms, respectively. For the step-down response, the fall time is measured as 6 ms. The percent overshoot is calculated as 6%. Figure 14c shows the harmonic content of the output current with a THD of 4.46%. V_{AB} , as presented in Figure 14a,b, displays that nine-level waveforms have been produced. Similarly, V_{AN} and I_A also reflect satisfactory performances.

In the second condition, the experiment without the tuning scheme was conducted. The conventional controller is designed with constant K_{pU} and K_{pL} as well as fixed K_{iU} and K_{iL} which are, respectively, 2 and 0.001, regardless of the change in V_{in} . For further examination of the controller's performance during the step response and steady-state condition, Figure 15 is provided as an illustration. The results show that all capacitor voltages are able to be kept around their respective references. The rise time, fall time, peak time and settling time are recorded as 9, 13, 12 and 200 ms, respectively.

The percent overshoot is calculated to be around 20%. THD of the output current is 4.92%, as displayed in Figure 16c. It can be noticed that these values are worse than those when the online tuning mechanism is applied.

Figure 13. Experimental results of the capacitor voltages (V_1 , V_2 , V_3 and V_4) with online tuning for a step response with V_{in} changes between 60 V and 200 V. (a) Step-up response (b) Steady-state condition (c) Step-down response.

Figure 14. Experimental results of inverter's waveforms (output current I_A , phase voltage V_{AN} , line-to-line voltage V_{AB} and input voltage V_{in}) with online tuning for a step response with V_{in} changes between 60 V and 200 V. (a) Step-up response, (b) step-down response, (c) output current harmonics.

Figure 15. Experimental results of the capacitor voltages (V_1 , V_2 , V_3 and V_4) without online tuning for a step response with V_{in} changes between 60 V and 200 V. (a) Step-up response, (b) steady-state condition, (c) step-down response.

Figure 16. Experimental results of inverter's waveforms (output current I_A , phase voltage V_{AN} , line-to-line voltage V_{AB} and input voltage V_{in}) without online tuning for a step response with V_{in} changes between 60 V and 200 V. (a) Step-up response, (b) step-down response, (c) output current harmonics.

7.3. Discussion of Main Results and Comparison with Other Control Strategies

The comparison between the simulation results and the experimental results by using the proposed online tuning mechanism are analyzed. Both results are compared in terms of the peak-to-peak capacitor voltage ripples, output current THD and rise time. For the peak-to-peak capacitor voltage ripples, the simulation result shows a value of 2 V while the experimental result indicates a value of 3 V. For the output current THD, the simulation result indicates 3.09% whereas the experimental result records 4.46%. The experimental result also reveals a higher rise time after a V_{in} change from 60 V to 200 V, namely, 6 ms, as compared with that of the simulation result, which is only 0.1 ms. Overall, the experimental results are observed to have higher readings in the peak-to-peak capacitor voltage ripples, output current THD and rise time as opposed to those of the simulation results. Nonetheless, this difference is expected since the simulation condition normally assumes an ideal case while the experimental condition takes into account various factors in a real environment such as external disturbances, instrument limitations and hardware constraints.

The experiment without the online tuning scheme shows that the capacitor voltage ripples are quite significant during the steady-state condition. Figure 15a,b show that the peak-to-peak capacitor voltage ripples reach up to 15 V. With the proposed online tuning method, the peak-to-peak capacitor voltage ripples are able to be reduced to 3 V, as shown in Figure 13a,b. Figure 16 also displays that without the online tuning mechanism, V_{AB} also takes the form of a nine-level waveform. I_A and V_{AN} also indicate satisfactory performances. The results show that the dynamic performance with the online tuning mechanism have been improved as compared with the results without tuning. The effectiveness of

the proposed PI controller with the proposed online tuning method has been validated through the improved performance achieved. At the same time, the inverter output shows satisfactory results, and the capacitor voltages are able to be balanced at the reference values with less ripples.

As stated in Section 1, various control approaches have been proposed for the purpose of capacitor voltage balancing. These include those that apply a fuzzy controller, model predictive controller and proportional-resonant controller. Despite the fact that these control approaches can also offer desirable solutions, there is still a concern with regard to the real-time implementation issue. The fuzzy controller and model predictive controller may suffer from high computational cost. As for the proportional-resonant controller, the need for infinite gain in order to perform well would lead to a difficulty for practical implementation. On the other hand, the proposed controller is based on the PI configuration and it is well-known that owing to its simplicity, the PI controller has been widely used in industrial applications. Although there is an online tuning module in the proposed controller's structure, the fact that the tuning mechanism is simple will not result in high computation. Hence, the proposed control strategy that employs the proposed controller is indeed attractive and practical for possible real-time implementation in industry.

8. Conclusions

This paper investigates the effectiveness of the proposed performance-based-tuning controllers for the buck-boost converter to balance the capacitor voltages of a five-level switch-sharing-based multilevel inverter. The buck-boost converter is chosen since it offers the simplest configuration, consisting of four power switches and two inductors, which are connected to four DC-link capacitors. In addition, the complexity of the control approach is considered low since the proposed online tuning mechanism is applied to the proportional gains without the need to adjust the integral gains. With the online tuning module incorporated in the controller's structure, the proposed PI controller is performed to improve the step response and steady-state performances while ensuring the quality of the inverter's output current and the capacitor voltage ripples remain intact. The simulation study shows that the proposed online tuning mechanism improves the quality of the output current, voltage ripples and efficiency as compared with those when no online tuning mechanism is applied. The highest efficiency is recorded at 96.9%, which is approximately 1.0% higher than the efficiency attained when no online tuning is employed. Two stages of the experimental investigation have been conducted to verify the efficacy of the proposed online tuning approach. In the preliminary testing stage, the online tuning mechanism that is based on the correlation between the proportional gains and the input voltage has been established considering the actual measured output current THD of the inverter. In the comparative testing stage, the performance of the controller with and without the proposed online tuning scheme has been evaluated. The experimental results reveal good improvement in terms of the dynamic and steady-state performances desired when the proposed tuning algorithm is applied. The capacitor voltages are able to be balanced satisfactorily with lower output current THD achieved at the inverter's output. Furthermore, capacitor voltage ripples are able to be reduced to 3 V as compared with the result without online tuning, which is 15 V. The rise time, fall time, peak time, settling time and percent overshoot also record encouraging results, denoting the superiority of the controller when the proposed online tuning module is integrated in the controller's structure. The fact that the online tuning mechanism is simple is a great advantage for real-time implementation. Ease of implementation is an important factor for practical application. Therefore, it can be concluded that better capacitor voltage balancing results and improved inverter output performances can be guaranteed via the application of the proposed tuning strategy, regardless of the change in the input voltage.

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