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The Demonstration of S²P (Serial-to-Parallel) Converter with Address Allocation Method Using 28 nm CMOS Technology

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Abstract: To improve the performance of analog, RF, and digital integrated circuits, the cutting-edge advanced CMOS technology has been widely utilized. We successfully designed and implemented a high-speed and low-power serial-to-parallel (S²P) converter for 5G applications based on the 28 nm CMOS technology. It can update data easily and quickly using the proposed address allocation method. To verify the performances, an embedded system (NI-FPGA) for fast clock generation on the evaluation board level was also used. The proposed S²P converter circuit shows extremely low power consumption of 28.1 uW at 0.91 V with a core die area of 60 × 60 μm² and operates successfully over a wide clock frequency range from 5 M to 40 MHz.

Keywords: serial to parallel converter; digital controller; embedded system; embedded hardware system; 5G; RF Front-End; low power; 28 nm CMOS; FPGA

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1. Introduction

As the 5G system demands broadband and high data rates, the system configuration becomes more complicated. A typical 5G system utilizes a multi-antenna MIMO structure for beamforming operation, and thus, it requires analog/digital control circuits to change the RF (radio frequency) gains and phases of multiple channels by compensating the performances with temperature and corner variations [1–3]. In general, it can be achieved by dynamic and static digital control circuits, respectively. The RF signal on a real-time basis is controllable through the dynamic digital control. Static case can help to find an optimal value through tuning work to increase the efficiency of the system. They have been implemented with advanced CMOS technology to enable fast operation with low power consumption that is strongly required especially for 5G systems application. Recently, it reaches the boundary of minimum utilized structure limitation, although the physical feature size scaling of CMOS transistor has been aggressively reduced. And the fabrication cost is still one of the critical problems. For this reason, many mm-wave circuits and systems are still being developed using sub-micron processes integrated with digital, analog, and RF block, which have cost advantages.

The 28 nm CMOS technology is a state-of-the-art process based on planar type MOSFET, and widely used in recent 5G/mm-wave systems because of the high transition frequency (F_t) and the low minimum noise figure (NF_{min}) performances. And a lot of researches is still being studied to optimize the CMOS process itself [1–18]. The previously reported papers, reducing circuit leakage by implementing high-K technology through a single-metal-gate fabrication for low power [4], power amplifier with a stacked technique with triple-well structures to overcome low voltage and transconductance, which are limited in circuit design [5], the bias optimization technique of transistor to overcome the limit of frequency maximum (F_{max}) [6], and low-noise amplifier with good performance using reduced noise

figure of CMOS process [7], were reported. In addition, the analog to digital converter (ADC) and digital to analog converter (DAC) circuit, which must operate digitizing signals with GHz-wide bands, must be designed by efficient structure or optimized circuit to avoid the increase in current consumption [8].

In digital control circuits for 5G applications, the power saving technique by sharing the common blocks according to operation mode is important. In more detail, in static digital control, a main design point is to reduce dc-current consumption using a simple control method to avoid massive analog connections [9]. The series-to-parallel (S²P) converter is as digital circuit that feed the input data serially, and read the output in parallel fashion. Thus, it has the advantage of being easily controlled by a simple circuit and leads to provide specific optimum condition to circuit [10]. For this reason, it is widely used in low-speed peripheral integrated circuits for data communications from a USB or a STAT hard disk driver including processors or microcontrollers [10]. Furthermore, it can also adapt to digitally controlled RFICs for finding optimum conditions, for examples variable capacitor bank to compensate the bandwidth according to process-voltage-temperature (PVT) variation in attenuation circuit of mm-wave systems, the fine-tuning circuit of voltage gain amplifier, phase shifter to reduce the mismatch effects, and transmitter and receiver module (TRM) control for array block [11–15].

In this paper, we firstly showed the successful demonstration of a series-to-parallel (S²P) converter circuit design using 28 nm CMOS process for 5G system that was capable of 160-bit control. To reduce power consumption, 160-bit consists of 20 bytes and each byte is directly assigned 20 address A [19:0] in our design. It helps to quickly update specific value corresponding to the desired address and can reduce unnecessary clock operation compared to the conventional S²P converter using data shifting method with the clock. In Section 2, in order to verify the excellence of nm-CMOS process we used, we check the performance change according to the length of the transistor in more detail. In Sections 3 and 4, the simulation results and measurement results will be shown along with the description of the proposed control circuit. And conclusions will be presented, finally.

2. 28 nm CMOS Technology Consideration

Nanoscale CMOS technology has the advantage of allowing high-frequency circuit design and low power operation due to the increase in the transition frequency (F_t). For analog and digital circuits, the transistor's F_t and low power characteristics are important factors in the design. Bandwidth and gain limiting characteristics, which are the performance degradation of analog circuits, are a difficult factor in designing an amplifier, and noise leads to many limitations in digital design. Of course, performance degradation due to intrinsic parasitic components of the transistor layout is large, but it can be overcome by scaling technology of CMOS to reduce parasitic components and operating voltage [16].

Figure 1 shows representative RF parameters such as F_t , F_{max} (maximum oscillation frequency), and NF_{min} (minimum noise figure) according to length of transistor. Here, the F_{max} in Figure 1a increases dramatically, and the F_t of 28 nm CMOS process has a high transient frequency of 142 GHz. For the same dc-current consumption of 8 μ A, NF_{min} decreases with the gate length scaling as shown in Figure 1b, due to the relationship of f/F_t where f means frequency of interest. The scaling CMOS technology improves the operation frequency due to the reduced bias and the scaling CMOS [16]. Therefore, nm-CMOS process is suitable for high-frequency RF circuits and high-speed digital circuits required for 5G system.

Figure 1. (a) The transient frequency (F_t) and maximum frequency (F_{max}), F_t and (b) minimum noise figure (NF_{min}) at 8 μ A current.

3. Proposed Serial to Parallel Converter

A general S²P circuit should have the same number of D-flip flop (D-FF) as the number of control outputs. Because it feeds the input data serially and reads the outputs in parallel fashion as shown in Figure 2a. It means that as the number of data increases, the number of clocks for operation also increases. Therefore, it is difficult to directly apply to a system that requires a lot of control, such as a 5G system, because it has unnecessary clock consumption and increase of dc power consumption, simultaneously. To improve this problem, the proposed S²P circuit was designed with minimum D-FF applied by allocating addresses per byte as depicted in Figure 2b.

Figure 2. Architecture of the conventional for 160-bit (a), proposed S²P converter (b), and flowchart for operation of proposed converter (c).

Figure 2b shows the proposed 160-bit S²P architecture, and the operation flowchart is as in Figure 2c. The first D-FF group, which receives the 8-bit data signal with clock, has the

same structure as a general 8-bit S²P converter. This D-FF has 4 input pins of data (D₁), reset (R₁), enable (E₁) and clock, and has an output (Q_A). After that, 8-bit data is output to the second D-FF group input along with the enable signal. This second D-FF also has data (D₂), reset (R₂), enable (E₂), clock, and address (A). This second D-FF outputs data to MUX-DEMUX block with one clock signal, and switches to the desired output byte according to allocated address signal.

After starting, confirming the data of the reset, S²P starts operating while receiving the data and the clock signal. After that, data is transmitted to the second D-FF through the enable signal, and the input enable signal is used as the enable signal of the second D-FF. At this time, the DEMUX of the input enable signal is switched to the enable signal of the second D-FF due to an additional enable signal, which generated by combination of input address signals. And then, data is output through MUX-DEMUX to desired output. Subsequent data updates are performed quickly in each sequence.

The proposed S²P converter can selectively update the desired output through the assigned address. The general converter requires 160 clock signals to update a desired output among 160-bit data. However, the proposed converter only needs 10 clocks per output byte without additional clock signal. This operation can reduce unnecessary clock operation of 150 bits, so it can be applied to a system requiring fast and low power.

Figure 3 shows the post-simulation results using cadence specter simulator. After reset, data of output address second O [1,7:0] and [1] bit of O [1,7:0] is input with 8 clock signals. At the ninth clock, the output (Q_A) of the first D-FF waits at the second D-FF input. Thereafter, at the 10th clock, the desired data is output and hold due to allocated address signal and enable.

Figure 3. The proposed S²P protocol of operating procedure.

The design proceeded with the IC digital circuit design method. Verilog code was verified using Modelsim simulation tool, and then DC compiler tool was used for synthesis. The layout was placed and routed using the IC compiler tool, and the timing issues were simulated and verified. The verification of the design includes the results of simulating timing issues using each worst corner model provided by the process company.

Figure 4 shows the chip layout in which place and routing (PNR) were performed include the process model. It was PNR using the IC compiler tool, and then layout was verified by layout and schematic comparison. The total chip was designed in an area of $990 \times 990 \mu\text{m}^2$, but it includes a buffer for measurement and pads for input/output pins. In addition, a $300\text{-}\Omega$ resistor was inserted into the buffer input for ESD protection. The proposed core S²P size was $60 \times 60 \mu\text{m}^2$, and integration is 85%.

Figure 4. The total chip layout with the S²P circuit.

Figure 5 shows the result of post-layout simulation. Output port O [1,1] updates the same output value according to the input data '10010010010010000'. The clock frequency is 40 MHz, and the designed S²P circuit works without issues.

Figure 5. The post-layout simulation result of the designed S²P circuit.

4. Implementation and Measurement Results

Figure 6 shows the measurement setup of the S²P chip. For the input signal, we used NI's USB-7845R FPGA and LabVIEW software, and the chip pad and PCB were connected via bond wires for evaluation. The power supply used Agilent's E3631A power supply and the output waveform was measured with a Tektronix's 4 channel oscilloscope.

Figure 7 shows the operating voltage according to input clock frequency. The operating voltage of S²P circuit was measured by 0.91 V at 40 MHz, 0.86 V at 30 MHz, and 0.82 V at 10 MHz and 5 MHz, respectively. As can be seen from the results, the circuit designed with a 1 V supply voltage worked well from 5 MHz to 40 MHz, and the power consumption reduced by 18% to 9%, respectively. The default current was measured by 30.9 μ A.

Figure 8 shows the measured waveform of oscilloscope equipment. The waveforms show only 4 waveforms that can verify operation due to the setup limitations of the equipment. Clock, reset, and enable signal are inputted. Based on the input of the address, the output waveform of address O [1,1] shows a normal output value at a clock frequency of 5 MHz to 40 MHz. The output O [1,1] value changes according to the input data '10010010010010000'. However, the output results at 20 MHz and 40 MHz do not seem to sufficiently reflect the input data at high operating frequencies, but the designed S²P circuit output does not contain a sufficient size drive buffer for the bond-wire, PCB,

and measurement probe capacitance. Therefore, it is difficult to represent accurate measurement results. However, the proposed S^2P circuit is integration with circuit requiring control, and it does not affect the actual operation.

Figure 6. The measurement setup and chip-photograph.

Figure 7. Operating voltage according to clock frequency.

Figure 8. The measurement results at 1 V supply with 5 MHz to 40 MHz clock frequency.

5. Conclusions

This paper firstly presents a successful demonstration of low power 28 nm CMOS serial-to-parallel converter applicable to 5G systems. The proposed circuit can reduce unnecessary clock signals to update time of data by applying the method of assigning addresses to the outputs. The proposed circuit has a power consumption of 28.1 μ W at 0.91 V and a maximum operating clock rate of 40 MHz. The core die area is $60 \times 60 \mu\text{m}^2$, contains 160 control bits, and is expected to be used efficiently in 5G systems.

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