


Article

Fermi-Level Pinning Mechanism in MoS₂ Field-Effect Transistors Developed by Thermionic Emission Theory

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Abstract: Molybdenum disulfide (MoS₂) field-effect transistors (FETs) with four different metallic electrodes (Au, Ag, Al, Cu) of drain-source were fabricated by mechanical exfoliation and vacuum evaporation methods. The mobilities of the devices were (Au) 21.01, (Ag) 23.15, (Al) 5.35 and (Cu) 40.52 cm²/Vs, respectively. Unpredictably, the on-state currents of four devices were of the same order of magnitude with no obvious difference. For clarifying this phenomenon, we calculated the Schottky barrier height (SBH) of the four metal–semiconductor contacts by thermionic emission theory and confirmed the existence of Fermi-level pinning (FLP). We suppose the FLP may be caused by surface states of the semiconductor produced from crystal defects.

Keywords: fermi-level pinning; MoS₂; field-effect transistors; thermionic emission theory

1. Introduction

Two-dimensional (2D) materials have attracted great attention with the birth of graphene in 2004 [1]. 2D materials are planar materials with atomic thickness [2]. They have excellent electrical properties, outstanding flexibility and good transparency [3,4]. These new physical properties can meet the needs of different applications such as electronics, photo electricity, energy storage and conversion [5]. In recent years, the transition metal dichalcogenides (TMDs), as an important part of 2D materials, have attracted great interest due to their various electrical properties including metal [6], semi-conducting [7], superconducting [8], charge density wave [9] and so on.

Molybdenum disulfide (MoS₂) is a typical material of TMDs. It is one of the most promising candidates to be the semiconductor of the next generation [5]. MoS₂ has a direct bandgap of 1.8 eV, which is suitable for developing field-effect transistors (FETs) with low static power consumption and high carrier mobility [10]. In the past decade, studies around MoS₂-FET were focused on devices preparation [11], electrode contact [12], hysteresis phenomenon [13], heterojunction structure [14], material modification [15], and so on. However, the research on the comparison of different typical electrode materials in MoS₂-FET are relatively rare.

In this paper, we prepared MoS₂ materials through a classical mechanical exfoliation method [1], fabricated the devices with different metallic electrodes, and characterized them subsequently. We found that the on-state currents of four devices were of the same order of magnitude with no obvious difference. In order to clarify the internal mechanism, we calculated the Schottky barrier height (SBH) of the four

metal–semiconductor contacts by thermionic emission theory and discovered that there may exist Fermi-level pinning (FLP) between the contacts in four devices [16].

2. Experiment

MoS₂ materials were purchased from a 2D semiconductors company. We exfoliated MoS₂ flakes with 3M Scotch tapes pasting for several times. Then, a substrate of n-type silicon wafer with 300 nm-thick silicon oxide was prepared. It was cleaned with acetone (for 20 min) and isopropanol (for 20 min) by ultrasonic. Then, the MoS₂ flake was transferred to the substrate by 3M Scotch tapes. Next, the substrate covered with MoS₂ was sent to the vacuum chamber. The first electrode material of Au was evaporated in the chamber through a shadow mask with 50 μ m length channel. The fabrication process and structure of FET devices are shown in Figures 1 and 2, respectively. Three other materials of Ag, Al and Cu were used as electrodes in the other three devices fabricated by the process mentioned above. Finally, four FET devices were prepared. The micro-images of the devices were obtained by optical microscope (LEICA DM 2700M), as shown in Figure 3a–d. The electrical properties of the devices were characterized by semiconductor characterization analyzer (Keithley 4200).

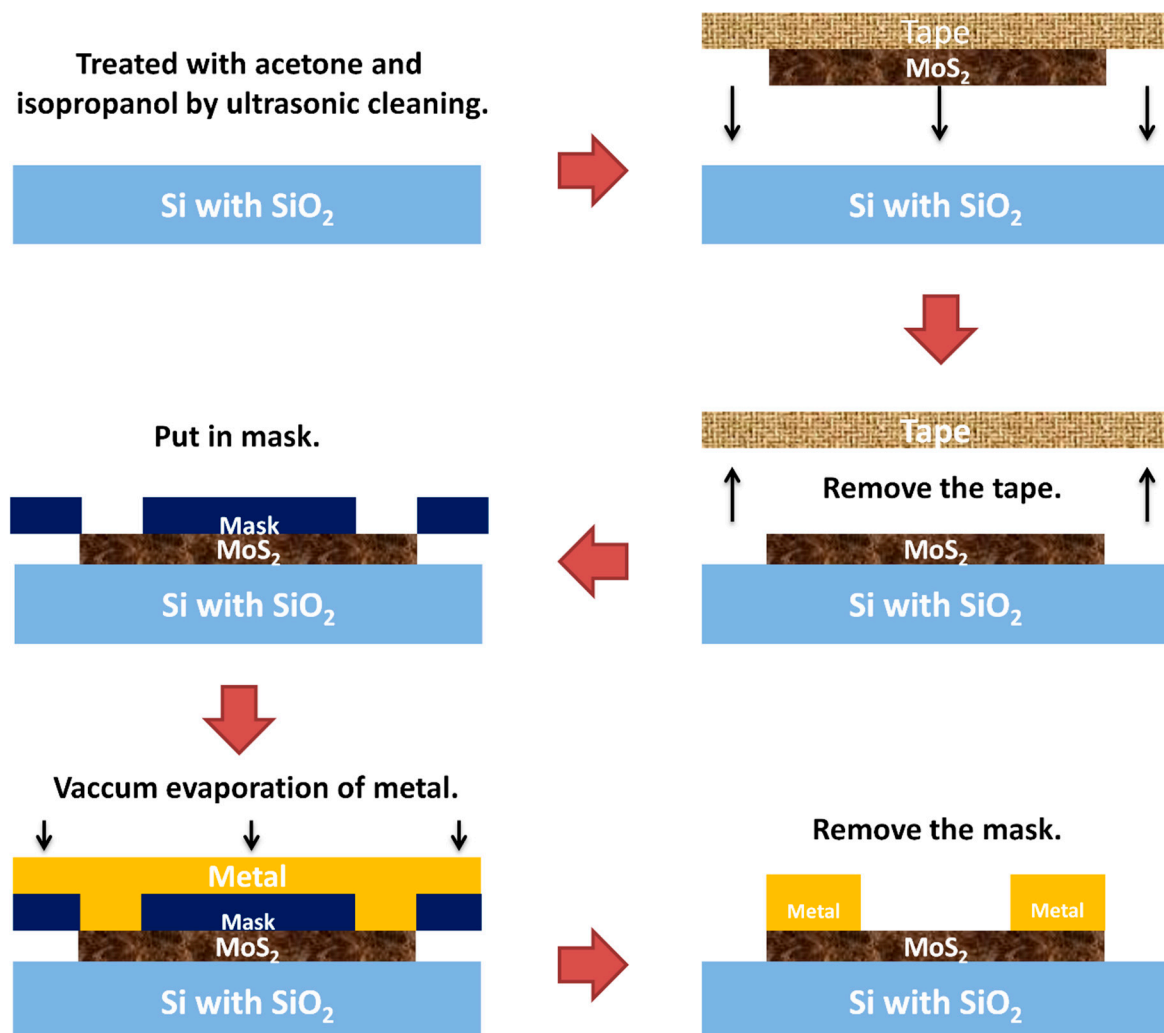


Figure 1. Fabrication process of field-effect transistor (FET) devices.

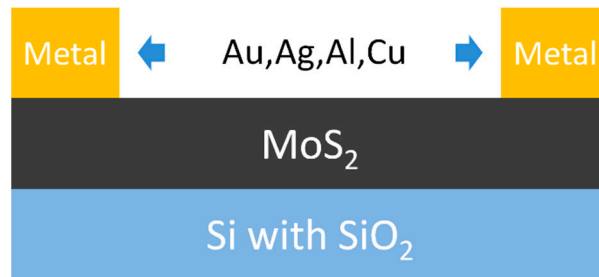


Figure 2. Molybdenum disulfide (MoS_2) FET devices structure.

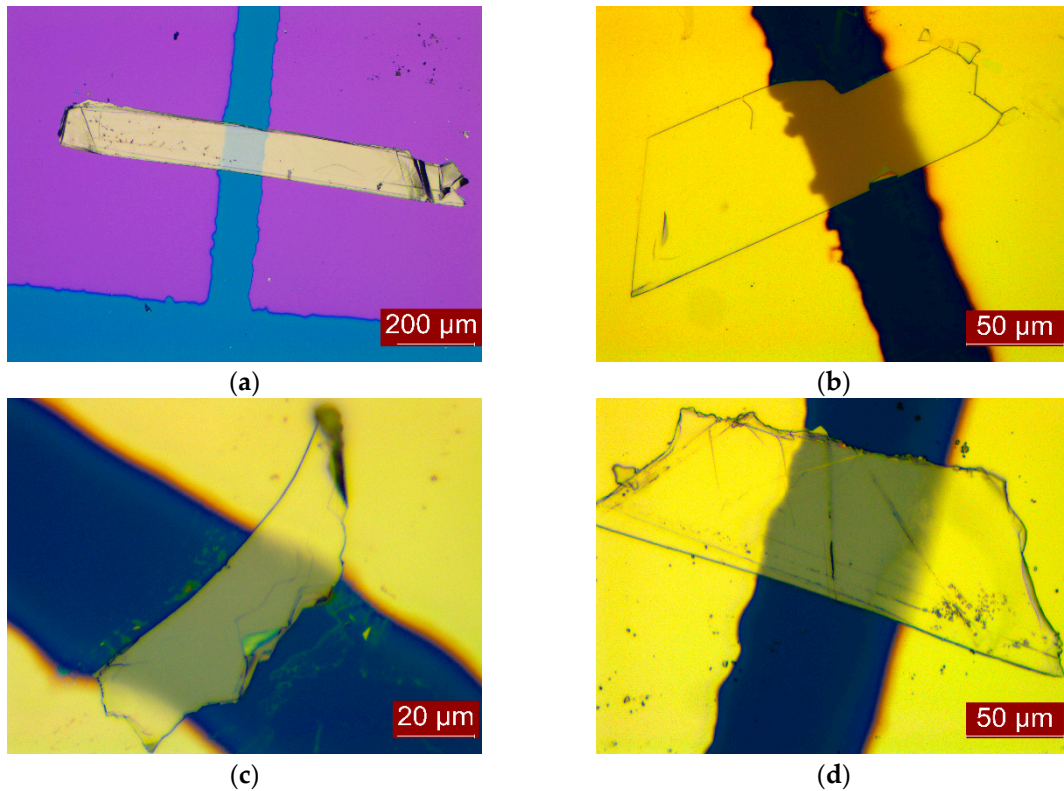


Figure 3. Microscope images of FET devices with the electrode of (a) Au; (b) Ag; (c) Al; (d) Cu.

3. Results and Discussion

The output and transfer curves of the devices with four types of metallic electrodes are shown in Figure 4. We can find that the devices are n-type depletion FETs as the current appeared in the negative coordinates in the transfer curve with the drain-source voltage of 10 V, 20 V and 30 V, as shown in Figure 4e–h. This result is consistent with previous studies. Meanwhile, we obtained the on/off ratio, threshold voltage (V_{th}) from the curves and calculated the carrier mobility [15] through the Equation (1). Where W denotes the channel width, L denotes channel length, C_i stands for the capacitance per unit area of silicon oxide.

$$\mu_{carrier} = \frac{W}{L} C_i V_{DS} I_{DS} (V_{GS} - V_{th}) \quad (1)$$

The characteristics of the devices are as shown in Table 1. We can find that the device with silver electrode has the relative ideal performance with a carrier mobility of $23.15 \text{ cm}^2/\text{Vs}$, the largest on/off ratio of 1.23×10^4 and the lowest threshold voltage of 2.21 V. This phenomenon may attributed to the fact that the work function of silver (4.26 eV) is close to the conduction band of molybdenum disulfide.

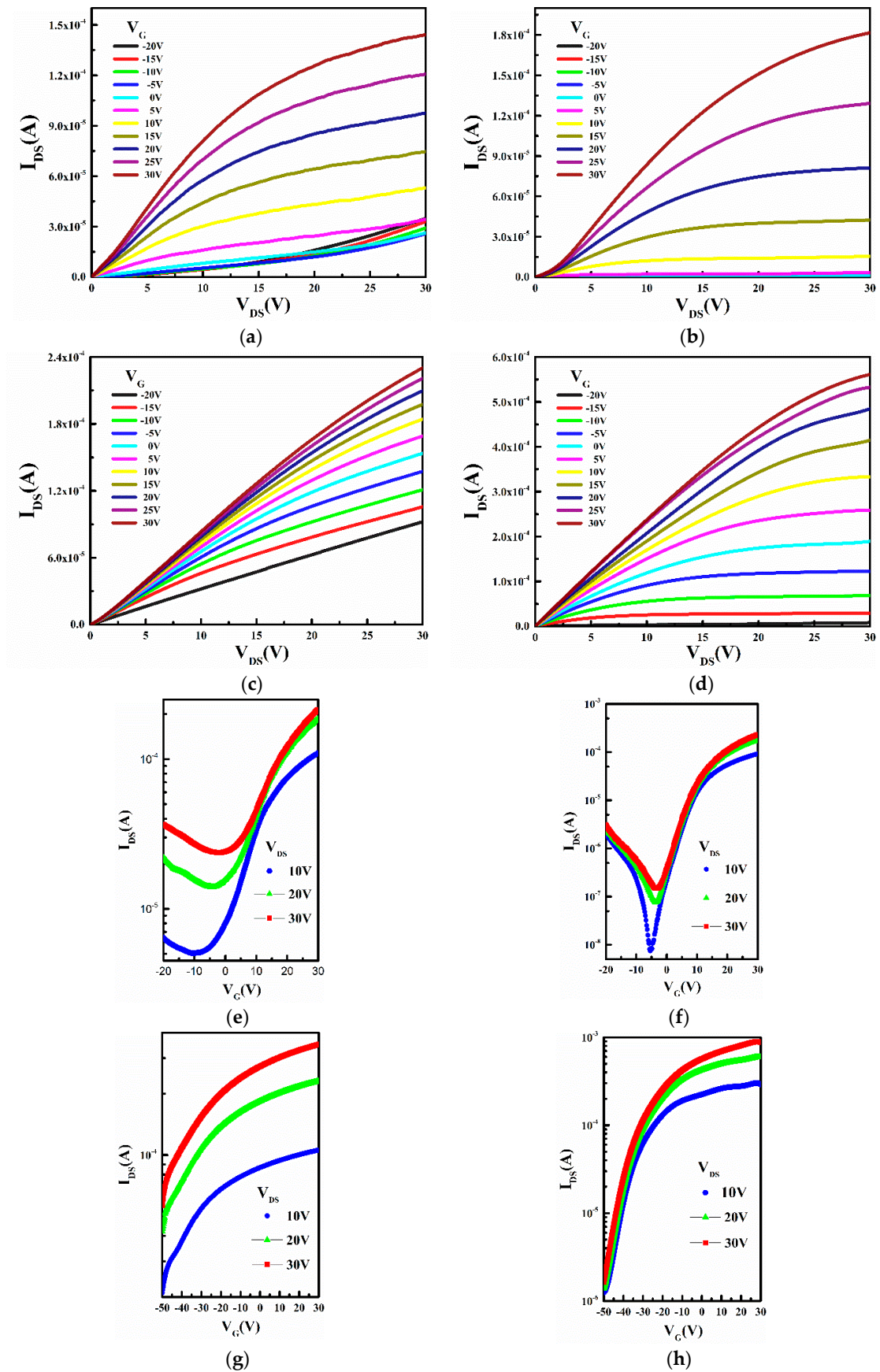
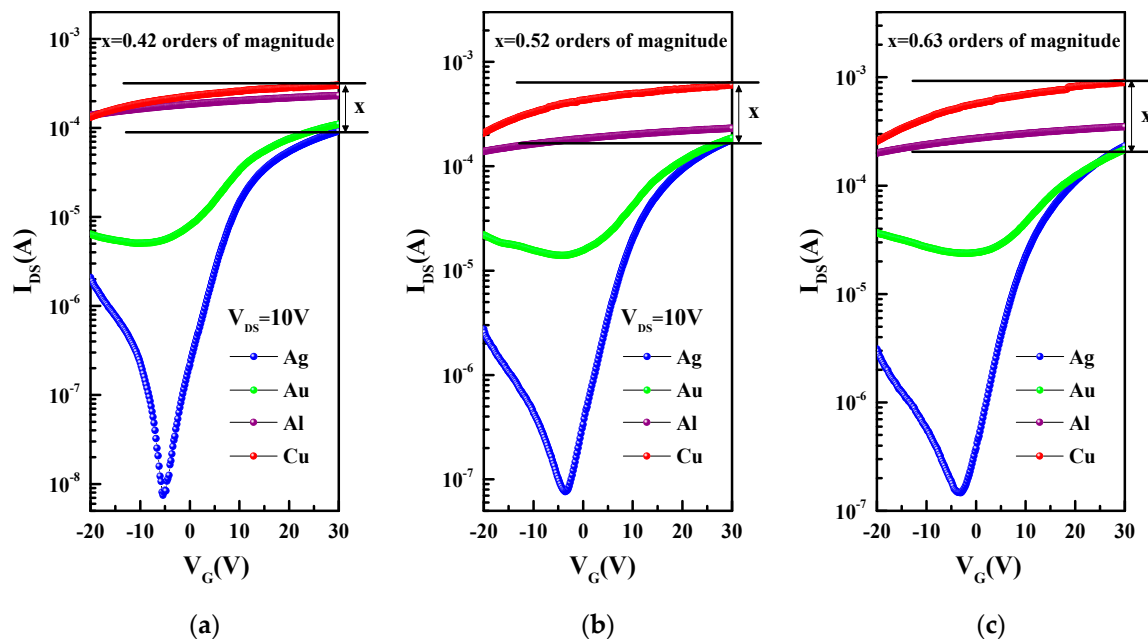


Figure 4. Output curve of (a) Au, (b) Ag, (c) Al, (d) Cu and transfer curve of (e) Au, (f) Ag, (g) Al, (h) Cu.

Table 1. Characteristic data of the MoS₂-FET devices ($V_{DS} = 10$ V).

Electrode	Mobility (cm ² /Vs)	On/Off Ratio	Threshold Voltage(V)
Au	21.01	2.18×10^1	−3
Ag	23.15	1.23×10^4	2.21
Al	5.35	4.14×10^0	−55
Cu	40.52	2.25×10^2	−55

The property of metal–semiconductor contact is essential to modern electronics and optoelectronics [17]. According to the thermionic emission theory, the mean free path of the majority of carriers (electrons) in n-type semiconductor-metal contact is much larger than the Schottky barrier width, so the collision of electrons in the barrier region can be neglected. The influence of the barrier shape is not prominent, and the Schottky barrier height (SBH) plays a decisive role here. SBH represents the energy required for a single charge carrier to transfer between semiconductor and metal. It fundamentally determines the efficiency of charge transfer and directly affects device performance [18]. Meanwhile, SBH is derived from the difference of work functions between metal and semiconductor, which can lead to discrepancies in barrier height and charge injection quantity [19]. All of these factors will eventually cause an obvious disparity in on-state current, which is presented on the transfer characteristic curve. Figure 5 is the on-state current of MoS₂ devices with four metallic electrodes at three types of drain-source voltage. The difference in the on-state currents in the transfer curve is less than 0.63 orders of magnitude that cannot fit with the gaps in the work functions of the four metals.

**Figure 5.** The comparison of the on-state current of MoS₂ devices with 4 different metallic electrodes at 3 different types of drain-source voltage of (a) 10 V; (b) 20 V; (c) 30 V.

As mentioned above, electrons in semiconductors can enter metals through barriers as long as they have enough energy to cross barriers. Similarly, electrons in metals can also enter semiconductors. Based on the above conditions, the calculation of current can be reduced to the calculation of the number of carriers crossing the barrier, as shown in Equation (2) [16], where A is the Richardson constant ($120 \text{ A/cm}^2 \cdot \text{K}^2$), T is the thermodynamic temperature (300 K), K_0 is the Boltzmann constant ($1.380 \times 10^{-23} \text{ J/K}$), V_{DS} is the drain-source voltage (10 V), $q\Phi_{SB}$ is SBH, q is the electron charge ($1.602 \times 10^{-19} \text{ C}$), and J is the current density between semiconductor and metal. It is known that the

drain-source current (I_{DS}) is the product of the current density (J) and the average contact area S of the electrode in the device, as shown in Equation (3). We substituted it into Equation (2) to obtain Equation (4). SBHs corresponding to different gate voltages between metals and semiconductors can be calculated with the known constant and I_{DS} in the device transfer characteristic curve at $V_{DS} = 10$ V.

$$J = A * T^2 \exp\left(-\frac{q\Phi_{SB}}{k_0T}\right) \exp\left(\frac{qV_{DS}}{k_0T}\right) \quad (2)$$

$$I_{ds} = J * S \quad (3)$$

$$\Phi_{SB} = -\ln\left(\frac{I_{DS}}{A * T^2 * S}\right) * \frac{k_0T}{q} + V_{DS} \quad (4)$$

The effective barrier height (Φ_{ESB}), defined as the SBH when V_g equals to flat-band voltage (V_{FB}), can be represented as the longitudinal coordinate value corresponding to an intersection point of the tangent of the descending position and the curve, as shown in Figure 6. It can be seen that Φ_{ESB} values of the four types of metal–semiconductor contacts ranged from 10.448 to 10.606 eV with a difference of no more than 0.16 eV. In ideal metal–semiconductor contact, SBH can be well predicted by the Schottky–Mott rule, as shown in Equations (5) and (6) [20], where Φ_M is the work function of metals; X_S and I_S are the electron affinity and ionization potential of semiconductors; $\Phi_{SB,n}$ and $\Phi_{SB,p}$ are the SBH of electrons and holes, respectively. The Schottky–Mott rule shows that Φ_{SB} is linearly related to the work function of metals, and its relationship curve has a uniform slope, as shown in Equation (7). In Equation (7), if $S = 1$, the metal–semiconductor system conforms to Schottky–Mott rule. However, the calculation based on the experimental data in this paper shows that there is no linear correlation between Φ_{SB} and metal work function for $S = 0.11$ in the four metal material systems as shown in Figure 7a. Theoretically, the above results are due to the effect of Fermi-level pinning (FLP). Meanwhile, the results we obtained were concluded from the statistical data based on a certain number of devices that meant the experimental results have high repeatability. Moreover, we present another group of four devices with the calculated S value of 0.019 in Figure 7b. This result is in good accordance to the former group.

We suppose the main causes of FLP are the surface states of semiconductors [20,21] formed by crystal defects [20–23] such as interface reconstruction. If the surface density of states of MoS_2 is very large, the metal semiconductor system will screen the effect of metal contact on the barrier. Here, the barrier height at the metal–semiconductor interface is mainly determined by the surface properties of MoS_2 , but not the work function of the metal. In general, due to the difference in the surface density of states, a part of the contact potential difference will fall in the semiconductor with metal–semiconductor contact, so the work function of metal may still impact on the surface barrier, but to a small extent. This is in accordance with our calculated results for the barrier heights of the four devices.

$$\Phi_{SB,n} = \Phi_M - X_S \quad (5)$$

$$\Phi_{SB,p} = I_S - \Phi_M \quad (6)$$

$$S = \left| \frac{d\Phi_{SB}}{d\Phi_M} \right| \quad (7)$$

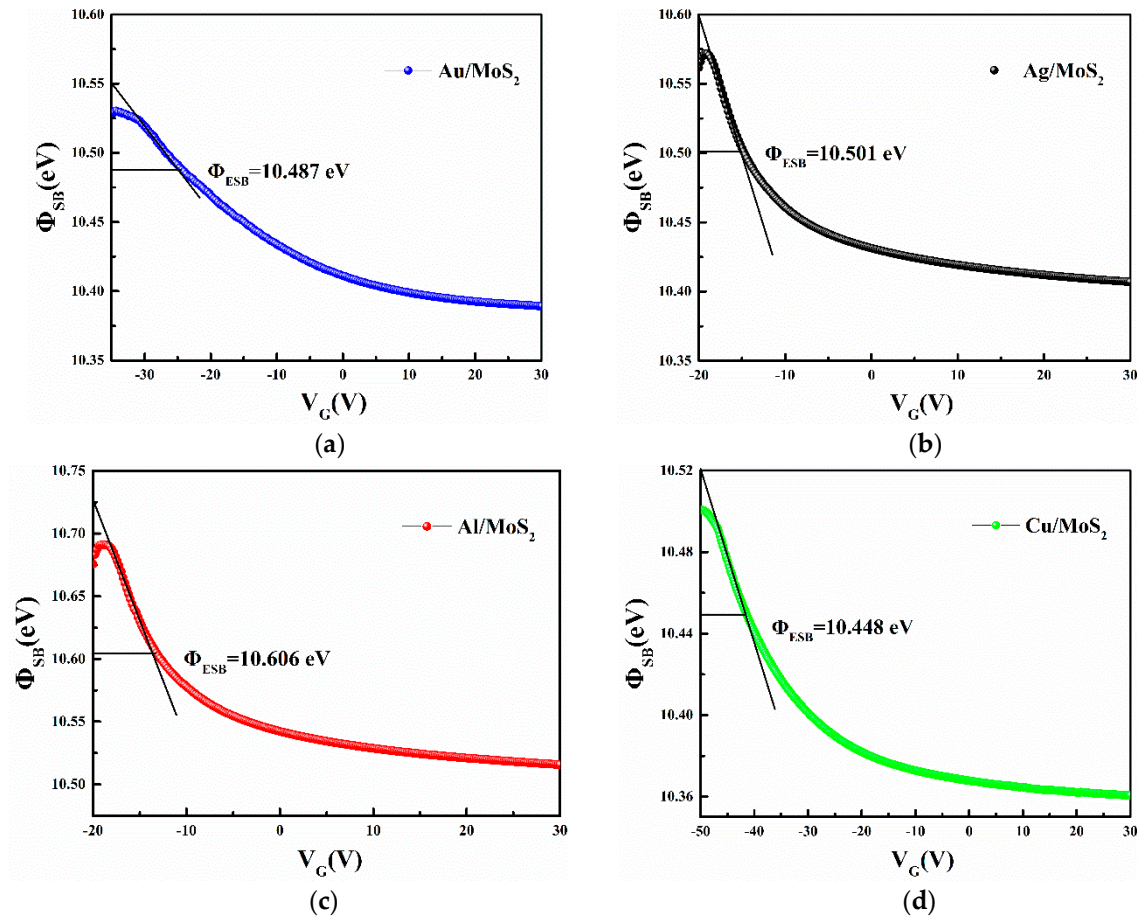


Figure 6. Barrier heights of MoS₂-FETs constructed by electrode of (a) Au; (b) Ag; (c) Al; (d) Cu.

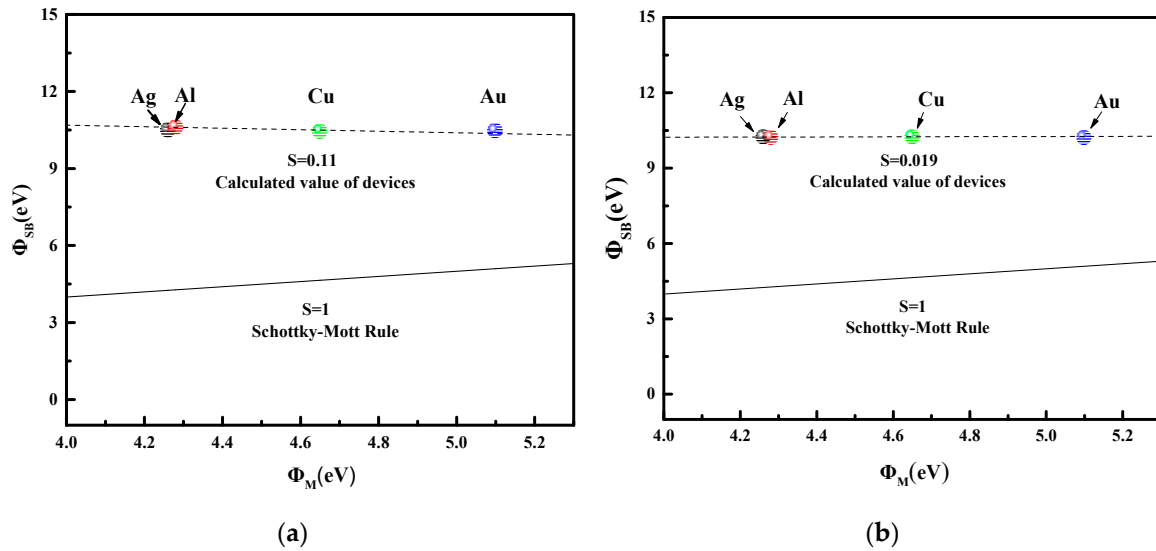


Figure 7. Calculated interface *S* values of devices comparing to Schottky–Mott rule in (a) Group 1 and (b) Group 2.

4. Conclusions

In this paper, the FLP mechanism was found in the MoS₂-FETs by calculating the barrier height through thermionic emission theory. The FLP limits some performance of the FETs with different electrodes and may be caused by the surface states of semiconductors produced from crystal defects.

Current studies will be helpful for obtaining a deep understanding of the metal–MoS₂ contact mechanism and can lay a foundation for the preparation of high performance MoS₂-FET devices.

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Conflicts of Interest: The authors declare no conflict of interest.

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