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An Interleaved DC/DC Converter with Soft-switching Characteristic and high Step-up Ratio

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Received: 25 February 2020; Accepted: 19 March 2020; Published: 22 March 2020

Abstract: This study presents a dc/dc converter featuring soft-switching characteristic, high conversion efficiency, and high step-up ratio. The proposed circuit is composed of two parallel-connected boost converters. Only one coupled inductor is used to replace inductors of the boost converters which are interleaved operated at discontinuous-conduction mode (DCM). The current ripples at the input and the output terminals are reduced due to the interleaved operation. By freewheeling the current of the coupled inductor to discharge the stored electric charges in the parasitic capacitors of the active switches, both active switches can fulfill zero-voltage switching on (ZVS). Owing to DCM operation, the freewheeling diodes can fulfill zero-current switching off (ZCS). Therefore, the power conversion efficiency is improved. The operation principle for each operation mode is analyzed in detail and design equations for the component parameters are provided in this report. Finally, a prototype 200 W 48–400 V converter was implemented and measured to demonstrate the effectiveness of the proposed circuit.

Keywords: boost converter; discontinuous-conduction mode (DCM); interleaved operation; voltage gain; zero-current switching off (ZCS); zero-voltage switching on (ZVS)

1. Introduction

Recently, renewable energies have been increasingly used to meet growing energy demands and mitigate climate change caused by the greenhouse effect due to the burning of large amounts of fossil fuels. Batteries are often used in energy storage systems to compensate the power fluctuation between renewable power generation systems and consumption [1–3]. Since battery voltage is usually small and has a wide range of variation, a high step-up dc/dc converter is indispensable on application where high dc voltage is required [4–6]. The boost converter has been widely adopted for step-up application because it has the advantages of simple circuit architecture and easy control [7,8]. Theoretically, the voltage gain of a boost converter is tremendous high when its duty ratio is close to 1. Under ideal conditions, the value of the voltage gain at the 0.9 duty cycle is equal to 10. Nevertheless, it is impractical to operate a boost converter at such a high duty cycle, because when the resistance of the inductor and the semiconductor device is considered in the actual circuit, both the circuit efficiency and the voltage gain will be greatly reduced [9]. On the other hand, the voltage gain of a boost converter operating at discontinuous-conduction mode (DCM) is higher than that of a boost converter operating at continuous-conduction mode (CCM). A DCM operated boost converter could provide a reasonable solution for achieving high voltage gain. Nevertheless, a smaller inductor is used at DCM operation

and the current ripples at both the input and the output sides are high. It requires a large capacitor to filter out the current ripple to obtain a smooth output voltage.

The circuit efficiency is another important issue for direct current-to-direct current (DC/DC) converters. However, the traditional pulse-width modulation (PWM) converters operate at hard switching, leading to high switching losses and high voltage and/or current stresses. In order to solve the drawbacks of hard switching, researchers have proposed many soft-switching technologies to enable the semiconductor devices operate at either ZVS or ZCS. Synchronous rectification (SR) technique is popularly applied to reduce the conduction loss, especially when the output is low voltage and high current. SR technique use a synchronous switch to replace the freewheel diode. If the synchronous switch remains on until the inductor current decreases from positive to negative, the active switch can achieve ZVS operation by flowing the negative current of the inductor to release to charge stored in its parasitic capacitor [10–12]. However, the SR technique is more complicated since it requires a current sensor and corresponding control to precisely turn off the synchronous switch. The active clamping circuits or snubber circuits are often used to achieve soft-switching operation [13–16]. However, these techniques need to use additional auxiliary active switches, diodes, and/or passive components to operate the main active switch at ZVS. The control circuit is more complicated and circuit cost is higher. Besides, the current loops in the active clamping or snubber circuits would cause conduction losses and even more switching losses.

In addition to increasing power capacity and reducing current ripple, some interleaved dc/dc converters also have the advantages of ZVS operation [17–20]. In these interleaved converters, the active switches are arranged to be turned on and off alternately and an additional inductor is added. The principle of ZVS operation is similar to that of SR technology. The additional inductor is operated at CCM. As soon as one active switch is turned off, the current of the additional inductor will flow through the parasitic capacitor of the other active switch to release its stored energy. When the parasitic capacitor is fully discharged, the diode connected in parallel with the active switch conducts to clamp the active switch at near zero volts. Then, it can be turned on at zero voltage. Unfortunately, the added inductor is usually larger than the energy-stored inductor of the PWM-typed converter. It hinders reducing the size and improving the efficiency of the converter.

Aiming to solve the above shortcomings and propose a better solution, this manuscript presents an interleaved converter. It is mainly composed of two boost converters connected in parallel. A coupled inductor consisting of a magnetic core and two windings is used instead of the two inductors of the boost converters. Although the boost converters are designed to operate at DCM, the current ripple is low due to interleaved operation. High circuit efficiency is achieved by operating all the semiconductors at either ZVS or ZCS. A 200 W 48 V/400 V prototype converter is built and measured to verify the feasibility of this proposed circuit.

2. Proposed Circuit Configuration and Operation Analysis

2.1. Proposed Circuit Configuration

Figure 1 shows the proposed interleaved dc/dc converter. It is mainly composed of two boost converters where the coupled inductor (T_1) served as the energy-stored inductor. The coupled inductor is made up of a magnetic core and two windings with the same number of turns. Two MOSFETs (S_1, S_2) play the role of active switches. Two diodes (D_1, D_2) are used to freewheel the inductor current while the other two diodes (D_{S1}, D_{S2}) respectively in parallel with S_1 and S_2 are the intrinsic diodes of the MOSFETs. The gate-source voltages (v_{GS1}, v_{GS2}) are used to alternatively turn the active switches on and off at a high switching frequency f_s . The waveforms of v_{GS1} and v_{GS2} are shown in Figure 2. They are complementary rectangular waveforms with a short overlap time between them.

Figure 1. Proposed interleaved dc-to-dc converter.

Figure 2. Gate-source voltages v_{GS1} and v_{GS2} .

Ignoring the winding resistance and the core loss, the equivalent circuit of the coupled inductor is shown in Figure 3. T_M is a transformer with a turn ratio equal to 1, and L_M is its mutual inductance. L_1 and L_2 represent the leakage inductances in the primary winding and the secondary ones, respectively. Based on the equivalent circuit, the currents flowing into L_1 and L_2 , denoted by i_{L1} and i_{L2} can be expressed as

$$i_{L1} = i_{LM} + i_{T1}, \quad (1)$$

$$i_{L2} = i_{T2} = -i_{T1}, \quad (2)$$

where i_{T1} , i_{T2} , and i_{LM} are the primary current, the secondary current and the magnetic exciting current of the transformer, respectively. From Figure 1, the input current denoted by i_{in} would be equal the sum of i_{L1} and i_{L2} . Based on Equations (1) and (2), i_{in} is equal to the magnetic exciting current.

$$i_{in} = i_{L1} + i_{L2} = i_{LM}, \quad (3)$$

Figure 3. Equivalent circuit for the coupled inductor.

The voltages across both windings of the transformer are equal and can be expressed as:

$$v_T = \frac{L_M di_{LM}}{dt}, \quad (4)$$

2.2. Circuit Analysis

In order to simplify the circuit analysis, some assumptions are made as follows.

- The semiconductor devices are ideal in spite of considering the intrinsic diode and the parasitic capacitance of the MOSFETs.
- The leakage inductances are equal ($L_1 = L_2 = L_l$). The mutual inductance L_M is large enough and the magnetic exciting current i_{LM} is constant.
- The output capacitance C_o is large enough. Hence, the output voltage V_o is regarded as constant.

According to the conducting status of the semiconductor devices, there are eight operation modes in one high-frequency cycle at steady-state operation. Figure 4 shows the current loops for each operation mode and Figure 5 illustrates the conceptual voltage and current waveforms of the main components.

Figure 4. Operation modes.

Figure 5. Conceptual waveforms.

A. Mode I ($t_0 < t < t_1$)

Before the beginning of Mode I, both active switches S_1 and S_2 are on. There are two current loops. One is i_{L1} flows through S_1 . The other is i_{L2} flows through S_2 . Since S_2 is turned on before S_1 , most of the magnetic exciting i_{LM} are supplied by i_{L2} .

Mode I starts at the instant when v_{GS2} drops to zero volts to turn off S_2 . The equivalent circuit is shown in Figure 4a. The current in the secondary winding i_{L2} diverts from S_2 to flow into its parasitic capacitance C_{DS2} . Since the parasitic capacitance is generally very small, it takes a very short time for the voltage across C_{DS2} being charged to equal the output voltage V_o . Thereafter, i_{L2} diverts from

C_{DS2} to flow through D_2 and the output capacitance C_o . During this period, C_o is charged. The voltage equations of the two converters are as follows.

$$V_{in} = v_{L1} + v_T, \quad (5)$$

$$V_{in} = v_{L2} + v_T + v_{DS2} = v_{L2} + v_T + V_o, \quad (6)$$

where v_{L1} and v_{L2} represent the voltages across the leakage inductances L_1 and L_2 , respectively. Adding Equations (5) and (6) gives

$$2V_{in} = (v_{L1} + v_{L2}) + 2v_T + V_o, \quad (7)$$

From Equation (3), the following equation is obtained.

$$v_{L1} + v_{L2} = \frac{L_l di_{L1}}{dt} + \frac{L_l di_{L2}}{dt} = \frac{L_l di_{LM}}{dt}, \quad (8)$$

The voltage across the mutual inductance can be obtained by substituting Equations (4) and (8) into Equation (7).

$$v_T = \frac{L_M}{L_l + 2L_M} (2V_{in} - V_o), \quad (9)$$

By designing V_o to be higher than two times of V_{in} , v_T would be negative and i_{LM} would decrease linearly in this mode. The voltages across the leakage inductances can be expressed as Equations (10) and (11) by substituting Equation (9) into Equations (5) and (6), respectively.

$$v_{L1} = \frac{L_l V_{in}}{L_l + 2L_M} + \frac{L_M V_o}{L_l + 2L_M}, \quad (10)$$

$$v_{L2} = \frac{L_l V_{in}}{L_l + 2L_M} - \frac{(L_l + L_M) V_o}{L_l + 2L_M}, \quad (11)$$

From Equations (10) and (11), v_{L1} is positive and v_{L2} is negative since L_m is much larger than L_l . Hence, i_{L1} rises and i_{L2} decreases linearly. It means that the magnetic exciting current diverts from the secondary winding to the primary winding. As soon as i_{L2} decreases to zero, D_2 turns off and the circuit operation enters Mode II.

B. Mode II ($t_1 < t < t_2$)

This mode describes the short transient for the C_{DS2} discharging from V_o to -0.7 V. The equivalent circuit is shown in Figure 4b. During this mode, the voltage across L_2 can be expressed as

$$v_{L2} = V_{in} - v_T - v_{DS2}, \quad (12)$$

The voltage v_{L2} is negative and i_{L2} continuously decreases from zero. In other words, i_{L2} changes polarity and becomes negative. The current loop of i_{L2} is C_{DS2} , the secondary winding, V_{in} . The voltages v_{L1} , v_{L2} and v_T are expressed as

$$v_{L1} = \frac{L_l V_{in}}{L_l + 2L_M} + \frac{L_M v_{DS2}}{L_l + 2L_M}, \quad (13)$$

$$v_{L2} = \frac{L_l V_{in}}{L_l + 2L_M} - \frac{(L_l + L_M) v_{DS2}}{L_l + 2L_M}, \quad (14)$$

$$v_T = \frac{L_M}{L_l + 2L_M} (2V_{in} - v_{DS2}), \quad (15)$$

During this mode, C_{DS2} is discharged and v_{DS2} keeps decreasing. From Equations(13) – (15), v_{L1} decreases. On the contrary, v_{L2} and v_T both increase. As soon as v_{DS2} decreases to -0.7 V, i_{L2} diverts from C_{DS2} to D_{S2} and Mode II ends.

C. Mode III ($t_2 < t < t_3$)

The equivalent circuit of Mode III is shown in Figure 4c. Neglecting the diode conduction voltage (0.7 V), the voltage equations for both converters are

$$V_{in} = v_{L1} + v_T, \quad (16)$$

$$V_{in} = v_{L2} + v_T, \quad (17)$$

Adding Equation (16) and Equation (17) results in

$$2V_{in} = (v_{L1} + v_{L2}) + 2v_T, \quad (18)$$

Substituting Equations (4) and (8) into Equation (18) leads to

$$v_T = \frac{2L_M V_{in}}{L_l + 2L_M}, \quad (19)$$

Substituting Equation (19) into Equations (16) and (17) results in

$$v_{L1} = v_{L2} = \frac{L_l V_{in}}{L_l + 2L_M}, \quad (20)$$

From Equations (19) and (20), v_T , v_{L1} , and v_{L2} are all positive. Since the mutual inductance L_M is usually much higher than the leakage inductance L_l , the v_{L1} and v_{L2} are very small and the currents i_{L1} and i_{L2} rises slowly.

During this mode, D_{S2} is on and the drain to source voltage of S_2 is clamped at 0.7 V. The gated voltage v_{GS2} becomes high level before i_{L2} rises to zero. When i_{L2} rises to zero and then becomes positive, S_2 is turned on at ZVS and Mode III ends.

D. Mode IV ($t_3 < t < t_4$)

The voltage equations for v_T , v_{L1} , and v_{L2} are as same as that of Mode III. The voltages v_T , v_{L1} , and v_{L2} are all positive. Therefore, the currents i_{LM} , i_{L1} , and i_{L2} keep rising. When the gated voltage v_{GS1} becomes zero volts. S_1 is turned off and the circuit enters Mode V.

E. Mode V ($t_4 < t < t_5$)- H. Mode VIII ($t_7 < t < t_8$)

The equivalent circuits of Mode V to Mode VIII are shown in Figure 4e–h, respectively. Owing to the symmetrical operation for both boost converters, the operation of Mode V - Mode VIII is similar to the operation of Mode I– Mode IV. As soon as v_{GS2} drops zero, S_2 is turned off and Mode VIII ends. The circuit goes to the first mode of the next high frequency cycle.

3. Design Equations

Since the mutual inductance L_M is large enough, I_{LM} is assumed to be constant. Based on the principle of energy conservation, the output power is equal to

$$P_o = \eta \times V_{in} \times I_{in} = \eta \times V_{in} \times I_{LM}, \quad (21)$$

where η represents the circuit conversion efficiency. From (21), I_{LM} can be expressed as

$$I_{LM} = \frac{P_o}{\eta V_{in}} = \frac{V_o^2}{\eta V_{in} R_o}, \quad (22)$$

By assuming that the mutual inductance L_M is much larger than the leakage inductance L_l , from Equations (9)–(11), v_T , v_{L1} , and v_{L2} in Mode I are approximately equal to

$$v_T = V_{in} - \left(\frac{V_o}{2}\right), \quad (23)$$

$$v_{L1} = \frac{V_o}{2}, \quad (24)$$

$$v_{L2} = \frac{-V_o}{2}, \quad (25)$$

In practical circuits, parasitic capacitors are very small. It takes only a short time to fully discharge the parasitic capacitor. It means that the period of Mode II is very short and hence i_{L2} is near zero at the end of this mode. Based on Equation (3), the peak value of i_{L2} is approximately equal to I_{LM} . In Mode I, i_{L2} decreases and the time required for the current i_{L2} to drop from its maximum value to zero is equal to

$$t_f = \frac{L_l I_{LM}}{v_{L1}} = \frac{L_l I_{LM}}{V_o/2} = \frac{2L_l I_{LM}}{V_o}, \quad (26)$$

The voltage equations for v_T in Mode I and in Mode III and Mode IV are Equations (9) and (19), respectively. At steady state, its average value should be zero.

$$\overline{v_T} = \frac{L_M}{L_l + 2L_M} (2V_{in} - V_o) \cdot t_f + \frac{2L_M V_{in}}{L_l + 2L_M} \cdot t_r = 0, \quad (27)$$

where t_f is the period of Mode I and t_r is that of Mode III plus Mode IV. The fall time t_f plus the rise time t_r equals to half of the switching period

$$t_f + t_r = 0.5T_s, \quad (28)$$

where T_s represents the switching period. Combining Equations (27) and (28) gets

$$t_f = \frac{V_{in}}{V_o} T_s, \quad (29)$$

Substituting Equation (29) into Equation (26) gets

$$\frac{V_{in} T_s}{V_o} = \frac{2L_l I_{LM}}{V_o}, \quad (30)$$

Combining Equations (22) and (30), the leakage inductance is obtained as

$$L_l = \frac{V_{in} T_s}{2I_{LM}} = \frac{\eta V_{in}^2}{2P_o f_s}, \quad (31)$$

4. Illustrative Example and Experimental Results

A 200 W prototype was built and tested to verify the feasibility of the proposed circuit. The circuit specification is shown in Table 1 and the values of the circuit component are shown in Table 2. The input and output voltages are 48V_{dc} and 400V_{dc}, respectively. The switching frequency of 50 kHz is chosen. From Equation (31), the output power is inverse proportional to leakage inductance L_l . Assuming a circuit efficiency of 95%, L_l can be obtained.

$$L_l = \frac{\eta V_{in}^2 R_o}{2V_o^2 f_s} = \frac{0.95 \times 48^2}{2 \times 200 \times 50 \times 10^3} = 0.11 \text{ mH}$$

Table 1. Specification of the proposed converter.

Input voltage V_{in}	48 V _{dc}
Output voltage V_o	400 V _{dc}
Output current I_o	0.5 A
Load Resistance R_o	800 Ω
Switching frequency f_s	50 kHz

Table 2. Component parameters.

Leakage inductance L_1, L_2	0.11 mH
Mutual inductance L_M	0.58 mH
Output capacitance C_o	220 μ F
Diodes D_1, D_2	C3D10060A
Active switches S_1, S_2	35N65M5

The control circuit is illustrated in Figure 6. It includes a half-bridge self-oscillating driver (IR2153), two inverters (74LS04P) and two power metal-oxide-semiconductor field-effect transistor (MOSFET) gate drivers (TLP250). The IR2153 provides two complementary square voltages with dead time between them. After being inverted by 74LS04P, the output becomes two square voltages with overlapping times. Finally, the overlapping voltages are sent to the TLP250 and their outputs are used to drive the MOSFETs.

Figure 6. Control circuit.

The waveforms of the gate voltages, v_{DS1} and v_{DS2} are shown in Figure 7. As shown, there are overlapping time between them. Figure 8 shows the current waveforms in the primary and the secondary windings of the coupled inductor. As expected, both currents decrease from the peak value to a negative value near zero. The current and voltage waveforms of the active switches are shown in Figure 9. It demonstrates that both active switches are operated at ZVS. The drain-to-source voltages of S_1 and S_2 are clamped at 0.7 V when the current is negative. It is believed that the negative currents flow through the intrinsic diodes of S_1 and S_2 . The output voltage and output current are shown in Figure 10. The measured voltage and current are 400V and 0.5A, consistent with the theoretical prediction. The measured circuit efficiency is 94.3%.

Figure 7. Voltage waveforms of v_{DS1} and v_{DS2} . (v_{DS1} , v_{DS2} : 5 V/div, time: 5 μ s/div)

Figure 8. Current waveforms of i_{L1} and i_{L2} . (i_{L1} , i_{L2} : 2 A/div, time: 5 μ s/div)

(a)

(b)

Figure 9. Voltage and current waveforms (a) v_{DS1} and i_{S1} , and (b) v_{DS2} and i_{S2} . (v_{DS1} , v_{DS2} : 200 V/div, i_{S1} , i_{S2} : 2 A/div, time: 5 μ s/div)

Figure 10. Waveform of V_o and I_o . (V_o : 100 V/div, I_o : 0.5 A/div, time: 5 ms/div)

5. Conclusions

This paper proposes an interleaved dc/dc converter that is composed of two boost converters. Both boost converters share a coupled inductor that is made up of one magnetic core with two windings. It effectively reduces the product size and cost. Owing to the interleaved operation, the power capacity is doubled. Moreover, low current ripple at both the input and the output sides is achieved due to the interleaved operation. By operating the boost converters at DCM, the freewheeling diodes and the active switches can respectively fulfill ZCS operation and ZVS operation, without the need to use any active clamping or snubber circuits. It helps to reduce the component count and improve the circuit efficiency. In summary, the proposed interleaved converter has the advantages of less component count, low current ripple, high circuit efficiency, and easy control. A 200 W prototype converter was implemented and measured. The circuit efficiency is 94.3% at rated power operation.

Author Contributions: Y.-N.C. and H.-L.C. conceived and designed the circuit; C.-H.C. and H.-C.Y. performed circuit simulations and designed parameters of the circuit components; W.-D.H. carried out the prototype converter, and measured as well as analyzed experimental results; H.-L.C. wrote the paper and Y.-N.C. revised it for submission. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: This work was supported by the Ministry of Science and Technology, R.O.C. under Grant MOST 105-2221-E-214-027.

Conflicts of Interest: The authors declare no conflicts of interest.

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