Analysis of a Three-Level Bidirectional ZVS Resonant Converter

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Abstract: A bidirectional three-level soft switching circuit topology is proposed and implemented for medium voltage applications such as 750 V dc light rail transit, high power converters, or dc microgrid systems. The studied converter is constructed with a three-level diode-clamp circuit topology with the advantage of low voltage rating on the high-voltage side and a full-bridge circuit topology with the advantage of a low current rating on the low-voltage side. Under the forward power flow operation, the three-level converter is operated to regulate load voltage. Under the reverse power flow operation, the full-bridge circuit is operated to control high-side voltage. The proposed *LLC* resonant circuit is adopted to achieve bidirectional power operation and zero-voltage switching (ZVS). The achievability of the studied bidirectional ZVS converter is established from the experiments.

1. Introduction

Renewable power to reduce the effect of global warming has been developed by using high efficiency power electronic based converters in local dc nanogrid or microgrid distribution [1–6] between renewable energy power and local dc or ac loads. In order to maintain the voltage stability on dc distribution system, energy storage power units are usually demanded between battery banks and dc bus system to save (or restore) excess (or insufficient) energy on the dc bus. Therefore, the bidirectional pulse-width modulation (PWM) converters have been proposed for the battery-based systems [7–14] such as electric vehicles, hybrid electric vehicles, and dc microgrids. In dc microgrids, the unipolar voltage (380 V) or bipolar voltage (±380 V or 760 V) distribution can be adopted on the dc bus voltage. High frequency link medium voltage converters have been used for dc traction power units, three phase industry power supplies and dc microgrids. Three-level dc converters with 600 V MOSFETs or conventional PWM converters with 1200 V IGBTs or SiCs have been presented in medium voltage input applications. The drawback of 1200 V IGBT is low switching frequency and the cost of 1200 V SiC is expensive. Bidirectional PWM converters with dual active bridge (DAB) structure have been studied to realize forward and reverse power transfer. Three-level bidirectional converters or cascaded converters with the high frequency MOSFETs have been developed for high voltage systems such as 760 V input. PWM scheme is widely adopted in bidirectional DAB systems to control power flow and realize soft switching turn-on characteristics. However, the control scheme for generating the PWM signals is complicated and the circulating current under low duty cycle is high. Resonant converters have the benefits of high circuit efficiency and low electromagnetic interference. A full-bridge resonant circuit topology was proposed in [15] to achieve bidirectional power transfer. However, the soft switching characteristics cannot be achieved in backward power flow. Bidirectional Full-bridge resonant converters presented in [16–18] have symmetric circuit structure to achieve forward and backward power flow so that power switches can realize zero-voltage switching. However, there is a

circulating current on the parallel inductor in primary-side which will result in addition conduction loss during forward power flow.

A soft switching three-level resonant converter is developed for high voltage to low voltage conversion. The profits of the developed converter are forward and backward power flow capability and zero-voltage turn-on characteristic. Three-level diode-clamp circuit topology is used on the primary-side and full-bridge circuit topology is adopted on the secondary-side. The *LLC* circuit tank is employed to control load voltage and achieve zero-voltage switching on active devices. For forward power transfer, the three-level diode-clamp converter is controlled using the pulse-frequency modulation (PFM) to control low-side voltage and active devices of full-bridge converter on the secondary-side are operated as synchronous rectifiers. In order to implement the same resonant circuit structures for bidirectional power flow, an additional inductor is connected on the primary-side during the reverse power flow condition. In reverse power flow operation, the full-bridge converter on the low-voltage side is operated with PFM scheme to control high-side voltage. The proposed converter with bidirectional power flow capability can be applied in local dc nanogrid or microgrid distribution between renewable energy power and local dc or ac loads. The circuit schematic and circuit operation are provided and discussed in Sections 2 and 3. The circuit characteristic and experiments with a 1.44 kW laboratory circuit are demonstrated and discussed to show the feasibility of the studied bidirectional power converter in Section 4. Finally, a conclusion of the studied converter is given in Section 5.

2. Circuit Schematic of the Developed Converter

Figure 1a provides the converter schematic of the studied bidirectional converter. There is a three-level diode-clamp circuit topology on the high-voltage side with the benefit of using low voltage rating switches. Clamped diodes D_a and D_b and capacitor C_f are used to balance input voltages V_{CH1} = V_{CH2} and reduce the voltage stress on $S_1 \sim S_4$. Full bridge circuit topology is used on the low-voltage side to achieve full-wave rectification. S_{ac} and L_b are series-connection and connect to points *a* and *b* in order to achieve *LLC* circuit operation under backward power flow operation (S_{ac} is ON). For forward power operation from V_H (high-side voltage) to V_L (low-side voltage), S_{ac} is OFF and L_b is disconnected on the primary-side. Figure 1b gives the circuit structure under forward power operation. $S_1 \sim S_4$ are main power devices to control output voltage V_L. L_r, L_m and C_r are *LLC* resonant circuit and $Q_1 \sim Q_4$ are activated as synchronous switches. For reverse power operation from the V_L terminal to the V_H terminal, S_{ac} is ON and Figure 1c provides the circuit diagram of reverse power operation. Switches $Q_1 \sim Q_4$ are major power switches and L_r, L_b and C_r are resonant circuit. $D_{S1} \sim D_{S4}$ are operated as a full-wave diode rectifier. Therefore, *LLC* resonant characteristics for both power flow are achieved and the turn-on switching loss of major power switches is removed.
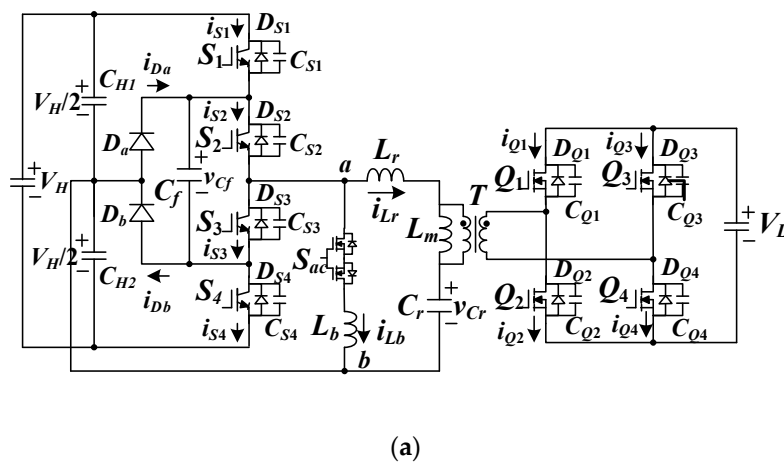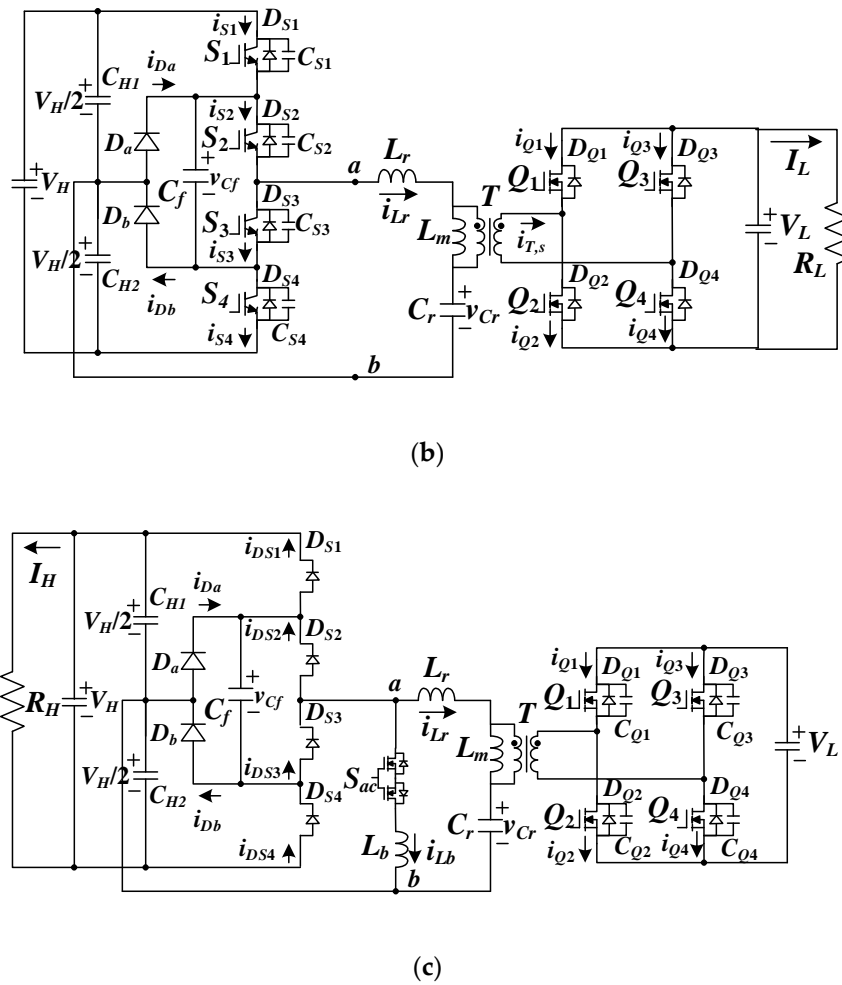

(a)

Figure 1. *Cont.*

(b)

(c)

Figure 1. Proposed converter (**a**) converter structure (**b**) forward power flow operation (S_{ac} off) (**c**) backward power flow operation (S_{ac} on, $S_1 \sim S_4$ off).

3. Circuit Operation

For forward power delivery, the electric power energy is transferred from V_H side to V_L side and S_{ac} is OFF. $S_1 \sim S_4$ are controlled with PFM scheme. Due to PWM signals of $S_1 \sim S_4$, there is a square wave with $-V_H/2$ or $V_H/2$ on the leg voltage v_{ab}. However, $Q_1 \sim Q_4$ are operated as the synchronous switches instead of the rectifier diodes in conventional full-bridge rectifier to reduce conduction loss. The equivalent resonant circuit and PWM waveforms for forward power delivery are provided in Figure 2. To realize the ZVS operation of $S_1 \sim S_4$, the input impedance of *LLC* circuit must be inductive. Figure 3 gives the corresponding equivalent circuits related to six operating steps in a switching period under f_r (resonant frequency) $> f_{sw}$ (switching frequency). It is assumed that the L_r represents the external series resonant inductance and the leakage inductance of transformer and C_r represents the external series resonant capacitance and the parasitic capacitance on transformer winding turns. The output capacitances $C_{S1} - C_{S4}$ are assumed to be identical. In the same manner, $C_{Q1} = \ldots = C_{Q4}$. Since the current i_{Cf} on C_f is less than i_{S1} and i_{S2} in mode 1 and i_{S3} and i_{S4} in mode 4, i_{Cf} is ignored in PWM waveforms. Therefore, i_{S1} is equal to i_{S2} in steps 1–3 and 6 and i_{S3} is equal to i_{S4} in steps 3–6.
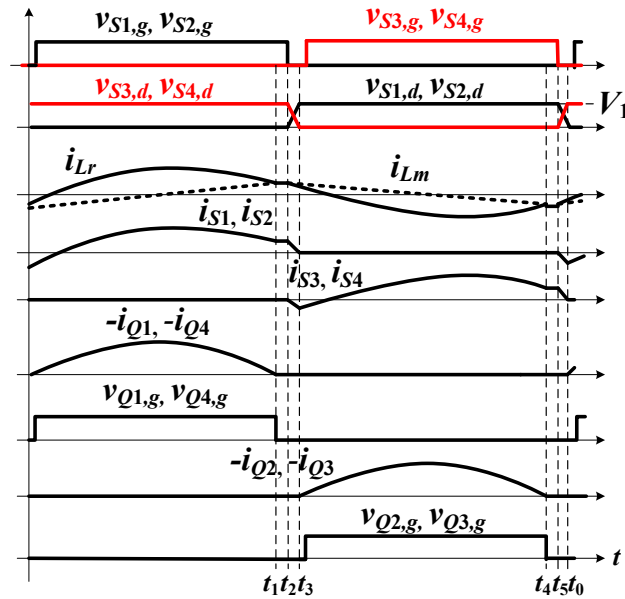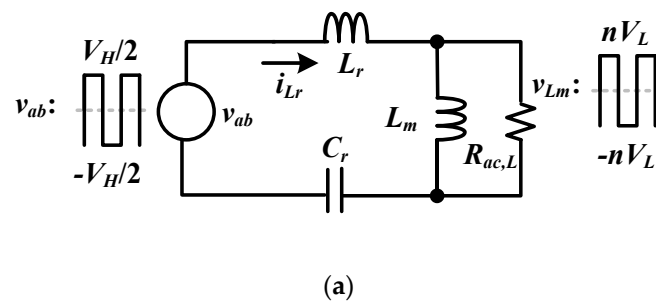
(**a**)

(**b**)

Figure 2. Forward power operation (**a**) the equivalent *LLC* resonant circuit (**b**) pulse-width modulation (PWM) waveforms.

(**a**)

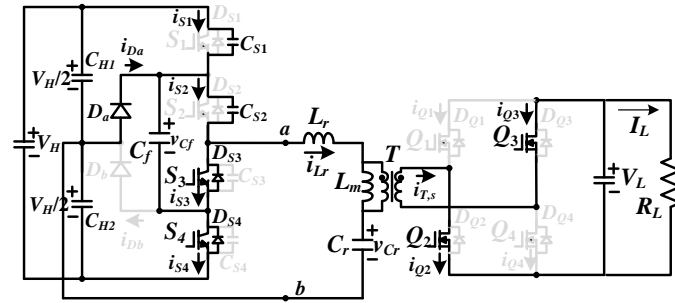**Figure 3.** *Cont.*
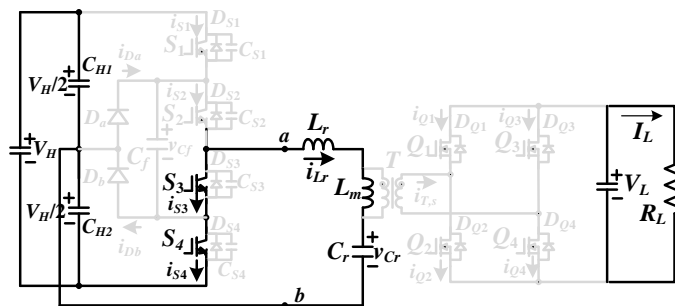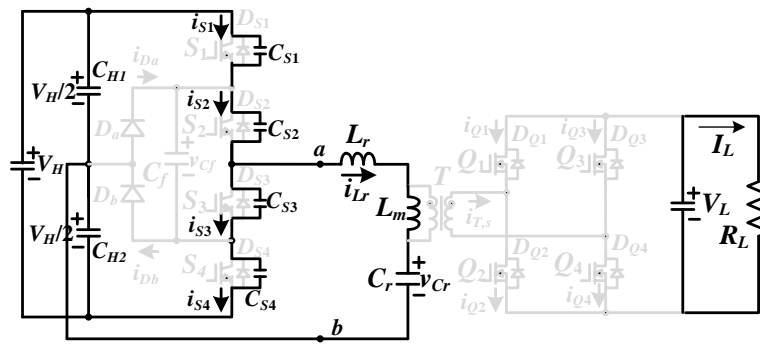
(**b**)

(**c**)

(**d**)

(**e**)

Figure 3. *Cont.*

(**f**)

Figure 3. The corresponding equivalent circuits related to six operating steps for forward power operation (**a**) step 1 circuit (**b**) step 2 circuit (**c**) step 3 circuit (**d**) step 4 circuit (**e**) step 5 circuit (**f**) step 6 circuit.

Step 1 ($t_0 \leq t < t_1$): At $t < t_0$, $i_{Lr} < 0$. Thus, i_{Lr} discharges C_{S1} and C_{S2} are discharged. At t_0, $v_{CS1} = v_{CS2} = 0$. Thus, D_{S1} and D_{S2} are conducting due to $i_{Lr} < 0$. The ZVS operation of S_1 and S_2 can be achieved after time t_0. If $i_{Lr} < 0$, D_b is forward biased. The leg voltage $v_{ab} = v_{Cf} = v_{CS3} = v_{CS4} = V_H/2$. Since $i_{Lr} > i_{Lm}$, Q_1 and Q_4 turn on to conduct the secondary-side current. When i_{Lr} increases and $i_{Lr} > 0$, D_b becomes off. In this step, the magnetizing voltage v_{Lm} is equal to nV_L, where $n = n_p/n_s$ is the transformer turns ratio, and i_{Lm} increases. The ripple current Δi_{Lm} in step 1 is equal to $nV_L\Delta t_{01}/L_m$ where $\Delta t_{01} = t_1 - t_0$. The resonant frequency in step 1 is $f_r = 1/(2\pi\sqrt{L_rC_r})$.

Step 2 ($t_1 \leq t < t_2$): If $f_{sw} < f_r$, i_{Q1} and i_{Q4} will decrease to zero ampere at t_1. Thus, Q_1 and Q_4 can turn off after time t_1. In step 2, the leg voltage $v_{ab} = V_H/2$ and L_r, L_m and C_r are resonant.

Step 3 ($t_2 \leq t < t_3$): At t_2, S_1 and S_2 turn off. The positive current $i_{Lr}(t_2)$ will charge C_{S1} and C_{S2}. On the other hand, C_{S3} and C_{S4} are discharged in this step. The ZVS operation of S_3 and S_4 is expressed in Equation (1).

$$i_{Lm,p} \geq \frac{V_H}{2}\sqrt{\frac{C_S}{L_r}} \tag{1}$$

where $i_{Lm,p}$ is the peak current on L_m and $C_S = C_{S1} = \ldots = C_{S4}$. The peak current $i_{Lm,p}$ is calculated from Equation (2).

$$i_{Lm,p} = \frac{\Delta i_{Lm}}{2} \approx \frac{nV_LT_{sw}}{4L_m} \tag{2}$$

The dead time t_d between S_3 and S_1 (or S_4 and S_2) is approximately expressed in Equation (3).

$$t_d > \frac{C_SV_H}{i_{Lm,p}} = \frac{4L_mC_SV_H}{nV_LT_{sw}} \tag{3}$$

Therefore, the maximum magnetizing inductance is derived in Equation (4).

$$L_m \leq \frac{nV_Lt_dT_{sw}}{4C_SV_H} \tag{4}$$

Step 4 ($t_3 \leq t < t_4$): At t_3, $v_{CS3} = v_{CS4} = 0$. Since $i_{Lr}(t_3)$ is positive, D_{S3} and D_{S4} are conducting. Power devices S_3 and S_4 can turn on after t_3 under zero voltage condition. Since $i_{Lr}(t_3) > 0$, D_a is forward biased. The leg voltage $v_{ab} = -V_H/2$ and $v_{Cf} = v_{CS1} = v_{CS2} = V_H/2$. When i_{Lr} decreases and $i_{Lr} < 0$, D_a becomes off. On the secondary side, $i_{Q2}(t_3) < 0$ and $i_{Q3}(t_3) < 0$. Therefore, Q_2 and Q_3 turn on to conduct the secondary-side current, the primary-side voltage $v_{Lm} = -nV_L$ and i_{Lm} decreases.

Step 5 ($t_4 \leq t < t_5$): The secondary-side switch currents $i_{Q2} = i_{Q3} = 0$ at t_4. Then, Q_2 and Q_3 turn off. In this step, $v_{ab} = -V_H/2$ and L_r, L_m and C_r are resonant.

Step 6 ($t_5 \leq t < T_{sw}+t_0$): At t_5, S_3 and S_4 turn off. In this step, $i_{Lr}(t_5) < 0$ and v_{CS1} and v_{CS2} decrease. The ZVS condition of S_2 and S_1 is the same as S_4 and S_3 in Equation (1). The step 6 is ended at time $T_{sw}+t_0$.
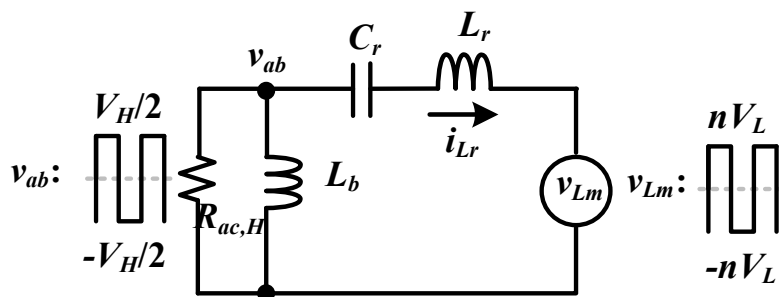
The *LLC* resonant circuit is controlled to achieve ZVS operation and the bidirectional power operation. The resonant circuit is based on the fundamental frequency analysis to achieve load voltage regulation. According to the switching status of power devices $S_1 \sim S_4$ and $Q_1 \sim Q_4$, the voltage values $V_H/2$ and $-V_H/2$ are observed on v_{ab}, and the other voltage values nV_L and $-nV_L$ are generated on the magnetizing inductor voltage v_{Lm}. L_r, C_r, L_m and $R_{ac,L}$ operate as a filter to suppress the high order harmonics. The root mean square (*rms*) voltages at the fundamental frequency for input and output sides are $v_{ab,rms} = \sqrt{2}V_H/\pi$ and $v_{Lm,rms} = 2\sqrt{2}nV_L/\pi$. Based on the power balance between the primary-side and the secondary-side of transformer, the primary-side load resistance is expressed as $R_{ac,L} = 8n^2R_L/\pi^2$. The transfer function $G_{H\_L}(s)$ between the output and input sides in Figure 2a is obtained as:

$$G_{H\_L}(s) = \frac{v_{Lm,rms}(s)}{v_{ab,rms}(s)} = \frac{\frac{sL_mR_{ac,L}}{sL_m+R_{ac,L}}}{\frac{sL_mR_{ac,L}}{sL_m+R_{ac,L}} + sL_r + \frac{1}{sC_r}} \tag{5}$$

$$\left|G_{H\_L}(F)\right| = \frac{K_1F^2}{\sqrt{\left[F^2(K_1+1)-1\right]^2 + \left[Q_1K_1F(F^2-1)\right]^2}} \tag{6}$$

where $F = f_{sw}/f_r$, $f_r = 1/(2\pi\sqrt{L_rC_r})$, $K_1 = L_m/L_r$ and $Q_1 = \sqrt{L_r/C_r}/R_{ac,L}$. From the given input voltage V_H, the output voltage V_L and the circuit parameters L_r, C_r, L_m and R_L, the switching frequency is obtained from Equation (6).

For reverse power flow shown in Figure 1c, the developed converter transfers power from V_L terminal to V_H terminal. S_{ac} is turned on and L_b, L_r and C_r are operated as a series resonant circuit to achieve voltage V_H regulation. Power devices $Q_1 \sim Q_4$ are controlled with PFM scheme and $D_{S1} \sim D_{S4}$ work as a full-wave rectifier. When $|i_{Lr}| > |i_{Lb}|$, D_{S1} and D_{S2} or D_{S3} and D_{S4} are conducting. Since the *LLC* resonant circuit by L_r, C_r and L_b is operated at the inductive load, power devices $Q_1 \sim Q_4$ are operated at the zero-voltage turn-on switching. Figure 4a shows the ac equivalent resonant circuit at reverse power flow operation. L_b and $R_{ac,H}$ are the parallel inductance and ac equivalent resistance. Figure 4b gives the main PWM waveforms and Figure 5 demonstrates the corresponding equivalent circuits at the reverse power flow operation.
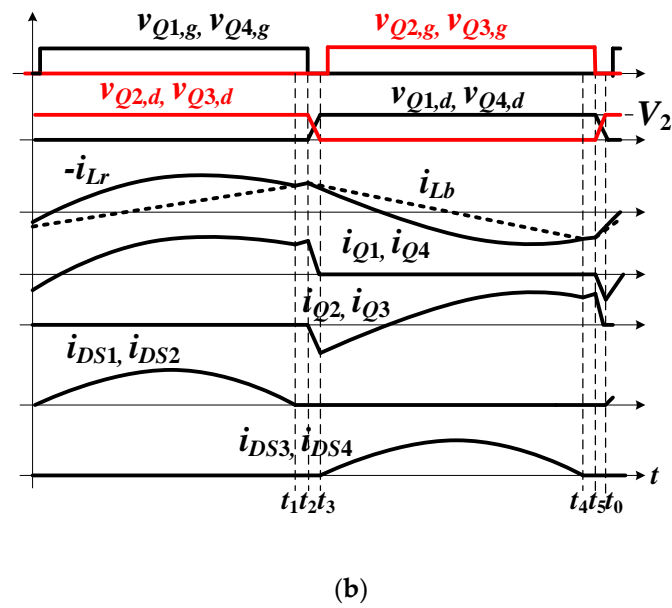

(a)

Figure 4. *Cont.*

(**b**)

Figure 4. The proposed circuit operated at reverse power flow (**a**) the equivalent *LLC* resonant circuit (**b**) PWM waveforms.
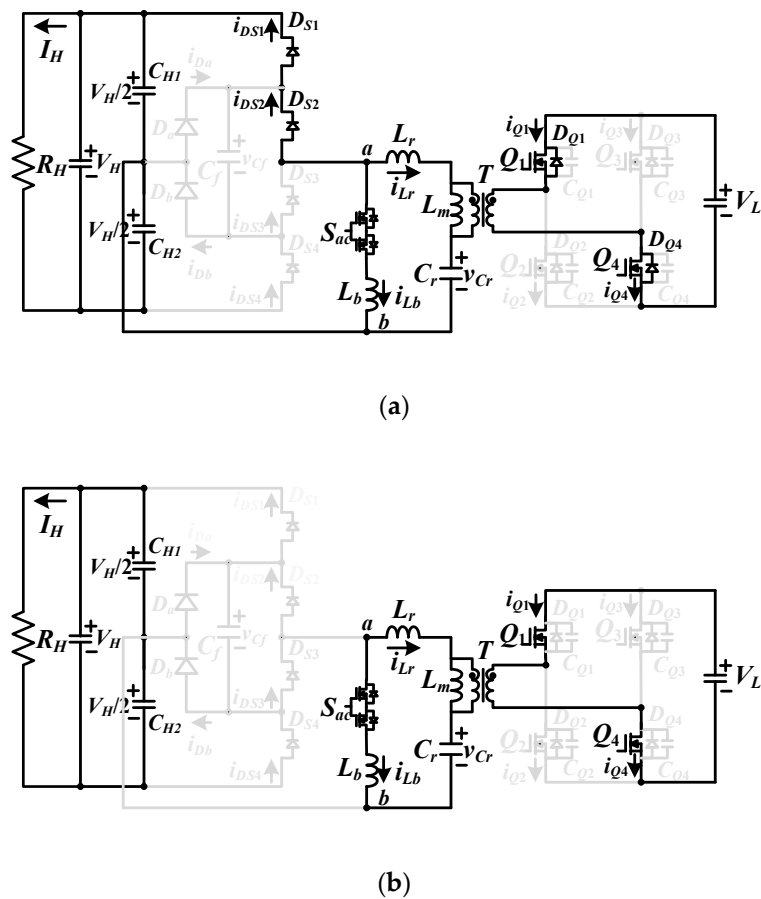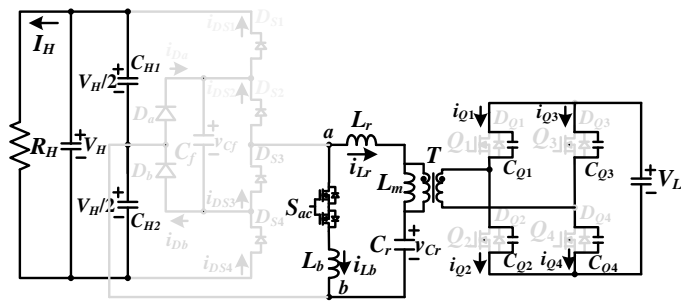

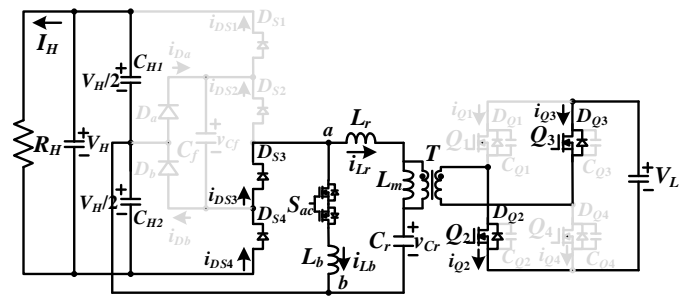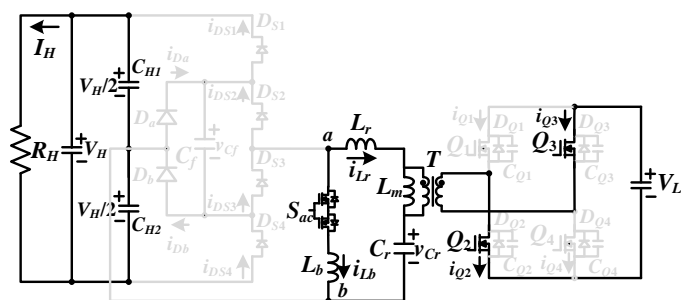(**a**)

(**b**)

Figure 5. *Cont.*

(**c**)

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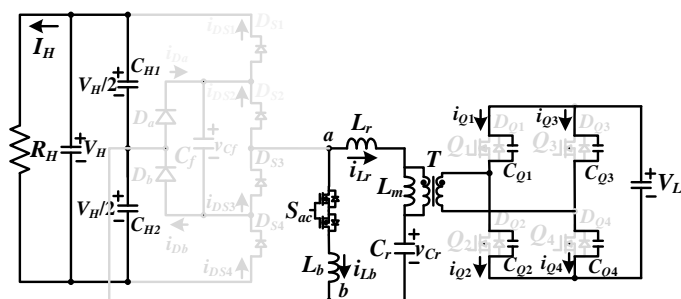
Figure 5. The corresponding equivalent circuits related to six operating steps under backward power transfer (**a**) step 1 circuit (**b**) step 2 circuit (**c**) step 3 circuit (**d**) step 4 circuit (**e**) step 5 circuit (**f**) step 6 circuit.

Step 1 ($t_0 \le t < t_1$): This step starts at t_0 when $v_{CQ4} = v_{CQ1} = 0$. Then, the D_{Q4} and D_{Q1} conduct and $v_{Q2,ds} = v_{Q3,ds} = V_L$. Due to D_{Q1} and D_{Q4} are conducting, $v_{Q4,ds}$ and $v_{Q1,ds} = 0$ and Q_1 and Q_4 can turn on under zero voltage. Due to $i_{Lr}(t_0) + i_{Lb}(t_0) < 0$, D_{S1} and D_{S2} are forward biased, C_{H1} is charged, $v_{Lm} = nV_L$, $v_{ab} = V_H/2$ and i_{Lm} and i_{Lb} both increase. Before switches Q_1 and Q_4 turn off, i_{DS1} and i_{DS2} will decrease to zero if $f_{sw} < f_r = 1/2\pi\sqrt{C_r L_r}$.

Step 2 ($t_1 \le t < t_2$): At time t_1, $i_{DS2} = i_{DS1} = 0$ and D_{S2} and D_{S1} are off. L_r, L_b, and C_r are series resonant at frequency $f_p = 1/2\pi\sqrt{C_r(L_b + L_r)}$.

Step 3 ($t_2 \le t < t_3$): Q_4 and Q_1 turn off at t_2. C_{Q2} and C_{Q3} are discharged in step 3. The ZVS condition of Q_3 and Q_2 are obtained in Equation (7).

$$(L_b + L_r)i^2_{Lb,p} + L_m i^2_{Lm,p} \ge 2C_Q V_L^2 \tag{7}$$

where $C_Q = C_{Q1} = .. = C_{Q4}$, $i_{Lm,p} \approx nV_L/(4L_m f_{sw})$ and $i_{Lb,p} \approx V_H/(8L_b f_{sw})$. At t_3, $v_{CQ3}(t_3) = v_{CQ2}(t_3) = 0$. The time interval Δt_{23} is expressed in Equation (8).

$$\Delta t_{23} \approx \frac{2V_L C_Q}{n[i_{Lm,p} + i_{Lb,p}]} = \frac{16 L_m L_b f_{sw} V_L C_Q}{n(2nL_b V_L + L_m V_H)} \le t_d \tag{8}$$

where t_d is dead time between Q_4 and Q_3 or Q_2 and Q_1.

Step 4 ($t_3 \le t < t_4$): Step 4 starts at t_3 when $v_{CQ2} = v_{CQ3} = 0$. Therefore, D_{Q3} and D_{Q2} conduct and Q_3 and Q_2 can turn on under zero voltage. In step 4, D_{S3} and D_{S4} conduct, $v_{ab} = -V_H/2$, $v_{Lm} = -nV_L$, and i_{Lm} and i_{Lb} both decrease.

Step 5 ($t_4 \le t < t_5$): $i_{DS3} = i_{DS4} = 0$ at t_4. In this step, Q_2 and Q_3 are still in the on state so that $v_{Lm} = -nV_L$. L_b, C_r and L_r are series resonant.

Step 6 ($t_5 \le t < T_{sw} + t_0$): Q_2 and Q_3 turn off at t_5. Then, C_{Q1} and C_{Q4} are discharged and $v_{CQ1} = v_{CQ4} = 0$ at $t_{sw} + t_0$.

The proposed converter has the similar operation principle for both forward and reverse power operation. For the reverse power operation, $Q_1 \sim Q_4$ are controlled as main power switches. $D_{S1} \sim D_{S4}$ are operated as diode rectifier to regulate voltage V_H. The resonant circuit including L_b, L_r and C_r is operated as a filter to suppress high order harmonics. The input *rms* voltage at fundamental frequency (Figure 4a) is calculated as $v_{Lm,rms} = 2\sqrt{2}nV_L/\pi$ and the ac equivalent resistance at high voltage side is $R_{ac,H} = 2R_H/\pi^2$. The *rms* voltage on v_{ab} is expressed as $v_{ab,rms} = \sqrt{2}V_H/\pi$. Components $R_{ac,H}$, L_b, L_r and C_r are resonant. The transfer function $G_{L\_H}(s)$ and gain $|G_{L\_H}(s)|$ are calculated in Equations (9) and (10), respectively.

$$G_{L\_H}(s) = \frac{v_{ab,rms}(s)}{v_{Lm,rms}(s)} = \frac{\frac{sL_b R_{ac,H}}{sL_b + R_{ac,H}}}{\frac{sL_b R_{ac,H}}{sL_b + R_{ac,H}} + \frac{1}{sC_r} + sL_r} \tag{9}$$

$$\left|G_{L\_H}(F)\right| = \frac{K_2 F^2}{\sqrt{[(F^2 - 1)Q_2 K_2 F]^2 + [F^2(K_2 + 1) - 1]^2}} \tag{10}$$

where $F = f_{sw}/f_r$, $f_r = 1/(2\pi\sqrt{L_r C_r})$, $K_2 = L_b/L_r$ and $Q_2 = \sqrt{L_r/C_r}/R_{ac,H}$. From the given input voltage V_H, output voltage V_L and the circuit parameters L_r, C_r, L_b and R_H, the switching frequency is obtained from Equation (10).

4. Circuit Parameters and Test Results

For forward power transfer, the input and output voltages are $V_H = 750$ V to 800 V and $V_L = 48$ V. The rated power is 1440 W ($v_L = 48$ V and $I_L = 30$ A). For reverse power transfer, the input and output voltages are $V_L = 36$ V to 52 V and $V_H = 800$ V. The transfer functions in Equations (6) and (10) for forward and backward power transfer operations are similar. Thus, the circuit parameters design operated at forward power flow is presented in this section. The dc voltage gain under $V_H = 800$ V

input and $V_{L,max}$ = 52 V output is designed to be unity. The transformer turns ratio is calculated in Equation (11).

$$n = |G_{H\_L}| \times \frac{V_{H,max}}{2V_{L,max}} \approx 7.7 \tag{11}$$

In the prototype circuit, the selected primary and secondary turns are n_H = 48 and n_L = 6. Thus, the actual transformer turns ratio is $n = n_H/n_L$ = 8. With the adopted turns ratio, the actual maximum and minimum voltage gains at $V_{L,nom}$ = 48 V condition are given in Equations (12) and (13).

$$|G_{H\_L}|_{max} = \frac{2nV_{L,nom}}{V_{H,min}} \approx 1.024 \tag{12}$$

$$|G_{H\_L}|_{min} = \frac{2nV_{L,nom}}{V_{H,max}} \approx 0.96 \tag{13}$$

The control parameters K_1 and Q_1 can be selected at full load $P_{L,full}$ and minimum input voltage $V_{H,min}$ conditions. To reduce circulating current, the inductor ratio K_1=10 is used in this prototype circuit. For Q_1 = 0.38 and K_1 = 10, it can obtain the peak gain of $|G_{H\_L}(s)|$ is 1.13. The ac equivalent resistance $R_{ac,L}$ at the rated power is obtained in Equation (14).

$$R_{ac,L} = \frac{8n^2}{\pi^2}R_L = \frac{8 \times (48/6)^2}{3.14159^2} \times \frac{48}{30} \approx 83\Omega \tag{14}$$

The circuit parameters $C_r = 1/2\pi Q_1 f_r R_{ac,L} \approx 50$ nF and $L_r = 1/(2\pi f_r)^2 C_r \approx 50$ μH under f_r = 100 kHz. The actual resonant inductance and capacitance are C_r = 47 nF and L_r = 54 μH and the magnetizing inductance $L_m = K_1 L_r = 540$ μH. The theoretical primary *rms* current is calculated as:

$$I_{pri,rms} = \frac{\pi I_o}{2\sqrt{2}n} \approx 4.2 \text{ A} \tag{15}$$

The theoretical minimum switching frequency is obtained as $f_{sw,min} = 1/2\pi \sqrt{C_r(L_r + L_m)} \approx 30$ kHz. The minimum switching frequency will result in the maximum *rms* magnetizing current.

$$I_{Lm,rms} = \frac{1}{2\sqrt{3}}\frac{nV_L}{4f_{sw,min}L_m} \approx 1.7 \text{ A} \tag{16}$$

Therefore, the *rms* resonant inductor current is obtained in Equation (17).

$$I_{Lr,rms} = \sqrt{I_{Lm,rms}^2 + I_{pri,rms}^2} \approx 4.53 \text{ A} \tag{17}$$

The flying capacitor C_f is used to realize voltage balance of C_{H1} and C_{H2} so that $V_{CH1} = V_{CH2} = V_H/2$. The theoretical voltage stresses of power semiconductors can be calculated as $v_{S1,stress} = .. = v_{S4,stress} = V_{H,max}/2 = 400$ V and $v_{Q1,stress} = .. = v_{Q4,stress} = V_{L,max} = 52$ V. The switch currents approximate $I_{S1,rms} = .. = I_{S4,rms} \approx I_{Lr,rms}/\sqrt{2} \approx 3.2$ A and $I_{Q1,rms} = .. = I_{Q4,rms} \approx \pi I_o/4 \approx 23.6$ A. Power devices $S_1 \sim S_4$ are implemented using IRG4PC40W with 600 V/20 A rating. Power switches $Q_1 \sim Q_4$ are implemented using IRFB3307 with 75 V/150 A rating. S_{ac} is implemented using two G20N50C with 500 V/20 A rating. The parallel inductor L_b is selected as 230 μH and $K_2 = L_b/L_r = 4.25$ under reverse power flow operation. The clamp diodes D_a and D_b are implemented with ultrafast recovery diodes HFA15TB60PBF with 600 V/15 A rating. The other circuit parameters used in the prototype are $C_{H1} = C_{H2} = 330$ μF/400 V, $C_f = 2.2$ μF/630 V and $C_L = 4400$ μF/100 V. The parameters and specifications used in the laboratory prototype are given in Table 1.

Table 1. Parameters and specifications of the presented converter.

Items	Parameter
High voltage V_H	750 V~800 V
Low voltage V_L	48 V
Rated power P_o	1440 W
Resonant frequency f_r	100 kHz
High-side capacitances C_{H1}, C_{H2}	330 µF/400 V
Low-side capacitance C_L	4400 µF/100 V
Resonant capacitance C_r	47 nF
Flying capacitance C_f	2.2 µF
Resonant inductance L_r	54 µH
Parallel inductance L_b	230 µH
Power switches S_1~S_4	IRG4PC40W (600 V/20 A)
Power switches Q_1~Q_4	IRFB3307 (75 V/150 A)
Power switch S_{ac}	G20N50C (500 V/20 A)
Clamp diodes D_a, D_b	HFA15TB60PBF (600 V/15 A)
Winding turns of T: n_H, n_L	48, 6
Magnetizing inductance L_m	540 µH

Figures 6–10 provide the test results for forward power operation and Figures 11–14 provide the measured waveforms for reverse power operation. The PWM signals of S_1–S_4 at 100% load are presented in Figure 6. S_1 (S_3) and S_2 (S_4) have the same gate-to-source voltage signals. The converter at V_H = 750 V input has less switching frequency than V_H = 800 V input condition. Figure 7 gives the experimental results of leg voltage v_{ab}, i_{Lr} and v_{Cr} at 100% load. It can be seen that the measured waveforms i_{Lr} and v_{Cr} are almost the sinusoidal waves due to f_{sw} close to f_r for both 750 V and 800 V inputs. Figure 8 shows the experimental results of V_{CH1}, V_{CH2}, V_{Cf}, V_{Da} and V_{Db}. The dc voltage differences between V_{CH1}, V_{CH2} and V_{Cf} are about 5V. Figure 9 demonstrates the switch currents of Q_1–Q_4 at 100% load. Figure 10 illustrates the PWM waveforms of S_1–S_4 at 20% load. It can observe that S_1–S_4 all turn on under ZVS at 20% load. Figure 11 gives the PWM signals of Q_1~Q_4 under backward power operation and different input voltages. Power devices Q_1 (Q_2) and Q_4 (Q_3) have the same gate-to-source voltage signals. Figure 12 illustrates the measured results of i_{Lr}, i_{Lb} and v_{Cr} under for reverse power operation. The parallel inductor current i_{Lb} is similar to the magnetizing current on conventional *LLC* resonant converter to achieve voltage step-up capability. Figure 13 shows the measured capacitor voltages V_{Cf}, V_{CH1} and V_{CH2} on the high voltage side. These three voltages V_{CH1}, V_{CH2} and V_{Cf} are almost balanced with about 7 V voltage difference. Figure 14 gives the measured PWM waveforms of Q_1~Q_4 under 20% load. It can observe that Q_1–Q_4 can turn on under zero voltage at 20% load. For forward power operation (buck mode), the measured circuit efficiencies are 89.7% at 20% load, 92.1% at 50% load and 91.8% at 100% load under 800 V input. For reverse power operation (boost mode), the measured circuit efficiencies are 86.3% at 20% load, 89.4% at 50% load and 88.9% at 100% load under 40 V input case. Figure 15a gives the picture of the prototype circuit and the experimental setup is given in Figure 15b.
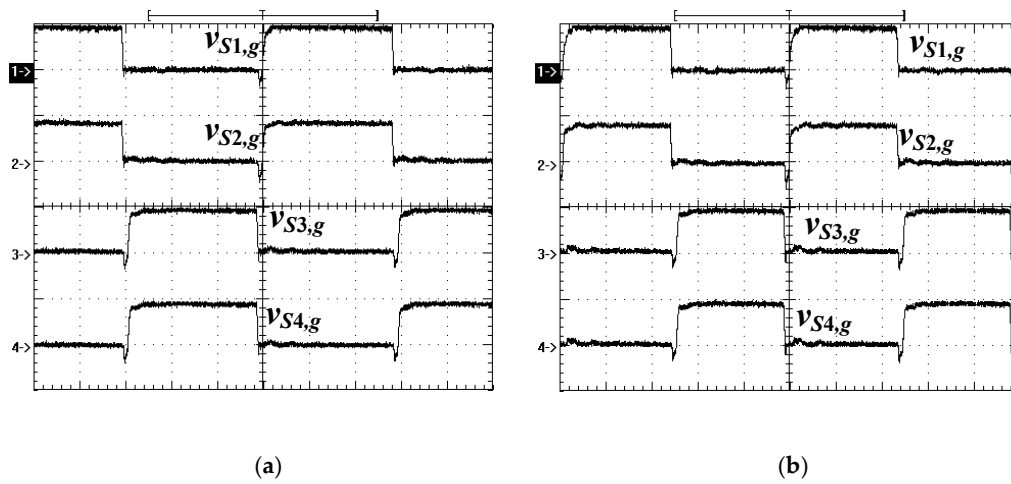
(**a**)　　　　　　　　　　　　　　(**b**)

Figure 6. Measured PWM signals of S_1–S_4 at full load (**a**) $V_H = 750$ V (**b**) $V_H = 800$ V ($v_{S1,g}$~$v_{S4,g}$: 10 V/div; time: 2 μs).
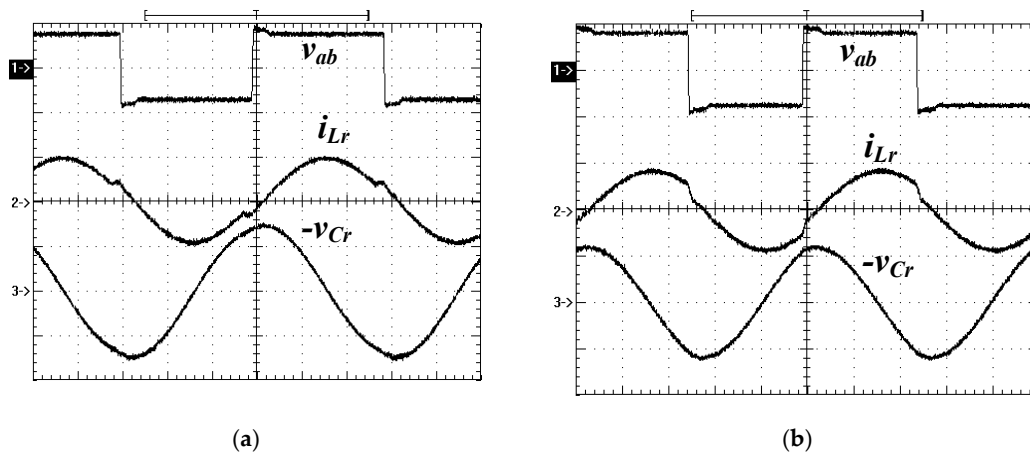

(**a**)　　　　　　　　　　　　　　(**b**)

Figure 7. Measured results of v_{ab}, i_{Lr} and v_{Cr} at full load (**a**) $V_H = 750$ V (**b**) $V_H = 800$ V (v_{ab}: 500V/div; i_{Lr}: 10 A/div; v_{Cr}: 200 V/div; time: 2 μs).
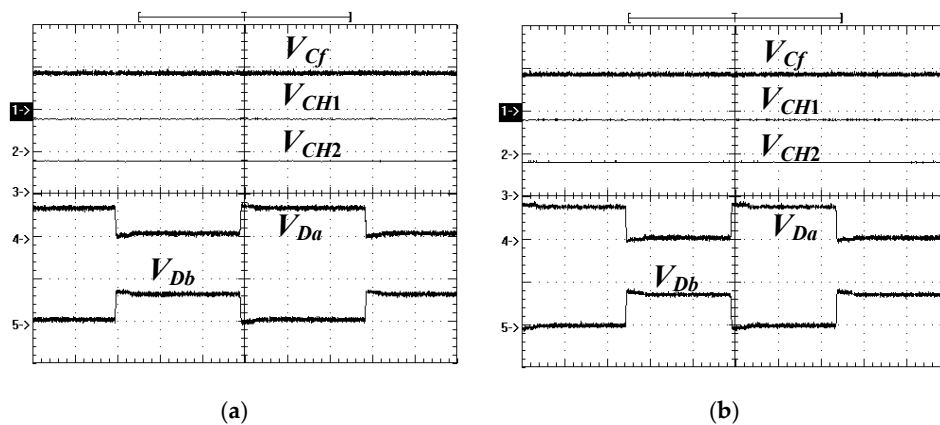

(**a**)　　　　　　　　　　　　　　(**b**)

Figure 8. Measured results of V_{Cf}, V_{CH1}, V_{CH2}, V_{Da} and V_{Db} at full load (**a**) $V_H = 750$ V (**b**) $V_H = 800$ V (v_{Cf}, V_{CH1}, V_{CH2}, V_{Da}, V_{Db}: 500 V/div; time: 2 μs).

Figure 9. Measured switch currents of Q_1–Q_4 under full load (**a**) $V_H = 750$ V (**b**) $V_H = 800$ V ($-i_{Q1} \sim -i_{Q4}$: 50 A/div; time: 2 μs).
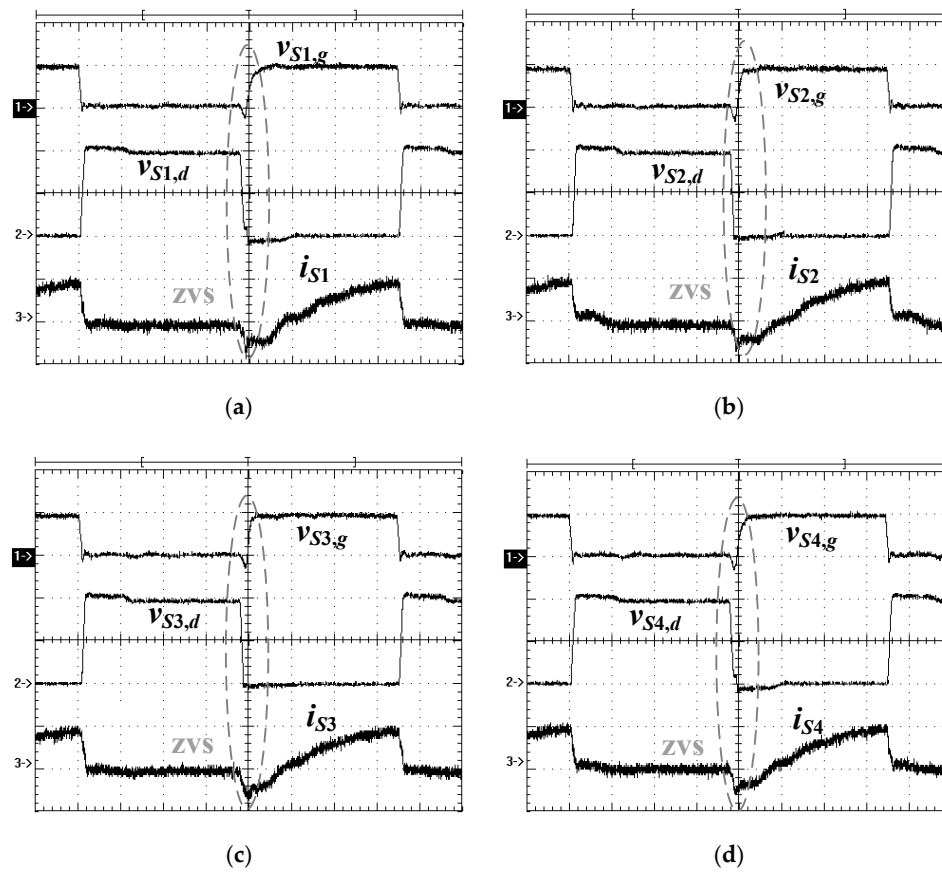

Figure 10. Measured PWM waveforms of S_1–S_4 at 20% load (**a**) S_1 waveforms (**b**) S_2 waveform (**c**) S_3 waveform (**d**) S_4 waveform ($v_{S1,g}$–$v_{S4,g}$: 10 V/div; $v_{S1,d}$–$v_{S4,d}$: 200 V/div; $i_{S1} \sim i_{S4}$: 2 A/div; time: 1 μs).
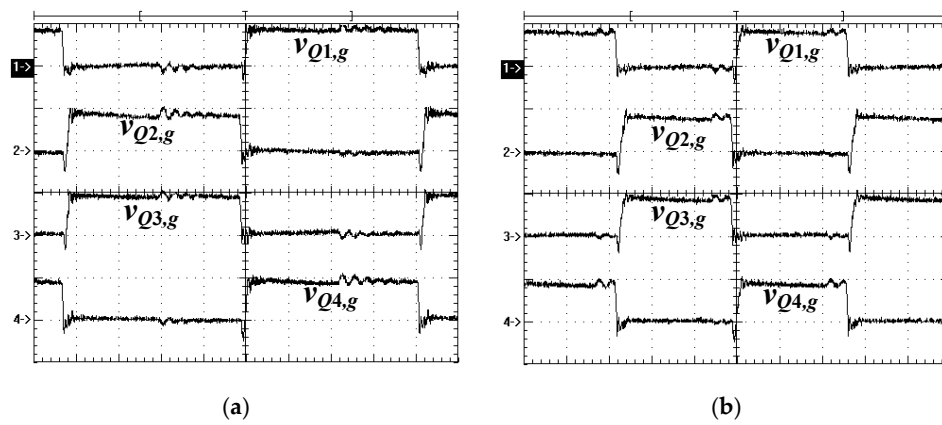
Figure 11. Measured PWM signals of $Q_1 \sim Q_4$ for reverse power operation and full load (**a**) $V_L = 36$ V (**b**) $V_L = 52$ V ($v_{Q1,gs} \sim v_{Q4,gs}$: 10 V/div; time: 2 µs).
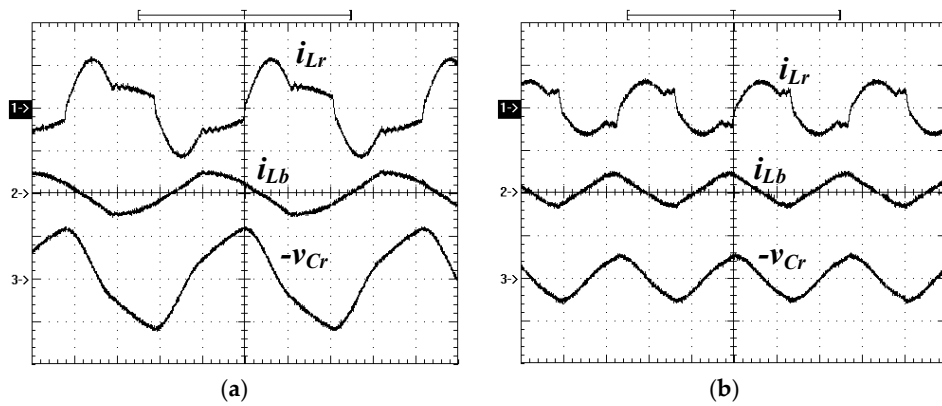

Figure 12. Measured results of i_{Lr}, i_{Lb} and v_{Cr} for reverse power operation and full load (**a**) $V_L = 36$ V (**b**) $V_L = 52$ V (i_{Lr}, i_{Lb}: 10 A/div; v_{Cr}: 500 V/div; time: 4 µs).
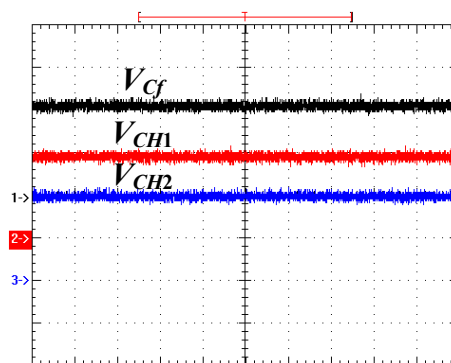

Figure 13. Measured results of V_{Cf}, V_{CH1}, and V_{CH2} under reverse power operation and full load (v_{Cf}, V_{CH1}, V_{CH2}, V_{Da}, V_{Db}: 200 V/div; time: 4 µs).
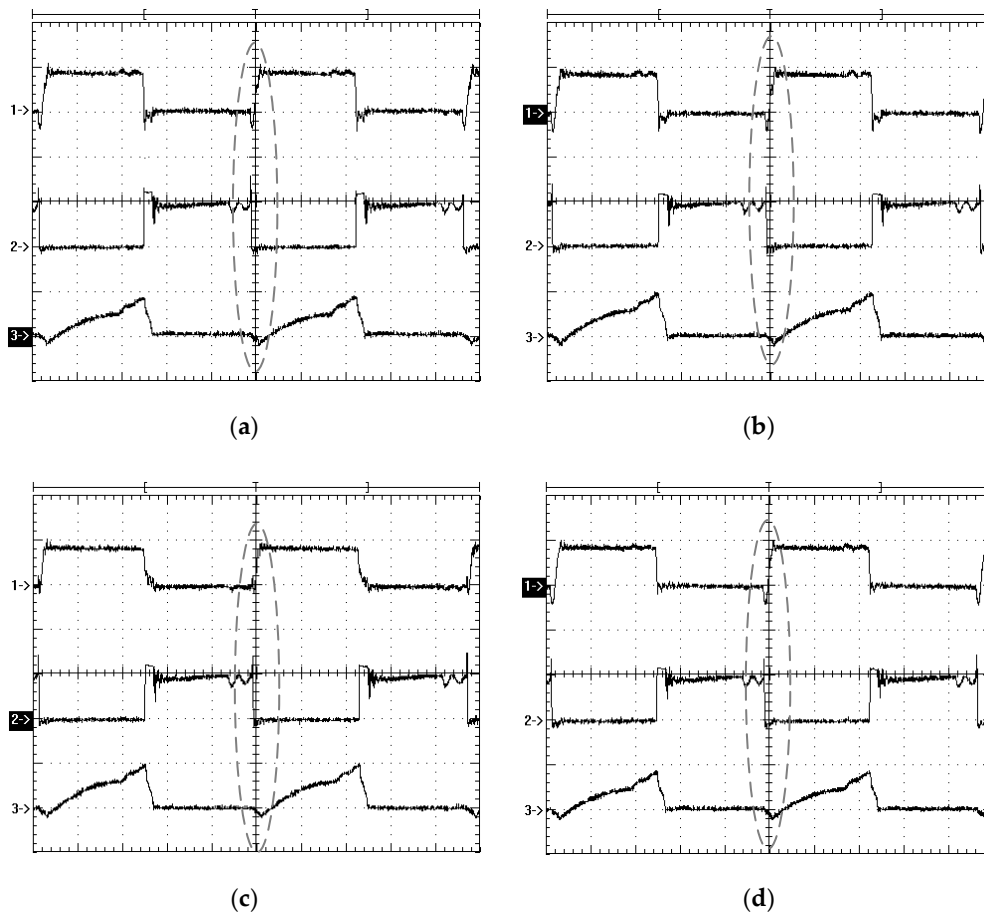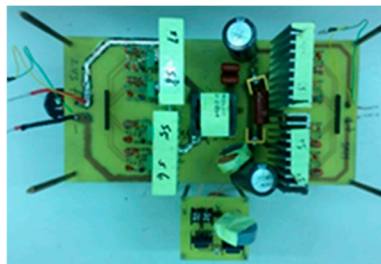
(**a**) (**b**)

(**c**) (**d**)

Figure 14. Measured waveforms of power devices $Q_1 \sim Q_4$ under reverse power operation and 20% load (**a**) Q_1 waveform (**b**) Q_2 waveform (**c**) Q_3 waveform (**d**) Q_4 waveform ($v_{Q1,g}$–$v_{Q4,g}$: 10 V/div; $v_{Q1,d}$–$v_{Q4,d}$: 50 V/div; i_{Q1}–i_{Q4}: 20 A/div; time: 2 μs)

(**a**) (**b**)

Figure 15. Pictures of the presented circuit: (**a**) prototype circuit; (**b**) experimental setup.

5. Conclusions

A new three-level resonant converter is proposed, analyzed, and discussed to realize bidirectional power transfer and soft switching operation capability. A three-level diode clamp series resonant converter is used on the high-voltage side to have low voltage rating on active devices. For forward power operation, the conventional *LLC* circuit is selected to have ZVS operation on all power switches. Full-wave rectifier with synchronous switches is adopted on the low-voltage side to reduce conduction loss on power semiconductors. To overcome the low voltage gain problem on conventional *LLC* converter under reverse power operation, a parallel inductor is connected to the leg terminal of three-level diode-clamp resonant converter. Thus, the proposed converter can achieve voltage step-up and step-down for forward and reverse power operation by using PFM scheme. Compared to the

bidirectional *LLC* circuit [15], the proposed converter can achieve ZVS operation for both power flow directions. Compared to the symmetric *LLC* converters in [16–18], the proposed *LLC* converter has less freewheeling current on primary-side for forward power operation. However, one ac switch is needed in the studied circuit compared to conventional bidirectional *LLC* circuit topology. Finally, the theoretical analysis is confirmed by experiments with a laboratory prototype.

References

1. Lin, B.-R.; Zhuang, Y.-S. Hybrid resonant converter with three half-bridge legs for wide voltage operation. *Appl. Sci.* **2020**, *10*, 310. [CrossRef]
2. Lin, B.-R.; Lin, G.-H. DC converter with wide soft switching operation, wide input voltage and low current ripple. *Appl. Sci.* **2020**, *10*, 4672. [CrossRef]
3. Jing, W.; Lai, C.H.; Wong, S.H.W.; Wong, M.L.D. Battery-super capacitor hybrid energy storage system in standalone dc microgrids: A review. *IET Renew. Power Gener.* **2017**, *11*, 461–469. [CrossRef]
4. Guerrero, J.M.; Loh, P.C.; Lee, T.-L.; Chandorkar, M. Advanced Control Architectures for Intelligent Microgrids—Part II: Power Quality, Energy Storage, and AC/DC Microgrids. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1263–1270. [CrossRef]
5. Lin, B.-R.; Dai, C.-X. Wide voltage resonant converter using a variable winding turns ratio. *Electronics* **2020**, *9*, 370. [CrossRef]
6. Meng, L.; Shafiee, Q.; Trecate, G.F.; Karimi, H.; Fulwani, D.; Lu, X.; Guerrero, J.M. Review on control of DC microgrids and multiple microgrid clusters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2017**, *5*, 928–948.
7. Emadi, A.; Lee, Y.J.; Rajashekara, K. Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2237–2245. [CrossRef]
8. Zhang, Y.; Gao, Y.; Li, J.; Sumner, M. Interleaved switched-capacitor bidirectional dc-dc converter with wide voltage-gain range for energy storage systems. *IEEE Trans. Power Electron.* **2018**, *33*, 3852–3869. [CrossRef]
9. Shen, C.-L.; Shen, Y.-S.; Chiu, P.-C.; Liang, T.-C. Isolated bidirectional converter with minimum active switches for high-voltage ratio achievement and micro-grid applications. *IET Power Electron.* **2017**, *10*, 2208–2216. [CrossRef]
10. Mangu, B.; Akshatha, S.; Suryanarayana, D.; Fernandes, B.G. Grid-connected PV-wind-battery-based multi-input transformer-coupled bidirectional dc-dc converter for household applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 1086–1095. [CrossRef]
11. Yilmaz, M.; Krein, P.T. Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles. *IEEE Trans. Power Electron.* **2013**, *28*, 2151–2169. [CrossRef]
12. Ahrabi, R.R.; Ardi, H.; Elmi, M.; Ajami, A. A novel step-up multiinput DC-DC converter for hybrid electric vehicles application. *IEEE Trans. Power Electron.* **2017**, *32*, 3549–3561. [CrossRef]
13. Xu, D.; Zhao, C.; Fan, H. A PWM plus phase-shift control bidirectional DC-DC converter. *IEEE Trans Power Electron.* **2004**, *19*, 666–675. [CrossRef]
14. Tao, H.; Kotsopoulos, A.; Duarte, J.L.; Hendrix, M.A.M. Family of multiport bidirectional DC-DC converters. *IEE Proc. Electr. Power Appl.* **2006**, *153*, 451–458. [CrossRef]
15. Pledl, G.; Tauer, M.; Buecherl, D. Theory of operation, design procedure and simulation of a bidirectional LLC resonant converter for vehicular applications. In Proceedings of the IEEE Vehicle Power and Propulsion Conference (VPPC 2010), Lille, France, 1–3 September 2010; pp. 1–5.
16. Tan, K.; Yu, R.; Guo, S.; Huang, A.Q. Optimal design methodology of bidirectional LLC resonant DC/DC converter for solid state transformer application. In Proceedings of the IECON 2014—40th Annual Conference of the IEEE Industrial Electronic Society, Dallas, TX, USA, 29 October–1 November 2010; pp. 1657–1664.

17. Jiang, T.; Zhang, J.; Wu, X.; Sheng, K.; Wang, Y. A bidirectional LLC resonant Converter with automatic forward and backward mode transition. *IEEE Trans. Power Electron.* **2015**, *30*, 757–770. [CrossRef]

18. Kim, E.-S.; Park, J.-H.; Jeon, Y.-S.; Kong, Y.-S.; Lee, S.-M.; Kim, K. Bidirectional secondary LLC resonant converter using auxiliary switches and inductor. In Proceedings of the 2014 IEEE Applied Power Electronics Conference and Exposition—APEC 2014, Fort Worth, TX, USA, 16–20 March 2014; pp. 1941–1947.