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Design Methodology of the Class-E Power Amplifier with Finite Feed Inductance—A Tutorial Approach

Ingrid Casallas , Carlos-Ivan Paez-Rueda , Gabriel Perilla , Manuel Pérez and Arturo Fajardo * 

Department of Electronic Engineering, Pontificia Universidad Javeriana, Bogotá 110311, Colombia; ingrid.casallas@javeriana.edu.co (I.C.); paez.carlos@javeriana.edu.co (C.-I.P.-R.); gabriel.perilla@javeriana.edu.co (G.P.); manuel.perez@javeriana.edu.co (M.P.)

* Correspondence: fajardo@javeriana.edu.co

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Abstract: The Class-E with finite feed inductance is a high-efficiency power amplifier that generally uses complex, long, and iterative design procedures. In this paper, we detail a design methodology that is based on an analytical model of this amplifier. This methodology explores the power amplifier design by the use of a symbolic mathematical tool, which was developed in the software Maple™. This approach helps to understand the Class-E circuit topology and it offers a fast and easy design procedure without having to examine, in-depth, the model analytical equations.

Keywords: Class-E; circuit design; power amplifiers; high-efficiency amplifier

1. Introduction

The Class-E power amplifier is a tuned switching Power Amplifier (PA), which is commonly used in Radio-Frequency (RF) applications. It uses a single switch element and a tuned reactive network between its power stage and its load. Furthermore, it achieves an ideal power efficiency of 100% under Zero Voltage Switching (ZVS) and Zero Voltage Derivative Switching (ZVDS) conditions. The circuit topology and its main waveforms are shown in Figures 1 and 2, respectively. This PA is used in many applications, such as wireless power transmission [1], dedicated short-range communications [2], low-power RF devices [3], induction heater systems [4], plasma generators [5], and street-lighting [6].

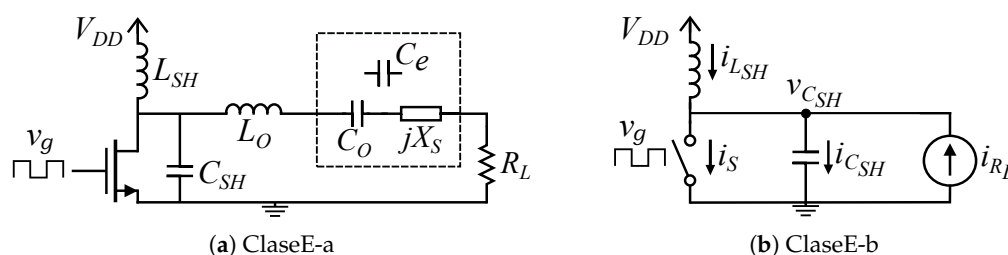


Figure 1. Class-E PA (a) Ideal model. (b) High Q_L model.

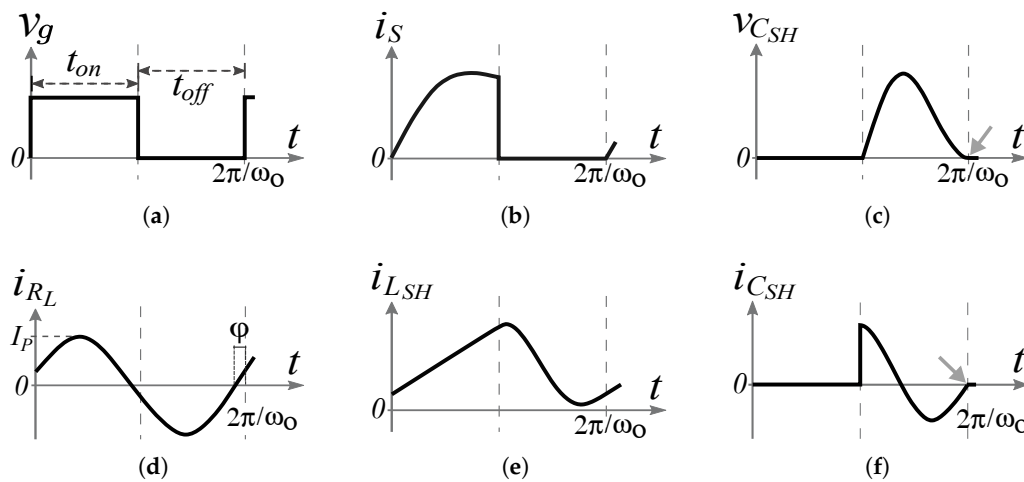


Figure 2. Waveforms of Class-E PA. (a) Switch-driver voltage. (b) Switch current. (c) Switch voltage. (d) Load resistance current. (e) L_{SH} current. (f) C_{SH} current.

The Class-E amplifier was introduced by Ewing in 1964, as a high-efficiency RF amplifier [7]. Since then, this PA has been analyzed in several works [8–21]. In contrast to the original implementation with RF choke inductors for Direct Current (DC) feeding, the use of a finite inductance offers a higher degree of freedom, a feature that is particularly useful in applications with size constraints, because it allows for the reduction of the inductor size [16]. For instance, in [19], the authors design a Class-E with Finite DC Feed Inductance (FDI) that is based on an integrated split inductor. Additionally, their design involves the breakdown limit of the integrated switch as a design restriction and it maximizes the PA output power under ZVS and ZVDS conditions while using an analytical model of the Class-E PA with FDI. Furthermore, to the best of our knowledge, the use of this topology has been concentrated only on applications in which the conventional topology (i.e., with RF choke) cannot be implemented (e.g., VLSI and RF applications).

In general, the Class-E with FDI models are more complex than the Class-E conventional models [15]. In particular, the conventional models assumed the feed current as a DC current that results in simple analytical equations [7], while in the Class-E with FDI models considered the current behavior into the circuit analysis [17]. Furthermore, some published models set the duty cycle (D) of the commutation signal to a fixed value (e.g., 0.5), which simplifies the amplifier model and design equations [12,15]. Following another simplification approaches, in [17,18], the authors assumed a high loaded quality factor and ideal components (i.e., ideal switch, inductors, and capacitors with infinite quality factor) to model the Class-E with FDI through analytical equations, which allows for an easy design procedure with mathematical software tools. However, the designer needs to implement the PA model in a software tool without some insight into its analytical equations expressed as explicit functions of the model variables and without a detailed procedure for obtaining these equations, because they were not reported in [17,18]. Only after overcoming this challenge, the designer could optimize the Class-E with FDI to a particular application by an exhaustive exploration of the design space when considering the involved trade-offs between the design specifications and restrictions [19].

The design of the Class-E PA with FDI has been explored in several works [11,12,16–20,22–25]. In general, the complexity of the circuit design of the Class-E with FDI is higher than the calculation of conventional Class-E components in order to guarantee ZVS and ZVDS operation. This design process involves multivariable equations with high complexity solutions which could require iterative procedures to achieve the given specifications and restrictions [13,15–20,25–27]. In [11–13], the authors design a Class-E with FDI using an iterative design approach, which involves time-consuming procedures. On one hand, these procedures usually involve a phase of tuning components to achieve the ZVS and ZVDS conditions [21,28,29]. On the other hand, other models, like the

ones proposed in [17,18], provide accurate analytic equations, which avoid iterative solutions with lower accuracy predictions under high values of parasitic elements of the amplifier components. The model that is presented in [17] considers two design parameters, which are D and the resonance frequency mismatch (q). The model proposed in [18] considers three design parameters: D , q , and the normalized slope of the switch voltage (S). The S parameter allows for defining three operation modes: non-ZVS, suboptimal operation (i.e., ZVS and non-ZVDS), and optimal operation (i.e., ZVS and ZVDS).

Commonly, the design equations synthesized from these analytical models are summarized into a set of math expressions that establish a link between circuit components and input parameters, these expressions are called the PA design set [17–19]. Under the amplifier optimal operation, the design set proposed by [17–19] is the same, and it allows the calculation of a large number of possible combinations of the circuit parameters, which guarantee the ZVS and ZVDS operation of the ideal Class-E with FDI under the specifications and restrictions of the particular application. However, this set is not widely used perhaps, because the model implementation demands extensive mathematical development, and to the best knowledge of the authors, a systematic methodology to explore the freedom of this analytical model is not reported, in particular with the possibility to analyze the design space when considering the involved trade-offs between design specifications and restrictions.

This paper proposes a novel design methodology of the Class-E with FDI based on the analytical model that was proposed by [17,19]. Furthermore, to simplify its adoption by the academic and scientific community, we share the PA model implementation, and the code used to apply the proposed method. In addition, this paper has been written following a tutorial approach to motivate related engineers and students with basic knowledge in circuit theory in order to integrate these amplifiers in their projects by following this paper (and its additional material) as a practical handbook. We devote particular attention to the selected examples to present the impact of the proposed methodology to optimize the PA. The outline of this paper is as follows. Section 2 presents the Class-E PA modeling and design equations. Section 3 describes the design methodology and explains two design approaches. Section 4 shows four design study cases. Finally, in Sections 5 and 6, the conclusions and the future work are presented.

2. PA Model and Design Set

2.1. PA Model

The Class-E is a power amplifier that reduces the switching losses by turning on the switch with zero voltage and zero current in the C_{SH} capacitor (i.e., ZVS and ZVDS operation), as illustrated in Figure 2c,f, respectively. This PA is fed by a DC source (V_{DD}) and a pulsed source (v_g) with a fundamental frequency f_0 . Furthermore, it supplies the power that is delivered to its load (R_L) in a narrow band centered in f_0 while using a quasi-tuned LC circuit, where the natural resonant frequency is

$$\omega_e = \frac{1}{\sqrt{L_0 C_e}} = \frac{1}{\sqrt{L_0 C_0}} + \Delta\omega = 2\pi f_0 + \Delta\omega \quad (1)$$

where $\Delta\omega$ is the frequency offset necessary to guarantee the ZVS and ZVDS operation. In the ideal Class-E PA model, the quality factor of the storage elements is infinite. The switch has: zero on-resistance, infinite off-resistance, and zero rise and fall commutation times. Under these assumptions, and supposing a high value of Q_L , the Class-E PA with FDI circuit model could be simplified to the one that is shown in Figure 1b. The current I_{RL} is out of phase by an angle φ regarding the voltage v_g (Figure 2d), and it is related to the load power (P_{out}) by

$$i_{RL}(t) = I_p \sin(2\pi f_0 t + \varphi) = \sqrt{\frac{2P_{out}}{R_L}} \sin(\omega_0 t + \varphi). \quad (2)$$

In the time intervals when the switch is on (t_{on}) and off (t_{off}), the main waveforms of the PA are predicted by the following equations [17,19]

$$i_{C_{SHon}}(t) = v_{C_{SHon}}(t) = 0 \quad (3)$$

$$i_{S_{on}}(t) = \frac{V_{DD}}{L_{SH}}t - I_p \sin(\varphi) + I_p \sin(\omega_o t + \varphi) \quad (4)$$

$$i_{L_{SHon}}(t) = \frac{V_{DD}}{L_{SH}}t - I_p \sin(\varphi) \quad (5)$$

$$i_{S_{off}}(t) = 0 \quad (6)$$

$$i_{L_{SHoff}}(t) = \frac{V_{DD}}{L_{SH}}t - I_p \sin(\varphi) - \frac{1}{L_{SH}} \int_{\frac{2\pi D}{\omega_o}}^t v_{C_{SH}} d\tau \quad (7)$$

$$i_{C_{SHoff}}(t) = \frac{V_{DD}}{L_{SH}}t + I_p (\sin(\omega_o t + \varphi) - \sin(\varphi)) - \frac{1}{L_{SH}} \int_{\frac{2\pi D}{\omega_o}}^t v_{C_{SH}} d\tau \quad (8)$$

$$v_{C_{SHoff}}(t) = V_{DD} \left(\frac{C1}{V_{DD}} \cos(q\omega_o t) + \frac{C2}{V_{DD}} \sin(q\omega_o t) + 1 - \frac{q^2}{1-q^2} p \cos(\omega_o t + \varphi) \right) \quad (9)$$

where

$$q = \frac{1}{\omega_o \sqrt{L_{SH} C_{SH}}} \quad (10)$$

$$D = \frac{t_{on}}{T} = t_{on} f_o \quad (11)$$

$$p = \frac{\omega_o L_{SH}}{V_{DD}/I_p} = \frac{\omega_o L_{SH}}{\sqrt{R_L \cdot R_{DC}}} \quad (12)$$

The variable p is the ratio between the impedance of L_{SH} at the operation frequency and the geometric mean of the resistance that the amplifier shows to the power supply (R_{DC}) and its load (R_L). The constants $C1$ and $C2$ are related to the solution of the involved differential equation. It is important to notice that the variable q cannot take the value of 1 because of the mathematical singularity that is introduced by (9). Furthermore, under ZVS and ZVDS conditions, φ , p , $C1$, and $C2$ could be expressed as a function of D and q variables [17]

$$\varphi = \arctan \left(\frac{b_1 c_2 - b_2 c_1}{\pm \sqrt{(a_1 c_2 - a_2 c_1)^2 + (b_1 c_2 - b_2 c_1)^2}}, \frac{a_1 c_2 - a_2 c_1}{\pm \sqrt{(a_1 c_2 - a_2 c_1)^2 + (b_1 c_2 - b_2 c_1)^2}} \right) \quad (13)$$

$$p = \frac{\pm \sqrt{(a_1 c_2 - a_2 c_1)^2 + (b_1 c_2 - b_2 c_1)^2}}{a_2 b_1 - a_1 b_2} \quad (14)$$

$$C1 = p V_{DD} \left(\frac{q^2}{1-q^2} \cos(2q\pi) \cos(\varphi) + \frac{q}{1-q^2} \sin(2q\pi) \sin(\varphi) \right) - V_{DD} \cos(2q\pi) \quad (15)$$

$$C2 = p V_{DD} \left(\frac{q^2}{1-q^2} \sin(2q\pi) \cos(\varphi) - \frac{q}{1-q^2} \cos(2q\pi) \sin(\varphi) \right) - V_{DD} \sin(2q\pi) \quad (16)$$

where

$$a_1 = 1 - \frac{1}{q^2 - 1} \cos(q2\pi(D-1)) + \frac{q^2}{q^2 - 1} \cos(2\pi D) \quad (17)$$

$$b_1 = -\frac{1}{q^2 - 1} \sin(q2\pi(D-1)) - \frac{q^2}{q^2 - 1} \sin(2\pi D) \quad (18)$$

$$c_1 = 2\pi D - \frac{1}{q} \sin(q2\pi(D-1)) \quad (19)$$

$$a_2 = \frac{q}{q^2 - 1} \sin(q2\pi(D - 1)) - \frac{q^2}{q^2 - 1} \sin(2\pi D) \quad (20)$$

$$b_2 = -\frac{q}{q^2 - 1} \cos(2\pi D) - \frac{q^2}{q^2 - 1} \cos(q2\pi(D - 1)) \quad (21)$$

$$c_2 = 1 - \cos(q2\pi(D - 1)). \quad (22)$$

2.2. Design Set of the Ideal Class-E PA

Commonly, the conventional design set K of the ideal Class-E PA is composed of four equations (i.e., K_P , K_L , K_C , and K_X), which relate to the PA specifications and circuit components [7,17,23,30,31]. For instance, by fixing the specification values of P_{out} and V_{DD} , the K_P equation can be used to find the R_L value through the expression that is shown in Figure 3. Therefore, in order to find the values of the circuit model from the design specifications, the expressions between the PA design variables (e.g., ω_o , R_L , C_{SH}) that are shown in Figure 3 can be used. This design set is composed of analytical functions of the D and q variables, which are given by Equations (23)–(27) [17,19].

$$K_L = \frac{\omega_o L_{SH}}{R_L} = \frac{p(D, q)}{2g_x(D, q)} \quad (23)$$

$$K_C = \omega_o C_{SH} R_L = \frac{2g_x(D, q)}{q^2 p(D, q)} \quad (24)$$

$$K_P = \frac{P_{out} R_L}{V_{DD}^2} = 2(g_x(D, q))^2 \quad (25)$$

$$K_X = \frac{X_s}{R_L} = \frac{\frac{1}{\pi} \int_0^{\frac{2\pi}{\omega}} (V_{C_{SH}}(t) \cos(\omega t + \varphi)) dt}{\frac{1}{\pi} \int_0^{\frac{2\pi}{\omega}} (V_{C_{SH}}(t) \sin(\omega t + \varphi)) dt} \quad (26)$$

$$K_{Q_L} = Q_L = \frac{\omega_o L_o}{R_L} = \frac{1}{\omega_o C_o R_L} \quad (27)$$

where X_s is a capacitive or inductive reactance that must be added to the resonant network (i.e., L_o and C_o) to guarantee the ZVS and ZVDS operation. We add the K_{Q_L} equation into the conventional design set, because the Q_L defines the L_o and C_o values. The current gain of the PA under the small ripple approximation is given by [20]

$$g_x = \frac{\langle i_s(t) \rangle_{2\pi}}{I_p} = \left(\frac{1 - \cos(2\pi D)}{2\pi} \right) \cos(\varphi) + \left(\frac{\sin(2\pi D)}{2\pi} - D \right) \sin(\varphi) + \frac{D^2 \pi}{p} \quad (28)$$

where $\langle x \rangle_{2\pi}$ is the moving average operator over the v_g period. The moving average of i_s is given by [32]

$$\langle i_s(t) \rangle_{2\pi} = \frac{\omega_o}{2\pi} \int_0^{\frac{2\pi D}{\omega_o}} i_s(\tau) d\tau. \quad (29)$$

In the design set that is composed of (23)–(27), the designer must fix the D and q values to design the PA from its specifications. In the literature, some “optimal” design equations have been proposed under particular restrictions. Table 1 shows a summary of the selected proposals, which could be used in order to design the PA according to the application. The most common design set considers a duty cycle $D = 0.5$ because it reduces the design complexity of the oscillator that controls the switch, and $q = 1.412$ because it maximizes the load power for a fixed V_{DD} and R_L [17].

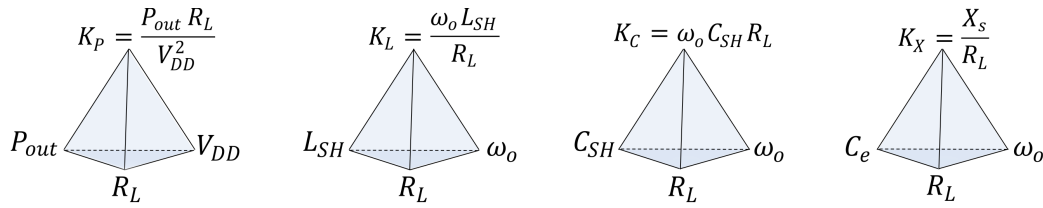


Figure 3. Design set relations.

Table 1. Design Sets of different Class-E PA models.

Parameter	Ewing [7] ^a	kazimierczuk [31]	Grebennikov [30]	Iwadare [23]	Acar [17] ^b
K_L	∞	∞	0.732	3.534	0.732
K_C	0.184	0.184	0.685	0.071	0.685
K_P	0.577	0.577	1.365	0.056	1.365
K_X	0.637	1.152	0	-4.903	0
R_{on} switch	finite	zero	zero	zero	zero
L_{SH}	infinite	infinite	finite	finite	finite
C_{SH}	linear	linear	linear	linear	linear
D	arbitrary	0.5	0.5	0.5	arbitrary

^a Calculated for $D = 0.5$ and zero on resistance. ^b Calculated for $D = 0.5$ and $q = 1.412$.

In a particular application, the PA designer can explore the design space defined by the D and q variables. On one hand, the design space of q was analyzed in [16] with a practical range between 0 and 1.9 for $D = 0.5$. On the other hand, the design space of D was studied in [33,34], with a practical range between 0.25 and 0.75. Additionally, the maximum current and voltage values supported by the PA components can be analyzed into the design process as specifications. For example, in [19], the authors included the rupture voltage of the switch in the design process using the following equation [20]

$$V_{C_{SHm}} \approx \frac{1.7613 + 0.0500q}{1 - D} V_{DD}. \quad (30)$$

As another example, in [35] the authors developed the analytical equation of the Root Mean Square (RMS) current through the switch given by

$$I_{RMS_{SW}} = \frac{V_{DD} \cdot g_x(D, q)}{R_L} \frac{f_1(D, q)}{f_2(D, q)} \quad (31)$$

where

$$f_1(D, q) = 0.4532 - 0.348q + 0.9159q^2 + 1.279D + 1.344D^2 - 0.6721qD - 1.589q^2D^2 - 0.1598q^3 + 0.7299D^3 + 1.039q^3D^3 \quad (32)$$

$$f_2(D, q) = 3.615 - 7.482q + 3.686q^2 - 7.518D + 7.672D^2 + 19.41qD - 11.87q^2D - 15.74qD^2 + 9.707q^2D^2 + 0.1672q^3 - 0.6993D^3 \quad (33)$$

2.3. Maple™ Implementation of the Analytical PA Model and Its Design Set

This section briefly describes the Maple™ code used for implementing the analytical model and the design set of the Class-E PA with FDI presented in the previous subsections. This model is composed of the Equations (4)–(9) and the variables φ , p , C_1/V_{DD} , C_2/V_{DD} , and g_x expressed as explicit functions of the q and D variables. These last functions were found through the algebraic solution of the equations proposed in [17,19], and then they were coding in the Maple™ script presented in Appendix A.1. The amplifier design set was coded based on the implemented model, the solution of the Equation (26) (coded as an intermediate function $KX2$), and the functional operator feature of Maple™. The resulting script is described in Appendix A.2. As a result of this implementation

approach, the amplifier model and its design set were coded as functions of the variables D and q . Finally, we code Equations (4)–(9) to estimate the main waveforms predicted by the model, the resulting script was summarized in Appendix A.3.

The scripts summarized in Appendix A could be used at least for two purposes. The first one is to plot the estimated waveforms under ZVS and ZVDS operation of the analytical model while using the D , L_{SH} , C_{SH} , R_L , and V_{CC} values. The second one is to calculate the design set using the q and D values.

3. Design Methodology of the Ideal Class-E PA with FDI

The design flow of the proposed methodology is shown in Figure 4. In step 1, the designer defines the input parameters, the maximum ratings, and the optimization goals. The maximum ratings can be defined based on the manufacturer's data sheets [19], the input parameters can be defined from the Class-E PA design specifications, and the optimization goals can be defined to maximize or minimize circuit variables (e.g., maximize the P_{out}). In steps 2 and 3, the designer must find the extended design set that involves the mathematical expressions for the unknown circuit values, maximum ratings, and optimization goals. In step 4, the designer must plot the search space (i.e., all possible values of the design variables subject to ZVS and ZVDS operation as a function of D and/or q) in a particular range of the D and q variables, if they are unknown. Once the designer explored the search space and found the optimum combination of D and q , the circuit components of the PA must be calculated in step 5, and the circuit operation must be verified in step 6. If all of the specifications are met, the design process is finalized. Otherwise, a new search of D or q values can be made to achieve it.

It is important to highlight that the design solution is an ideal approximation, which uses assumptions, such as ideal components. When the ZVS and ZVDS conditions are not achieved after the design implementation, either by the effect of non-ideal components or by approximation to commercial values, a tuning process can be performed. Commonly, this process fits the point of ZVS and ZVDS in order to accomplish the soft-switching operation by the tuning of the component values [21,28,29].

3.1. Design Approaches

In this subsection, we explore the design of an ideal Class-E with FDI for wireless transfer applications under two design approaches by applying the proposed methodology. These approaches are: to use an optimum value of D and q reported in the literature and to optimize the PA for minimizing the stress supported by the switch. These designs were calculated with Maple™ to simplify numerical development. These approaches were solved while using the support tools developed for this tutorial and the procedure reported in Appendix B. These tools could be used for different applications and design specifications with minor modifications. Furthermore, the validation of the design process was made by circuit simulations in OrCAD PSpice® Designer. All of the simulations employed transient analysis with a maximum time step of 1 ns, ideal components, voltage-controlled switch with zero fall and rise commutation times, off-resistance of 300 MΩ, and on-resistance of 10 mΩ.

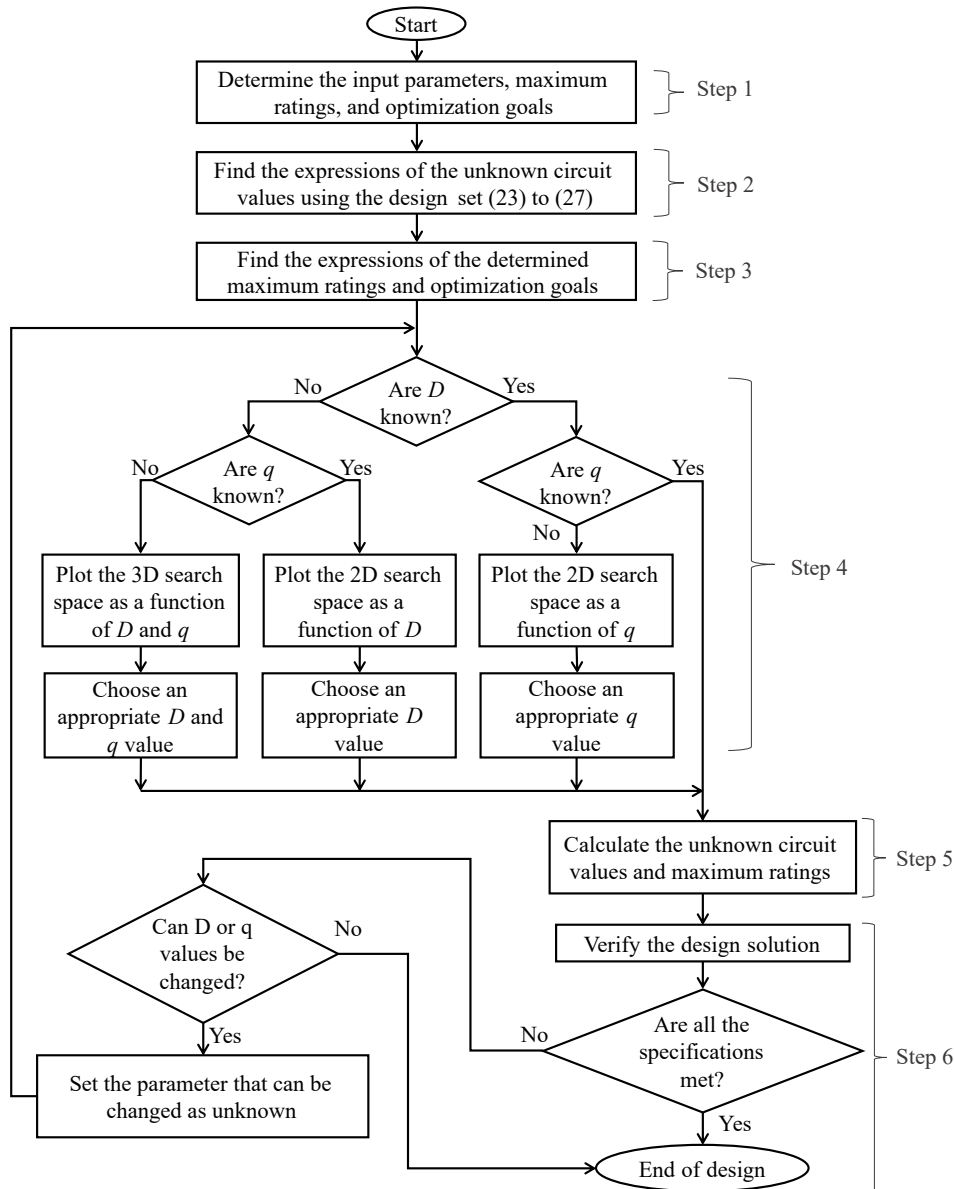


Figure 4. Proposed Design Methodology for Class-E PA.

3.1.1. Approach A: Design Based on a Reported Optimal Point

In this approach, the design specifications are based on the standard QiTM, which defines inductive charging guides for wireless power applications over short distances [36]. Following the design methodology that is proposed in Section 3, the design steps are:

Step 1: the specifications of the design were defined from the power class 0 specification of standard QiTM, which are summarized in Table 2. The L_o value corresponds to a commercial transmitter coil in compliance with the standard. The D and q values were defined in order to maximize the output power with low complexity of the switch driver [17]. Additionally, the only restriction considered was the breakdown voltage of the switch. Therefore, the v_{CSHm} value was limited to 30 V (typical maximum rating of MOSFETs for low voltage applications [37]).

Table 2. Class-E PA specifications.

f_o [kHz]	V_{DD} [V]	L_o [μ H]	P_{in} [W]	η	D	q
100	5	24	10	1	0.5	1.412

Step 2: in this design, the unknown variables are L_{SH} , C_{SH} , C_e , and R_L . The process used to find these unknown values from the design set is illustrated in Figure 5. This diagram has four phases. In phase 1 is found the equation of R_L . In phase 2, are identified the expressions for calculating C_{SH} , L_{SH} , X_s , and K_{Q_L} . Subsequently, phase 3 identifies the expression of C_o , and finally, in phase 4 is found the C_e equation. In the diagram shown in Figure 5, the input parameters or design specifications are shown in silver boxes, the relations of the design set in blue boxes, and the unknown expressions in white boxes. We followed this graphical notation in the diagrams that will appear in Section 4.

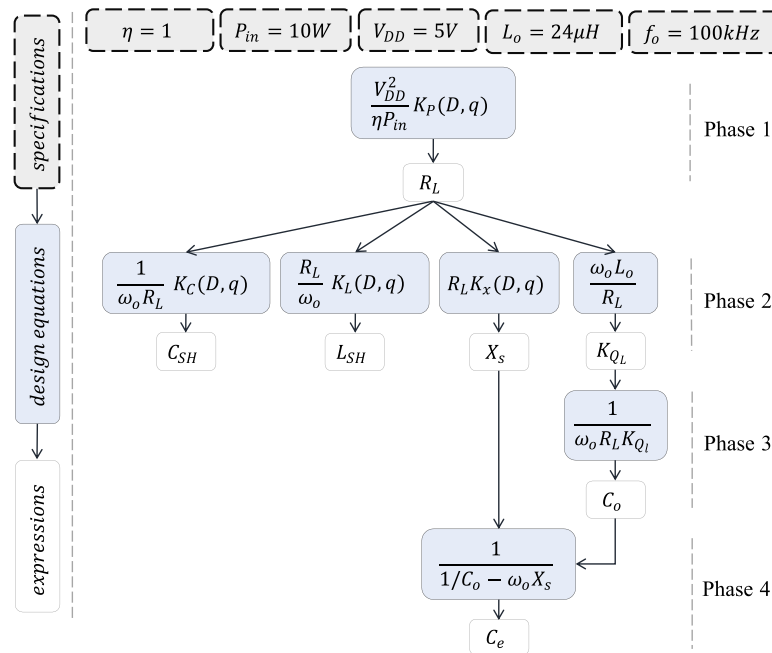


Figure 5. Phases to find the expressions of unknown circuit values.

Step 3: the design set is extended by the expression of $V_{C_{SHm}}$ described in (30).

Step 4: this step is skipped, because D and q are specifications of this design.

Step 5: the extended design set was implemented in Maple™ while using the support tools developed for this tutorial. The resulting model parameters are listed in Table 3, and the resulting circuit components and restrictions were listed in Table 4.

Table 3. Model parameter values for approach A.

Parameter	Value *	Parameter	Value *	Parameter	Value *
K_L	0.7332	K_X	−0.0002	$C1/V_{DD}$	2.6106
K_C	0.6841	φ	−2.4925	$C2/V_{DD}$	−2.1385
K_P	1.3632	p	43.8534	g_x	0.8256

* Calculated for $D = 0.5$ and $q = 1.412$.

Table 4. Circuit components and restriction values of approach A.

Variable	Design Values	Commercial Values
R_L [Ω]	3.41	3.40
L_{SH} [μH]	3.98	3.90
C_{SH} [nF]	319.48	330.00
C_e [nF]	105.54	100.00
$V_{C_{SHm}}$ [V]	18.32	NA
D	0.5	0.5
q	1.412	1.412

Step 6: in Figure 6, the theoretical (Model) and simulated (Ideal sim.) waveforms of the designed Class-E were plotted. These waveforms present ZVS and ZVDS operation under the design restriction of V_{CSHm} less than 30 V. Therefore, the simulation verifies the good performance of the designed Class-E PA.

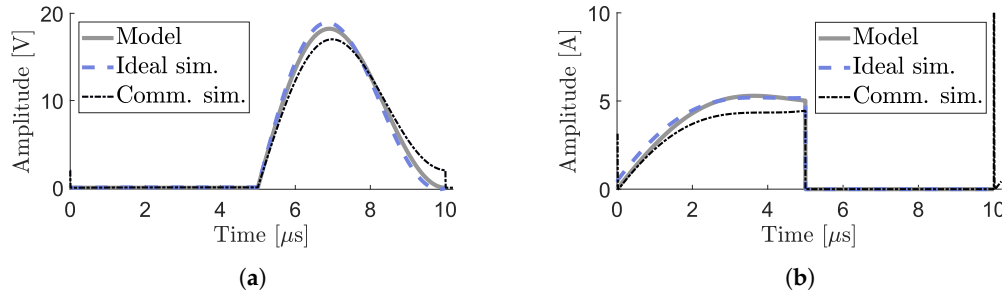


Figure 6. Waveforms of the Class-E PA designed in approach A. (a) v_{CSH} . (b) i_S .

The Class-E PA is susceptible to the component values. For instance, when the components found in the design process of the last example are approximated to the closest commercial component values, the simulated waveforms have significant changes (Comm. sim. in Figure 6). Furthermore, the ZVS and ZVDS conditions are not met and, consequently, the switch stress is increased. This electric stress could be quantified by the output power capability, which is given by [38]

$$C_p = \frac{P_{out}}{\max \{V_p, V_{pon}\} \cdot \max \{I_p, I_{pon}\}} \quad (34)$$

where I_p and V_p are the peak current and peak voltage across the switch, respectively. The I_{pon} and V_{pon} are the current and voltage values at the switch turn-on time, as shown in Figure 7.

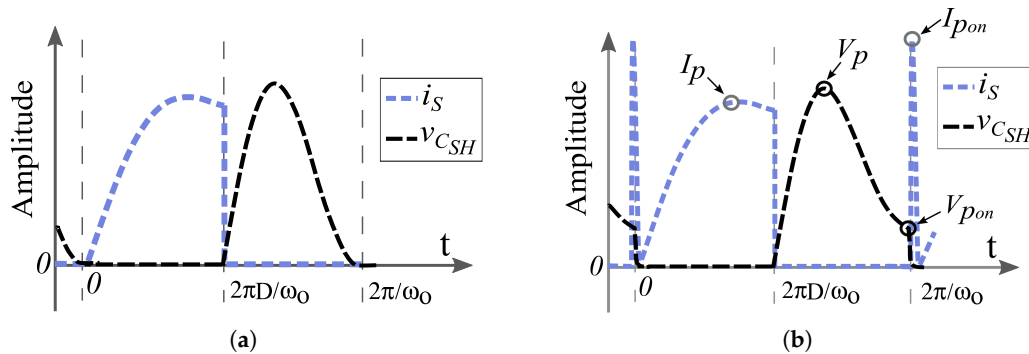


Figure 7. Switching condition waveforms. (a) PA with ZVS and ZVDS. (b) PA without ZVS and ZVDS.

3.1.2. Approach B: Design under an Optimization Goal

In this approach, the Class-E PA is designed based on the same specifications of the approach A. However, we explore the overall PA design space in order to guarantee a high C_p according to circuit values of commercial components.

Steps 1, 2, and 3: similar to the ones presented in Section 3.1.1. However, D and q are defined as design variables.

Step 4: the design search space was plotted in Figure 8. The variable D should be less than 0.625 to accomplish the design restriction (i.e., $V_{CSHm} < 30$ V), as shown in Figure 8a,b. An optimization process was developed over the search space of the components (Figures 8c–f in order to find circuit components under commercial values restriction. This process was implemented by parametric sweeps

of the D and q variables. We plot, in Figure 8g, the sweep of the optimum D , from this family of curves we found the optimum value of q as 1.821.

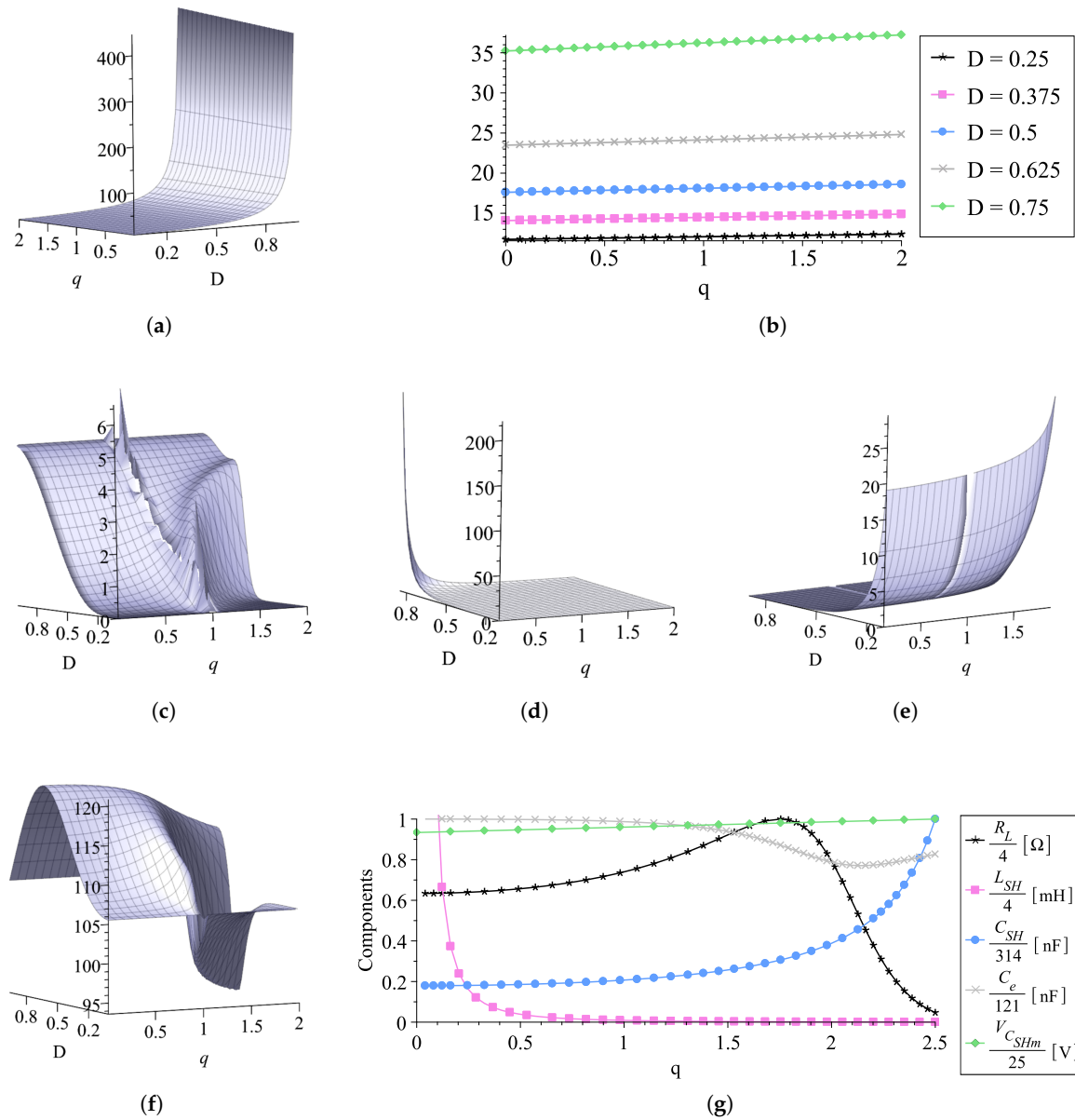


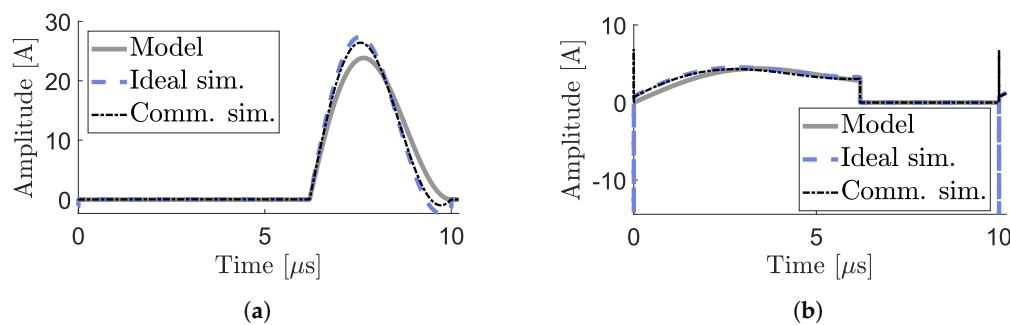
Figure 8. Design search space (a) V_{CSHm} . (b) V_{CSHm} parametric plot. (c) $R_L(D, q)$ [Ω]. (d) $L_{SH}(D, q)$ [mH]. (e) $C_{SH}(D, q)$ [μF]. (f) $C_e(D, q)$ [nF]. (g) Component values with $D = 0.62$.

Step 5: following the process that is described in Section 3.1.1, we found the circuit components and its closest commercial values, as summarized in Table 5.

Table 5. Circuit components and restriction values of approach B.

Variable	Design Values	Commercial Values
R_L [Ω]	3.95	3.90
L_{SH} [μ H]	7.51	7.50
C_{SH} [nF]	101.74	100.00
C_e [nF]	102.36	100.00
$V_{C_{SHm}}$ [V]	24.37	NA
D	0.62	0.62
q	1.821	1.821

Step 6: the design was verified by simulation, obtaining satisfactory waveforms for the approximate commercial values, as shown in Figure 9 (comm. sim.).

**Figure 9.** Waveforms of the Class-E PA designed in approach B. (a) $v_{C_{SH}}$. (b) i_S .

Finally, Table 6 presents a comparison of the simulated results by following both design approaches with commercial components. The results are related to the electrical stress of the switch. The optimization process reduces the stress of the switch, in particular, the C_p was increased by 2079% approximately.

Table 6. Simulated circuit parameters.

Parameter	Approach A	Approach B	Optimization Effect * [%]
V_p [V]	17.02	26.42	55.20
V_{pon} [V]	2.00	0.08	96.12
I_p [A]	4.45	4.30	3.37
I_{pon} [A]	189.00	6.72	96.45
P_{in} [W]	8.81	10.50	19.23
P_{out} [W]	8.68	10.43	20.18
η	0.99	0.99	0.79
C_p	0.0027	0.0588	2078.94

$$* \text{ Optimization effect} = \frac{[\text{Approach A} - \text{Approach B}]}{\text{Approach A}} \cdot 100.$$

3.2. Maple™ Implementation of Approach A and B

This section describes briefly the Maple™ script used to design the PAs with the approaches A and B of the proposed methodology. The script was divided into segments. In the first segment, the PA model variables and its design set were defined as a function of the D and q variables while using the script summarized in Appendices A.1 and A.2 (described in Section 2.3). In the next segment, the input parameters and extended design set were defined according to the results of steps 1 to 3 of the proposed methodology. Subsequently, if the variables D and/or q are unknown, then a dedicated segment plots the search space (3D or 2D), which are required in step 4 of the methodology. In the next segment,

the script calculates the circuit components from the chosen values of D and q . In the last segment, the script plots the main circuit waveforms, which are used to compare the model estimation with the simulated values. This script was summarized in Appendix B, and it could be adapted with little modifications to the specific requirements of a particular application. For instance, we use a modified script in order to develop the amplifier designs that are reported in the next section. Additionally, as a support tool, we developed a basic code to start a new design following the proposed methodology (i.e., supplementary materials BasicCode.mw file in the support tools).

4. Study Cases and Analysis Results

In order to evaluate the proposed design methodology, four study cases were selected with the initial specifications listed in Table 7. These cases show different design starting points and they involve the optimization of at least one circuit variable. In the first study case, the design goal is to find the maximum output power for a given V_{DD} and R_L . This example could be useful in wireless power transfer applications, where the power amplifier load could be fixed into the PA design as a specification for maintaining the high efficiency of the inductive link while using an adaptive impedance matching network between the output of the amplifier and link [1,19]. The second case requires the maximum load resistance while using $D = 0.5$. This design approach could be useful in VLSI applications where the MOSFET driver is integrated, since, by setting $D = 0.5$, its layout complexity is reduced and consequently the overall chip size too [16]. Furthermore, maximizing the load value decreases the power dissipation in the parasitic elements of the output load network because the current delivered to the load under the same output power is decreased [19]. The design goal of the third study case is to find the maximum C_p value for a given P_{out} , R_L , f_o , and Q_L . The C_p maximization improves the useful life of the semiconductor device and reduces the cost of the amplifier; this feature is relevant for several Class-E applications. Finally, the fourth study case looks for the higher R_L value with a limited RMS current through the switch. This design approach with a limited value of the switch RMS current could be used when the switch has size constraints, because the consumed power of the switch is directly related to this RMS value. Furthermore, the R_L maximization could be used in order to reduce the losses in the quasi-tuned LC circuit, as we discussed before. In each case, the unknown circuit values were found applying the proposed methodology by using the software Maple™, the obtained solutions are listed in Table 8. Additionally, the validation of the design solutions was made by circuit simulations in OrCAD PSpice® Designer software. In all simulations were used ideal components and a voltage-controlled switch with zero falls and rise commutation times, off-resistance of 300 MΩ, and on-resistance of 10 mΩ.

Table 7. Design specifications.

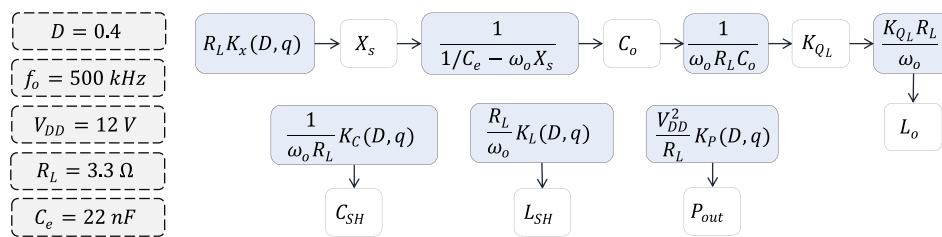
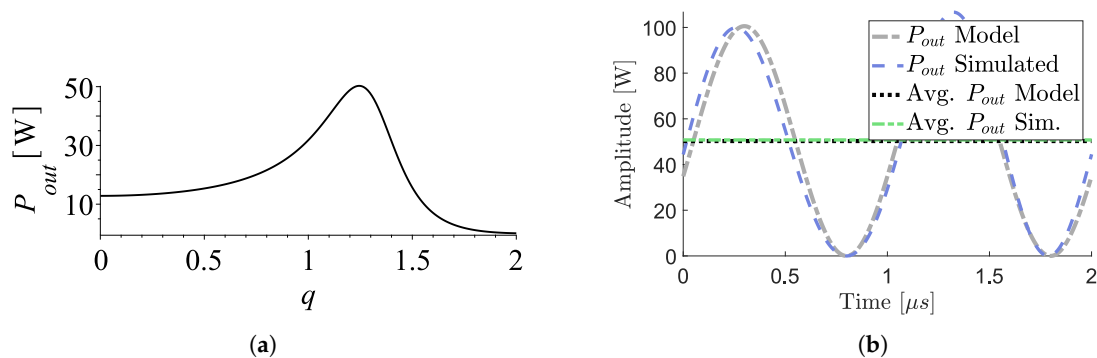
Specification	Case 1	Case 2	Case 3	Case 4
D	0.4	0.5	nv	nv
q	nv	nv	nv	nv
f_o [MHz]	0.5	1	10	4
Q_L	nv	nv	30	32
V_{DD} [V]	12	nv	nv	6
P_{in} [W]	nv	1	8	6
P_{out} [W]	nv	1	8	6
η	1	1	1	1
R_L [Ω]	3.3	nv	2.4	nv
L_o [μH]	nv	33	nv	nv
C_e [nF]	22	nv	nv	nv
C_{SH} [nF]	nv	22.6	nv	nv
maximize	P_{out}	R_L	C_p	R_L
$I_{RMS_{SW}}$	nv	nv	nv	<2A

nv: Unknown value.

Table 8. Design solutions.

Parameter	Case 1	Case 2	Case 3	Case 4
R_L [Ω]	3.30	4.94	2.40	10.90
L_{SH} [nH]	492.19	520.09	31.05	1.47
C_{SH} [nF]	133.02	22.60	2.60	172.20
L_o [μ H]	4.61	33.00	1.15	13.87
C_e [nF]	22.00	0.76	0.22	114.10
V_{DD} [V]	12.00	1.93	4.44	6.00
P_{in} [W]	50.28	1.00	8.00	6.00
P_{out} [W]	50.28	1.00	8.00	6.00
η	1	1	1	1
D	0.40	0.50	0.55	0.75
q	1.244	1.468	1.771	2.504
Q_L	4.39	41.94	30.00	32.00

In study case 1, it is required the maximum output power for a given V_{DD} and R_L , the specified duty cycle is 0.4, and the q value is undefined. The mathematical expressions of the unknown circuit values were obtained following the process that is described in the diagram of Figure 10. According to the P_{out} search space plotted in Figure 11a, the maximum output power for $D = 0.4$ is achieved at $q = 1.244$. Therefore, the unknown circuit components were calculated and listed in Table 8 using $q = 1.244$. Finally, the design solution was verified by simulation. The simulated P_{out} was 50.82 W, and the waveforms of the output power and average output power are shown in Figure 11b.

**Figure 10.** The process to find the unknown design values of study case 1.**Figure 11.** Class-E PA waveforms of study case 1. (a) P_{out} search space for $D = 0.4$. (b) Model and simulated waveforms of the P_{out} and average P_{out} .

In the second design, the maximum R_L is found for a given f_o and C_{SH} , the specified duty cycle is 0.5 and the q value is undefined. The expressions of unknown circuit components were obtained with the process that is shown in Figure 12. According to the R_L search space plotted in Figure 13a, the maximum load resistance for $D = 0.5$ is achieved at $q = 1.468$. Hence, the circuit parameters were calculated and summarized in Table 8 using $q = 1.468$. Finally, the design solution was verified, the switch voltage and current obtained in the simulation are shown in Figure 13b, where a soft-switching behavior is observed.

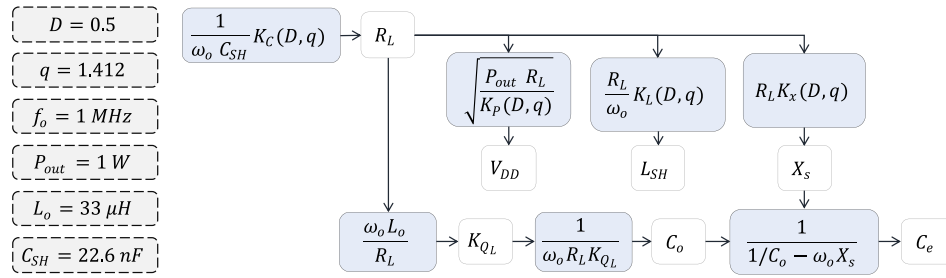


Figure 12. The process to find the unknown design values of study case 2.

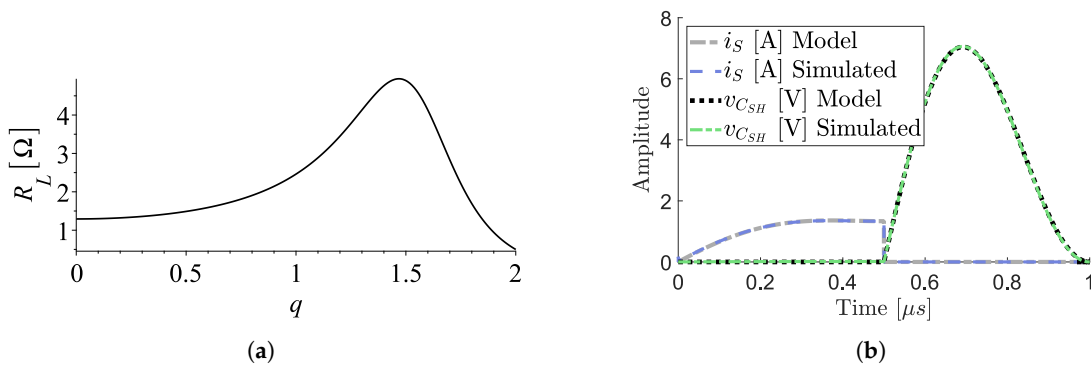


Figure 13. Class-E PA waveforms of study case 2. (a) R_L search space for $D = 0.5$. (b) Model and simulated waveforms of the switch current and voltage.

In the study case 3, the maximum output power capability is found for a given P_{out} , f_o , R_L , where Q_L , the D and q values are undefined. The unknown circuit expressions were obtained following the process described in Figure 14. The C_p variable search space is shown in Figure 15a, the curve behavior shows that the maximum C_p is around $D = 0.5$, and it decreases at extreme D values (i.e., $D = 0.25$ and $D = 0.75$). The maximum C_p is achieved at $D = 0.55$, for $q = 1.771$, as shown in Figure 15b. Therefore, the unknown parameters were calculated and are listed in Table 8 using these values. Finally, the design solution was verified. The simulated C_p was 0.1071, the waveforms of the switch current and output power are shown in Figure 15c.

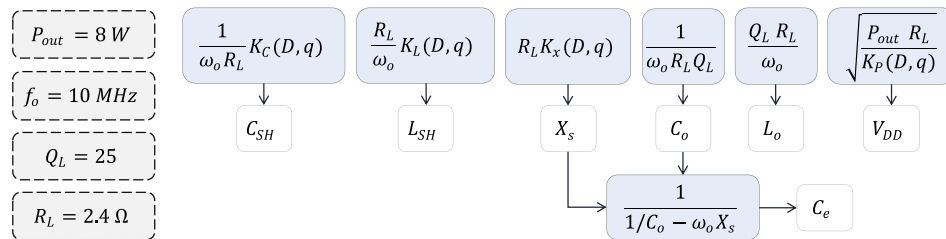


Figure 14. The process to find the unknown design values of study case 3.

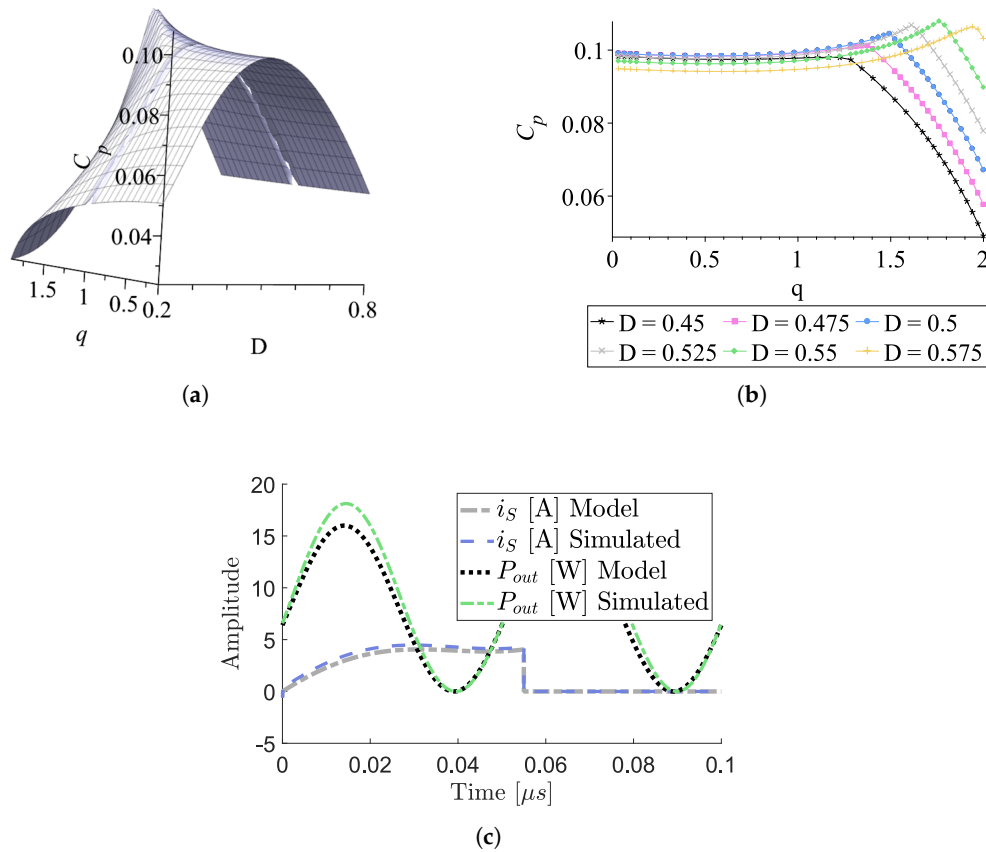


Figure 15. Class-E PA waveforms of study case 3. (a) C_p surface. (b) C_p for $D = 0.45, 0.47, 0.5, 0.53, 0.55$, and 0.57 . (c) Model and simulated waveforms of the switch current and P_{out} .

In the study case 4, the maximum R_L value is found with the $I_{RMS_{SW}}$ being limited to 2 A, the D and q values are undefined. The expressions for the unknown circuit components were obtained with the process shown in Figure 16. The search space of R_L and $I_{RMS_{SW}}$ are plotted as a function of D and q in Figure 17a,b, respectively. The analytical expression of $I_{RMS_{SW}}$ is taken from the Equation (31). The curve behavior of Figure 17a shows that the R_L value increases as D increases. Similarly, the curve behavior of Figure 17b shows that the $I_{RMS_{SW}}$ decreases as D increases. Consequently, the duty cycle is set at 0.75, because it allows a high R_L value and restricts the RMS switch current under 2 A. According to Figure 17a, the maximum load resistance for $D = 0.75$ is achieved at $q = 2.504$. Therefore, the unknown parameters were calculated and are summarized in Table 8 while using $D = 0.75$ and $q = 2.504$. Finally, the design solution was verified by simulation, where the simulated switch RMS current was 1.39 A. The waveforms of the switch current and $I_{RMS_{SW}}$ are shown in Figure 17c. With D values different than 0.5, the q range to obtain the optimal solution can be greater than 1.9, as shown in Figure 17a.

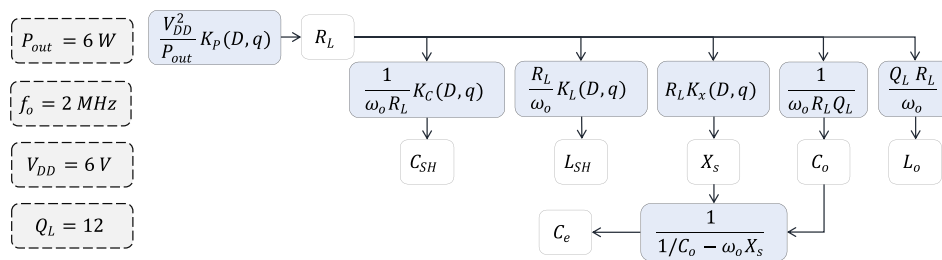


Figure 16. The process to find the unknown design values of study case 4.

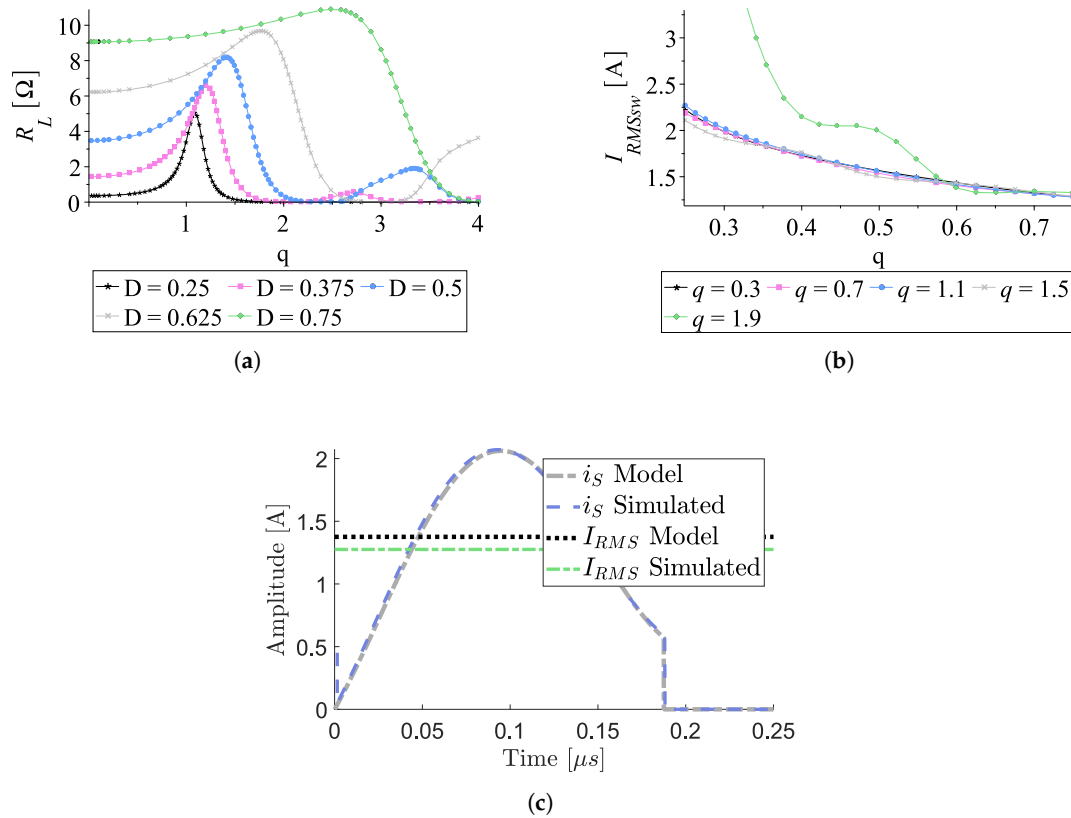


Figure 17. Class-E PA waveforms of study case 4. (a) R_L for $D = 0.25, 0.325, 0.5, 0.625$, and 0.75 . (b) I_{RMSsw} for $q = 0.3, 0.7, 1.1, 1.5$, and 1.9 . (c) Model and simulated waveforms of the switch current and average i_s .

The optimization goals and maximum ratings were verified in the simulation for each example, the obtained simulated results were summarized and confronted with the predicted values in Table 9. The simulated efficiency in all cases was 0.99. The study cases 1 and 2 show a good performance, ZVS and ZVDS conditions are achieved, and the Absolute Percentage Error (APE) is less than 2.14% in the simulated parameters. In the third design, the predicted and simulated C_p value has an absolute percentage error of 1.06%. The study case 4 accomplish an R_L value 33% greater than the obtained with the typical operation point (the load resistance calculated with $D = 0.5$ and $q = 1.412$ is 8.18Ω for the same specifications). Additionally, the I_{RMSsw} restriction is achieved and it has an APE of 1.16%. The Mean Absolute Percentage Error (MAPE) of the analyzed parameters is 3.01%, which verifies the adequate design procedure.

Table 9. Design results.

Study case	Parameter	Model	Simulated	APE *
1	P_{in} [W]	50.28	51.36	2.14
	P_{out} [W]	50.28	50.82	1.08
	η	1.00	0.99	1.04
2	P_{in} [W]	1.00	1.00	0.13
	P_{out} [W]	1.00	0.99	0.78
	η	1.00	0.99	0.65
3	P_{in} [W]	8.00	8.95	11.89
	P_{out} [W]	8.00	8.87	10.83
	η	1.00	0.99	0.95
	C_p	0.1082	0.10705	1.06
4	P_{in} [W]	6.00	6.31	5.20
	P_{out} [W]	6.00	6.28	4.69
	η	1.00	1.00	0.49
	$I_{RMS_{SW}}$ [A]	1.38	1.39	1.16

$$* \text{ APE} = \frac{|\text{Model} - \text{Simulated}|}{\text{Model}} \cdot 100.$$

5. Conclusions

This paper presents a design methodology of the ideal Class-E PA with FDI, which explores the PA circuit components freedom easily by use of the mathematical software Maple™. The presented examples show the impact of the proposed methodology in PA optimization. Furthermore, a presentation and Maple™ codes were developed as support tools for this methodology proposal. We hope that this document and the support materials motivate engineers to integrate this amplifier into their projects.

6. Future Work

This paper presents the results of the first milestones reached under the framework of the research project entitled “Class E Amplifier with Gallium Nitride Transistors for Wireless Power Transfer Applications”, which aims to respond to the following research question: how to design a class E PA using transistors made of Gallium Nitride (GAN), ensuring high efficiency when the load is a standard inductive link for charging mobile phones? In future work, we will expand the proposed methodology with more analytical expressions that are related to the maximum rating constraints of the amplifier components, such as the RMS value of the feed inductance current. Furthermore, we will explore a specific tuning process to guarantee ZVS and ZVDS operation of the amplifier when its load is an inductive link and its switch is implemented by a CMOS or a GAN device.

Supplementary Materials: The following are available online at <http://www.mdpi.com/2076-3417/10/24/8765/s1>, readme.txt: General instructions of the support tools, ApproachA.mw: Code of “Approach A” developed in the tutorial, ApproachB.mw: Code of “Approach B” developed in the tutorial, BasicCode.mw: Template with the basic steps to develop a new design of the Class-E amplifier with FDI, TutorialMaple.pptx: Presentation of the model equations and the step by step to develop a Class-E PA design with MAPLE™.

Author Contributions: Conceptualization, all authors; methodology, all authors; supervision, A.F.; writing, original draft preparation, all authors; writing–review and editing, all authors; visualization, I.C. and A.F. All authors read and agreed to this version of the manuscript.

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electromagnetic interference source under soft and forced switching operation ". They are identified with IDs 20066 and 09376, respectively. Moreover, the authors would like to thank Professor Fernando Rangel de Sousa from the Universidade Federal de Santa Catarina in Florianapolis (Brazil), for the fruitful discussions during the design methodology conception.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

PA	Power Amplifier
RF	Radio-Frequency
ZVS	Zero Voltage Switching
ZVDS	Zero Voltage Derivative Switching
FDI	Finite DC-Feed Inductance
DC	Direct current

Appendix A. Analytical Model of Class-E PA with FDI Implemented in Maple™

This appendix summarizes the Maple™ implementation of the analytical model of Class-E PA with FDI used in this paper. The reported scripts are available in the support tools developed for this tutorial. The reported scripts were developed in Maple™ 2020 Academic Edition and running in a Windows 10 (64-bit) system, CPU @ 2.30 GHz, and 4.00 GB RAM. Furthermore, they can be copied and pasted directly into the Maple™ document.

Appendix A.1. Explicit Functions of the Variables the φ , p , C_1/V_{DD} , C_2/V_{DD} , and g_x Developed in Maple™

Appendix A.1.1. φ Definition

[illegible]

Appendix A.1.2. p Definition

[illegible]

Appendix A.1.3. C_1/V_{DD} Definition

[illegible]

[illegible]

Appendix A.1.4. C_2/V_{DD} Definition

[illegible]

Appendix A.1.5. g_x Definition

$$\begin{aligned} \text{I0_IP} &:= (D, q, p, \varphi) \rightarrow D \sin(\varphi) + \sin(\varphi) \sin(Pi^*D) \cos(Pi^*D) / Pi - \cos(\varphi) \cos(Pi^*D)^2 / Pi + Pi^*D^2 / p + \cos(\varphi) / Pi; \\ \text{gx} &:= (D, q) \rightarrow \text{I0_IP}(D, q, p(D, q), \Phi(D, q)); \end{aligned}$$

Appendix A.1.6.

If This Code was Copy and Pasted in Maple™ Verify the Following Values:

$Dp := 0.5 ;$	
$qp := 1.412 ;$	
$evalf(\text{Phi}(Dp, qp)) ;$	0.2639596328
$evalf(p(Dp, qp)) ;$	1.210593000
$evalf(C1_VDD(Dp, qp)) ;$	2.610615843
$evalf(C2_VDD(Dp, qp)) ;$	-2.138459018
$evalf(gx(Dp, qp)) ;$	0.8256039532

Figure A1. Values of the defined variables for $D = 0.5$ and $q = 1.412$.

Appendix A.2. Design Set Gains K_L , K_C , K_P , and K_X Developed in Maple™

Appendix A.2.1. Definition of the Design Set Gains

$KX2 := (D, q, p, \varphi, C1_VDD, C2_VDD) \rightarrow (-C2_VDD^2 q^2 \cos(\varphi) \cos(Pi^2 q)^2 - C2_VDD^2 \sin(\varphi) \sin(Pi^2 q) \cos(Pi^2 q) + 2^*C1_VDD^2 q^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \sin(\varphi) \cos(D^2 Pi) - C1_VDD^2 \cos(D^2 Pi^2 q)^2 \sin(\varphi) \cos(D^2 Pi)^2 - C1_VDD^2 \sin(\varphi) \cos(D^2 Pi)^2 + C2_VDD^2 q^2 \cos(\varphi) \cos(Pi^2 q)^2 + 1/2^*Pi^2 p^2 q^2 - C1_VDD^2 \sin(\varphi) \cos(Pi^2 q)^2 + \cos(\varphi) \sin(D^2 Pi) \cos(D^2 Pi) + C1_VDD^2 \sin(\varphi) + q^2 \sin(\varphi) + \sin(\varphi) \cos(D^2 Pi)^2 + 2^*C2_VDD^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \cos(\varphi) \cos(D^2 Pi) - 2^*C1_VDD^2 q^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \cos(\varphi) \cos(D^2 Pi)^2 - 2^*C2_VDD^2 q^2 \cos(D^2 Pi^2 q)^2 \sin(\varphi) \cos(D^2 Pi) - q^2 \cos(\varphi) \sin(D^2 Pi) \cos(D^2 Pi) + 2^*C1_VDD^2 \cos(D^2 Pi^2 q)^2 \sin(\varphi) \cos(D^2 Pi)^2 - C1_VDD^2 \cos(\varphi) \sin(D^2 Pi) \cos(D^2 Pi) - C2_VDD^2 q^2 \cos(D^2 Pi^2 q)^2 \cos(\varphi) \cos(D^2 Pi) - C2_VDD^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \sin(\varphi) \cos(D^2 Pi)^2 - 1/2^*D^2 Pi^2 p^2 q^2 - 2^*p^2 q^2 \cos(D^2 Pi)^4 \sin(\varphi) \cos(\varphi) + 2^*p^2 q^2 \cos(D^2 Pi)^2 \sin(\varphi) \cos(\varphi) + 2^*C2_VDD^2 q^2 \cos(D^2 Pi^2 q)^2 \cos(\varphi) \cos(D^2 Pi)^2 + C2_VDD^2 q^2 \sin(\varphi) \sin(D^2 Pi) \cos(D^2 Pi) + 2^*C1_VDD^2 \cos(D^2 Pi^2 q)^2 \cos(\varphi) \sin(D^2 Pi) \cos(D^2 Pi) + 2^*C2_VDD^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \sin(\varphi) \cos(D^2 Pi)^2 - 2^*p^2 q^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \sin(\varphi) \cos(D^2 Pi)^2 + C1_VDD^2 q^2 \cos(\varphi) \cos(Pi^2 q) + C1_VDD^2 q^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \cos(\varphi) + p^2 q^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \cos(\varphi) \cos(D^2 Pi)^2 - \sin(\varphi) \cos(Pi^2 q) - 1/(q^2 + 1/(q^2 - 1/(C1_VDD^2 \cos(D^2 Pi^2 q)^2 \cos(\varphi) + 2^*C1_VDD^2 q^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \sin(\varphi) \cos(D^2 Pi)^2 - 2^*C2_VDD^2 q^2 \cos(D^2 Pi^2 q)^2 \sin(\varphi) \cos(D^2 Pi)^2 + C2_VDD^2 q^2 \cos(\varphi) \sin(D^2 Pi) \cos(D^2 Pi) - C1_VDD^2 q^2 \sin(\varphi) \cos(D^2 Pi)^2 - q^2 \cos(\varphi) \sin(D^2 Pi) \cos(D^2 Pi) - C1_VDD^2 \cos(\varphi) \cos(D^2 Pi)^2 - \sin(\varphi) \sin(D^2 Pi) \cos(D^2 Pi) - C1_VDD^2 \cos(\varphi) \cos(Pi^2 q)^2 - 2^*C2_VDD^2 q^2 \cos(D^2 Pi^2 q)^2 \cos(\varphi) \cos(D^2 Pi)^2 - C1_VDD^2 \cos(\varphi) \cos(D^2 Pi)^2 - \sin(\varphi) \sin(D^2 Pi) \cos(D^2 Pi) + 2^*p^2 q^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \sin(\varphi) \cos(D^2 Pi)^2 - C2_VDD^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \cos(\varphi) \cos(D^2 Pi)^2 + 2^*p^2 q^2 \cos(D^2 Pi)^4 \cos(\varphi) \cos(\varphi) + 2^*p^2 q^2 \cos(D^2 Pi)^2 \cos(\varphi) \cos(\varphi) + C2_VDD^2 q^2 \sin(D^2 Pi^2 q) \cos(D^2 Pi^2 q) \sin(\varphi) \cos(D^2 Pi) - \cos(\varphi) + q^2 \sin(\varphi) \sin(D^2 Pi) \cos(D^2 Pi) + 2^*C1_VDD^2 \cos(D^2 Pi^2 q)^2 \cos(\varphi) \cos(D^2 Pi)^2 - C2_VDD^2 q^2 \sin(\varphi) \cos(Pi^2 q) \cos(Pi^2 q))$
 $KX := (D, q) \rightarrow KX2(D, q, p(D, q), \Phi(D, q), C1_VDD(D, q), C2_VDD(D, q))$
 $KL := (D, q) \rightarrow 1/2^*p(D, q)/gx(D, q)$
 $KC := (D, q) \rightarrow 2^*gx(D, q)/(q^2 p(D, q))$
 $KP := (D, q) \rightarrow 2^*gx(D, q)^2$

Appendix A.2.2.

If This Code was Copy and Pasted in Maple™ Verify the Following Values:

```

Dp := 0.5 :
qp := 1.412 :
evalf(KX(Dp, qp));
                                -0.00017163
evalf(KL(Dp, qp));
                                0.7331560100
evalf(KC(Dp, qp));
                                0.6841230254
evalf(KP(Dp, qp));
                                1.363243775

```

Figure A2. Values of the design set gains for $D = 0.5$ and $q = 1.412$.

Appendix A.3. Waveforms of the Analytical Model with Maple™

Appendix A.3.1.

The Following Parameters Must be Defined to Use the Next Functions:

```

Dsp := "Duty cycle value";
fsp := "operation frequency in Hzh";
VDD := "VDD value";
Lsh := "Lsh value";
Csh := "Csh value";
RL := "RL value";
qsp := 1/(2^*Pi^2*fsp^2*(Lsh^2*Csh));

```

Appendix A.3.2. v_g Plot

```

vg := t -> piecewise(t <= Dsp*aux, 1, Dsp*aux < t, 0);
aux := 1/fsp; axeX := 0 .. 1*aux; Tit := typeset("Switch driver waveform"); Labx := "Time [s]"; Laby := "Amplitude [V]"; sSize := 12; dfont := "Times"; titSize := 15; axeSize := 15;
plot(vg(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);

```

Appendix A.3.3. $v_{C_{SH}}$ Plot

```

vCsh := t -> piecewise(x <= Dsp*aux, 0, Dsp*aux < x, VDD*(1 + C1_VDD(Dsp, qsp)*cos(2^*Pi*fsp*qsp*t) + C2_VDD(Dsp, qsp)*sin(2^*Pi*fsp*qsp*t) - qsp^2*p(Dsp, qsp)*cos(2^*Pi*fsp*t + Phi(Dsp, qsp)))/(-qsp^2 + 1));
aux := 1/fsp; axeX := 0 .. 1*aux; Tit := typeset("Switch voltage waveform"); Labx := "Time [s]"; Laby := "Amplitude [V]"; sSize := 10; dfont := "Times"; titSize := 15; axeSize := 15;
plot(vCsh(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);

```

Appendix A.3.4. i_s Plot

```

Is := t -> piecewise(x <= Dsp*aux, VDD*t/Lsh - 2^*gx(Dsp, qsp)*VDD*sin(Phi(Dsp, qsp))/RL + 2^*gx(Dsp, qsp)*VDD*sin(2^*Pi*fsp*t + Phi(Dsp, qsp))/RL, Dsp*aux < x, 0);
aux := 1/fsp; axeX := 0 .. 1*aux; Tit := typeset("Switch current waveform"); Labx := "Time [s]"; Laby := "Amplitude [A]"; sSize := 10; dfont := "Times"; titSize := 15; axeSize := 15;
plot(Is(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);

```

Appendix A.3.5. $i_{C_{SH}}$ Plot

```
iCsh := t->piecewise(x <= Dsp*aux, 0, Dsp*aux < x, VDD*t/Lsh - int(vCsh(tt), tt = Dsp/fsp .. t)/Lsh + 2*gx(Dsp, qsp)*VDD*(sin(2*Pi*fsp*t + Phi(Dsp, qsp)) - sin(Phi(Dsp, qsp)))/RL);
aux = 1/fsp; axeX := 0 .. 1*aux; Tit := typeset(C[SH]*current*waveform); Labx := "Time [s]"; Laby := "Amplitude [A]"; sSize := 12; dfont := "Times"; titSize := 15; axeSize := 15;
plot(iCsh(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6,
size = [0.5, 0.5]);
```

Appendix A.3.6. $i_{L_{SH}}$ Plot

```
iLsh := t->piecewise(x <= Dsp*aux, VDD*t/Lsh - 2*gx(Dsp, qsp)*VDD*sin(Phi(Dsp, qsp))/RL, Dsp*aux < x, VDD*t/Lsh - 2*gx(Dsp, qsp)*VDD*sin(Phi(Dsp, qsp))/RL - int(vCsh(tt), tt = Dsp/fsp .. t)/Lsh);
aux = 1/fsp; axeX := 0 .. 1*aux; Tit := typeset(L[SH]*Current*waveform); Labx := "Time [s]"; Laby := "Amplitude [A]"; sSize := 12; dfont := "Times"; titSize := 15; axeSize := 15;
plot(iLsh(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6,
size = [0.5, 0.5]);
```

Appendix A.3.7. i_{R_L} Plot

```
iRL := t->2*gx(Dsp, qsp)*VDD*sin(2*Pi*fsp*t + Phi(Dsp, qsp))/RL;
aux = 1/fsp; axeX := 0 .. 1*aux; Tit := typeset(R[L]*Current*waveform); Labx := "Time [s]"; Laby := "Amplitude [A]"; sSize := 12; dfont := "Times"; titSize := 15; axeSize := 15;
plot(iRL(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6,
size = [0.5, 0.5]);
```

Appendix B. Maple™ Implementation of the Proposed Methodology Following the Approaches A and B

This appendix summarizes the Maple™ script developed to assist the amplifier design methodology proposed in this paper. The reported scripts are available in the support tools developed for this tutorial.

The reported scripts were developed in Maple 2020 Academic Edition and running in a Windows 10 (64-bit) system, CPU @ 2.30 GHz, and 4.00 GB RAM. Furthermore, they can be copied and pasted directly into the Maple™ document. Additionally, as one support tool, we developed a basic code to start a new design following the methodology proposed in this paper (BasicCode.mw in supplementary materials).

Appendix B.1. Maple™ Process of Approach A

Appendix B.1.1. Define the Input Parameters and the Extended Design Set

Input Parameters

```
fsp := 100000.;
&omega;sp := evalf(2*Pi*fsp);
VDDsp := 5;
Losp := 0.000024;
Pinsp := 10;
effsp := 1;
Dsp:=0.5;
qsp:=1.412;
```

Extended Design Set

```
RL := (D, q) -> KP(D, q)*VDDsp^2/(Pinsp*effsp);
Lsh := (D, q) -> KL(D, q)*RL(D, q)/&omega;sp;
Csh := (D, q) -> KC(D, q)/(&omega;sp*RL(D, q));
KQL := (D, q) -> &omega;sp*Losp/RL(D, q);
Xs := (D, q) -> RL(D, q)*KX(D, q);
Co := (D, q) -> 1/(&omega;sp*RL(D, q)*KQL(D, q));
Ce := (D, q) -> 1/(1/Co(D, q) - &omega;sp*Xs(D, q));
VCshm := (D, q) -> VDDsp*(1.7613 + 0.0500*q)/(1 - D);
```

Appendix B.1.2. Plot the Search Space (Only for D and/or q Unknown)

This step is skipped because D and q are known values.

Appendix B.1.3. Calculate the Circuit Values

Circuit Values

```
evalf(RL(Dsp, qsp));
evalf(Lsh(Dsp, qsp));
evalf(Csh(Dsp, qsp));
evalf(Ce(Dsp, qsp));
evalf(VCshm(Dsp, qsp));
```


Verify the Following Values:

$evalf(RL(Dsp, qsp));$	3.41
$evalf(Lsh(Dsp, qsp));$	3.98×10^{-6}
$evalf(Csh(Dsp, qsp));$	319.48×10^{-9}
$evalf(Ce(Dsp, qsp));$	105.54×10^{-9}
$evalf(VCshm(Dsp, qsp));$	18.32

Figure A3. Component values of approach A.

Appendix B.1.4. Plot the Circuit Waveforms

v_g Plot

vg := t->piecewise(t <= Dsp*aux, 1, Dsp*aux < t, 0);
aux := 1/fsp; axeX := 0 .. 1*aux; Tit := typeset(Switch*driver*waveform); Labx := "Time [s]"; Laby := "Amplitude [V]"; sSize := 12; dfont := "Times"; titSize := 15; axeSize := 15;
plot(vg(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);

$v_{C_{SH}}$ Plot

vCsh := t->piecewise(x <= Dsp*aux, 0, Dsp*aux < x, VDDsp*(1 + C1_VDD(Dsp, qsp)*cos(ωsp*qsp*t) + C2_VDD(Dsp, qsp)*sin(ωsp*qsp*t) - qsp^2*p(Dsp, qsp)*cos(ωsp*t + Phi(Dsp, qsp)))/(-qsp^2 + 1));
aux := 1/fsp; axeX := 0 .. 1*aux; Tit := typeset(Switch*voltage*waveform); Labx := "Time [s]"; Laby := "Amplitude [V]"; sSize := 10; dfont := "Times"; titSize := 15; axeSize := 15;
plot(vCsh(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);

i_s Plot

Ip := (D, q) -> 2*gx(D, q)*VDDsp/RL(D, q);
Is := t->piecewise(x <= Dsp*aux, VDDsp*t/Lsh(Dsp, qsp) - Ip(Dsp, qsp)*sin(Phi(Dsp, qsp)) + Ip(Dsp, qsp)*sin(ωsp*t + Phi(Dsp, qsp)), Dsp*aux < x, 0);
aux := 1/fsp; axeX := 0 .. 1*aux; Tit := typeset(Switch*current*waveform); Labx := "Time [s]"; Laby := "Amplitude [A]"; sSize := 10; dfont := "Times"; titSize := 15; axeSize := 15;
plot(Is(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);

$i_{C_{SH}}$ Plot

iCsh := t->piecewise(x <= Dsp*aux, 0, Dsp*aux < x, VDDsp*t/Lsh(Dsp, qsp) - int(vCsh(tt), tt = Dsp/fsp .. t)/Lsh(Dsp, qsp) + Ip(Dsp, qsp)*(sin(ωsp*t + Phi(Dsp, qsp)) - sin(Phi(Dsp, qsp))));
aux := 1/fsp; axeX := 0 .. 1*aux; Tit := typeset(C[SH]*current*waveform); Labx := "Time [s]"; Laby := "Amplitude [A]"; sSize := 12; dfont := "Times"; titSize := 15; axeSize := 15;
plot(iCsh(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);

$i_{L_{SH}}$ Plot

iLsh := t->piecewise(x <= Dsp*aux, VDDsp*t/Lsh(Dsp, qsp) - Ip(Dsp, qsp)*sin(Phi(Dsp, qsp)), Dsp*aux < x, VDDsp*t/Lsh(Dsp, qsp) - Ip(Dsp, qsp)*sin(Phi(Dsp, qsp)) - int(vCsh(tt), tt = Dsp/fsp .. t)/Lsh(Dsp, qsp));
aux := 1/fsp; axeX := 0 .. 1*aux; Tit := typeset(L[SH]*Current*waveform); Labx := "Time [s]"; Laby := "Amplitude [A]"; sSize := 12; dfont := "Times"; titSize := 15; axeSize := 15;
plot(iLsh(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);

i_{R_L} Plot

iRL := t->Ip(Dsp, qsp)*sin(ωsp*t + Phi(Dsp, qsp));
aux := 1/fsp; axeX := 0 .. 1*aux; Tit := typeset(R[L]*Current*waveform); Labx := "Time [s]"; Laby := "Amplitude [A]"; sSize := 12; dfont := "Times"; titSize := 15; axeSize := 15;
plot(iRL(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);

If the Maple™ Process is Well Developed, the Waveforms of the Circuit will be as Follows:

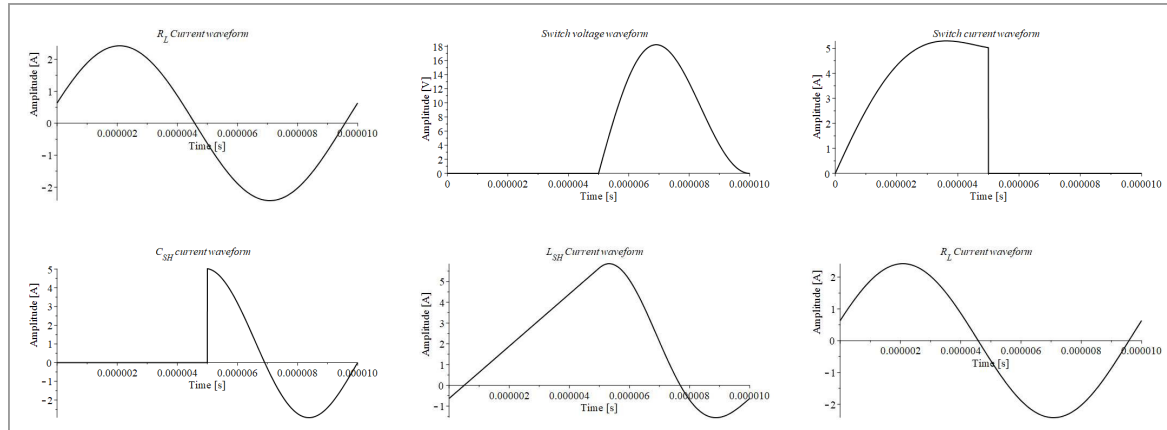


Figure A4. Model circuit waveforms of approach A.

Appendix B.2. Maple™ Process of Approach B

Appendix B.2.1. Define the Input Parameters and the Extended Design Set

Input Parameters

```
fsp := 100000.;
'omega.sp := evalf(2*Pi*fsp);
VDDsp := 5;
Losp := 0.000024;
Pinsp := 10;
effsp := 1;
```

Extended Design Set

```
RL := (D, q) -> KP(D, q)*VDDsp^2/(Pinsp*effsp);
Lsh := (D, q) -> KL(D, q)*RL(D, q)/omega.sp;
Csh := (D, q) -> KC(D, q)/(omega.sp*RL(D, q));
KQL := (D, q) -> omega.sp*Losp/RL(D, q);
Xs := (D, q) -> RL(D, q)*KX(D, q);
Co := (D, q) -> 1/(omega.sp*RL(D, q)*KQL(D, q));
Ce := (D, q) -> 1/(Co(D, q) - omega.sp*Xs(D, q));
VCshm := (D, q) -> VDDsp*(1.7613 + 0.0500*q)/(1 - D);
```

Appendix B.2.2. Plot the Search Space (Only for D and/or q Unknown)

3D R_L Plot

```
plot3d(RL(Dv, qv), qv = 0 .. 2, Dv = 0 .. 0.99, tickmarks = [[0.5, 1.0, 1.5, 2], [0.2, 0.5, 0.8], default], labels = [q, D, R_L*[Omega]], labeldirections = ["horizontal", "horizontal", "vertical"], axes = normal, color = gray, font = [axes, "TIMES", 28]);
```

3D L_{SH} Plot

```
plot3d(Lsh(Dv, qv)*10^3, qv = 0.1 .. 2, Dv = 0.1 .. 0.85, tickmarks = [[0.5, 1, 1.5, 2], [0.2, 0.5, 0.8], default], labels = [q, D, L_SH*[mH]], labeldirections = ["horizontal", "horizontal", "vertical"], axes = normal, color = gray, font = [axes, "TIMES", 28]);
```

3D C_{SH} Plot

```
plot3d(Csh(Dv, qv)*10^6, qv = 0.1 .. 1.9, Dv = 0.1 .. 0.9, tickmarks = [[0.5, 1, 1.5, 2], [0.2, 0.5, 0.8], default], labels = [q, D, C_SH*[muF]], labeldirections = ["horizontal", "horizontal", "vertical"], axes = normal, color = gray, font = [axes, "TIMES", 28]);
```

3D C_e Plot

```
plot3d(Ce(Dv, qv)*10^9, qv = 0.01 .. 2, Dv = 0.01 .. 0.96, tickmarks = [[0.5, 1, 1.5, 2], [0.2, 0.5, 0.8], default], labels = [q, D, Ce*[nF]], labeldirections = ["horizontal", "horizontal", "vertical"], axes = normal, color = gray, font = [axes, "TIMES", 28]);
```

3D $V_{C_{SHm}}$ Plot

```
plot3d(VCshm(Dv, qv), Dv = 0 .. 1, qv = 0 .. 2, tickmarks = [[0.2, 0.5, 0.8], [0.5, 1, 1.5, 2], default], labels = [D, q, V_C_SHm*[V]], labeldirections = ["horizontal", "horizontal", "vertical"], axes = normal, color = gray, font = [axes, "TIMES", 28]);
```

$V_{C_{SHm}}$ Parametric Plot

```
F1 := VCshm(0.25, x): L1 := typeset(D = 0.25): S1 := asterisk: C1 := black:
F2 := VCshm(0.375, x): L2 := typeset(D = 0.375): S2 := solidbox: C2 := gray:
F3 := VCshm(0.5, x): L3 := typeset(D = 0.5): S3 := solidcircle: C3 := black:
F4 := VCshm(0.625, x): L4 := typeset(D = 0.625): S4 := diagonalcross: C4 := gray:
F5 := VCshm(0.75, x): L5 := typeset(D = 0.75): S5 := soliddiamond: C5 := black:
Labx := "q": Laby := V_C_SHm*[V]: axeX := 0 .. 2: res := 30: sSize := 12: dfont := "TIMES": axeSize := 28:
functionList := [F1, F2, F3, F4, F5]: colorList := [C1, C2, C3, C4, C5]: legendList := [L1, L2, L3, L4, L5]:
symbolList := [S1, S2, S3, S4, S5]: styleList := [pointline, pointline, pointline, pointline, pointline]:
plot([seq(functionList[k], k = [1, 2, 3, 4, 5])], x = axeX, 'numpoints' = res, thickness = 2.4, 'style' = [seq(styleList[k], k = [1, 2, 3, 4, 5])], 'colour' = [seq(colorList[k], k = [1, 2, 3, 4, 5])], 'legend' = [seq(legendList[k], k = [1, 2, 3, 4, 5])], 'symbol' = [seq(symbolList[k], k = [1, 2, 3, 4, 5])], 'legendstyle' = ['location' = right, font = [dfont, axeSize]], 'symbolsize' = sSize, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"]);
```

Parametric Sweep for an Optimum Value of D

```

Dsp := 0.62;
Fsym := x->RL(Dsp, x); with(ArrayTools): vectest := RegularArray(0.1 .. 2.5, 30); FNum := evalf(seq(Fsym(x), x = eval(vectest))); RLmax := max(FNum);
Fsym := x->Lsh(Dsp, x); with(ArrayTools): vectest := RegularArray(0.1 .. 2.5, 30); FNum := evalf(seq(Fsym(x), x = eval(vectest))); Lshmax := max(FNum);
Fsym := x->Csh(Dsp, x); with(ArrayTools): vectest := RegularArray(0.1 .. 2.5, 30); FNum := evalf(seq(Fsym(x), x = eval(vectest))); Cshmax := max(FNum);
Fsym := x->VCshsm(Dsp, x); with(ArrayTools): vectest := RegularArray(0.1 .. 2.5, 30); FNum := evalf(seq(Fsym(x), x = eval(vectest))); VCshsmmax := max(FNum);
F1 := RL(Dsp, x)/RLmax; L1 := typeset[RL][Omega]/round(1000*Lshmax); S1 := asterisk; C1 := black;
F2 := Lsh(Dsp, x)/Lshmax; L2 := typeset[L][SH][mH]/round(1000*Lshmax); S2 := solidbox; C2 := gray;
F3 := Csh(Dsp, x)/Cshmax; L3 := typeset[C][SH][nF]/round(0.10*10^10*Cshmax); S3 := solidcircle; C3 := black;
F4 := VCshsm(Dsp, x)/VCshsmmax; L4 := typeset[VC][SHm][V]/round(1.0*10^10*VCshsmmax); S4 := diagonalcross; C4 := gray;
F5 := typeset[D, Dsp]; Labx := 'q'; Laby := 'Components'; axesX := 0 .. 2.5; axesY := 0 .. 1; sSize := 12; dfont := "TIMES"; titSize := 12; axisSize := 20; functionList := [F1, F2, F3, F4, F5]; colorList := [C1, C2, C3, C4, C5]; legendList := [L1, L2, L3, L4, L5]; symbolList := [S1, S2, S3, S4, S5]; styleList := [pointline, pointline, pointline, pointline, pointline];
plot(seq(functionList[k], k = [1, 2, 3, 4, 5]), x = axesX, y = axesY, 'numpoints' = 1, 'thickness' = 2.4, 'style' = [seq(styleList[k], k = [1, 2, 3, 4, 5])], 'colour' = [seq(colorList[k], k = [1, 2, 3, 4, 5])], 'legend' = [seq(legendList[k], k = [1, 2, 3, 4, 5])], 'symbol' = [seq(symbolList[k], k = [1, 2, 3, 4, 5])], 'legendstyle' = ['location' = right, font = [dfont, axisSize]], 'symbolsize' = sSize, font = [title, dfont, titSize], font = [axes, dfont, axisSize], 'labels' = [Labx, Laby], labelDirections = ['horizontal', 'vertical'], 'title' = [Tit]);

```

If Step 4 is well Developed, the Plots of the Search Space will be as Follows

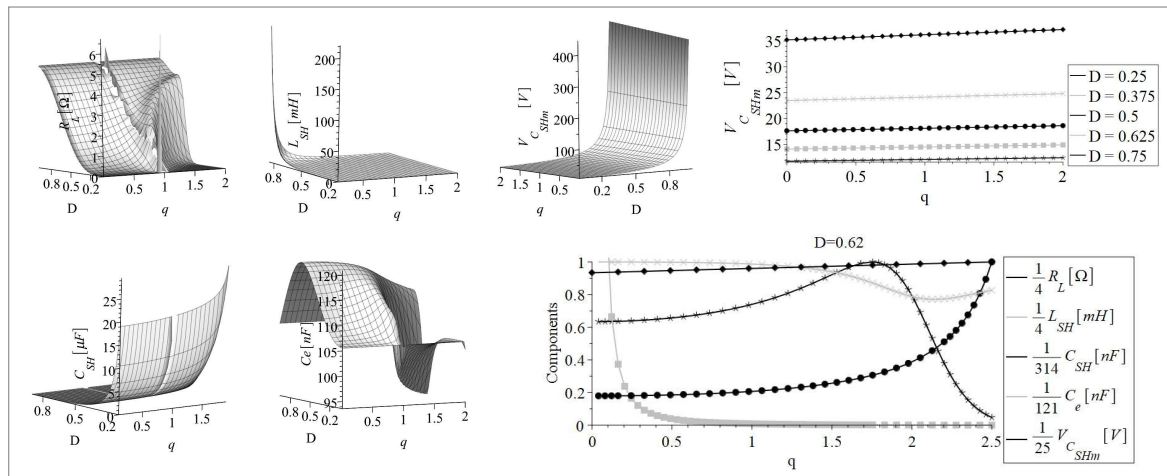


Figure A5. Search space of approach B.

Appendix B.2.3. Calculate the Circuit Values

Circuit Values

```

Dsp := 0.62;
qsp := 1.821;
evalf(RL(Dsp, qsp));
evalf(Lsh(Dsp, qsp));
evalf(Csh(Dsp, qsp));
evalf(Ce(Dsp, qsp));
evalf(VCshsm(Dsp, qsp));

```

Verify the Following Values:

$\text{evalf}(RL(Dsp, qsp));$	3.95
$\text{evalf}(Lsh(Dsp, qsp));$	7.51×10^{-6}
$\text{evalf}(Csh(Dsp, qsp));$	101.74×10^{-9}
$\text{evalf}(Ce(Dsp, qsp));$	102.36×10^{-9}
$\text{evalf}(VCshsm(Dsp, qsp));$	24.37

Figure A6. Component values of approach B.

Appendix B.2.4. Plot the Circuit Waveforms

v_g Plot

```
vg := t -> piecewise(t <= Dsp*aux, 1, Dsp*aux < t, 0);
aux := 1/fsp: axeX := 0 .. 1*aux: Tit := typeset(Switch*driver*waveform): Labx := "Time [s]": Laby := "Amplitude [V]": sSize := 12: dfont := "Times": titSize := 15: axeSize := 15:
plot(vg(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);
```

$v_{C_{SH}}$ Plot

```
vCsh := t -> piecewise(x <= Dsp*aux, 0, Dsp*aux < x, VDDsp*(1 + C1_VDD(Dsp, qsp)*cos(&omega;sp*qsp*t) + C2_VDD(Dsp, qsp)*sin(&omega;sp*qsp*t) - qsp^2*p(Dsp, qsp)*cos(&omega;sp*t + Phi(Dsp, qsp)))/(-qsp^2 + 1));
aux := 1/fsp: axeX := 0 .. 1*aux: Tit := typeset(Switch*voltage*waveform): Labx := "Time [s]": Laby := "Amplitude [V]": sSize := 10: dfont := "Times": titSize := 15: axeSize := 15:
plot(vCsh(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);
```

i_s Plot

```
Ip := (D, q) -> 2*gx(D, q)*VDDsp/RL(D, q);
Is := t -> piecewise(x <= Dsp*aux, VDDsp*t/Lsh(Dsp, qsp) - Ip(Dsp, qsp)*sin(Phi(Dsp, qsp)) + Ip(Dsp, qsp)*sin(&omega;sp*t + Phi(Dsp, qsp)), Dsp*aux < x, 0);
aux := 1/fsp: axeX := 0 .. 1*aux: Tit := typeset(Switch*current*waveform): Labx := "Time [s]": Laby := "Amplitude [A]": sSize := 10: dfont := "Times": titSize := 15: axeSize := 15:
plot(Is(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);
```

$i_{C_{SH}}$ Plot

```
iCsh := t -> piecewise(x <= Dsp*aux, 0, Dsp*aux < x, VDDsp*t/Lsh(Dsp, qsp) - int(vCsh(tt), tt = Dsp/fsp .. t)/Lsh(Dsp, qsp) + Ip(Dsp, qsp)*(sin(&omega;sp*t + Phi(Dsp, qsp)) - sin(Phi(Dsp, qsp))));
aux := 1/fsp: axeX := 0 .. 1*aux: Tit := typeset(C[SH]*current*waveform): Labx := "Time [s]": Laby := "Amplitude [A]": sSize := 12: dfont := "Times": titSize := 15: axeSize := 15:
plot(iCsh(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);
```

$i_{L_{SH}}$ Plot

```
iLsh := t -> piecewise(x <= Dsp*aux, VDDsp*t/Lsh(Dsp, qsp) - Ip(Dsp, qsp)*sin(Phi(Dsp, qsp)), Dsp*aux < x, VDDsp*t/Lsh(Dsp, qsp) - Ip(Dsp, qsp)*sin(Phi(Dsp, qsp)) - int(vCsh(tt), tt = Dsp/fsp .. t)/Lsh(Dsp, qsp));
aux := 1/fsp: axeX := 0 .. 1*aux: Tit := typeset(L[SH]*Current*waveform): Labx := "Time [s]": Laby := "Amplitude [A]": sSize := 12: dfont := "Times": titSize := 15: axeSize := 15:
plot(iLsh(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);
```

i_{R_L} Plot

```
iRL := t -> Ip(Dsp, qsp)*sin(&omega;sp*t + Phi(Dsp, qsp));
aux := 1/fsp: axeX := 0 .. 1*aux: Tit := typeset(RL*Current*waveform): Labx := "Time [s]": Laby := "Amplitude [A]": sSize := 12: dfont := "Times": titSize := 15: axeSize := 15:
plot(iRL(x), x = axeX, font = [title, dfont, titSize], font = [axes, dfont, axeSize], 'labels' = [Labx, Laby], labeldirections = ["horizontal", "vertical"], 'title' = [Tit], color = "black", style = line, thickness = 2.6, size = [0.5, 0.5]);
```

If the Maple™ Process is well Developed, the Waveforms of the Circuit will be as Follows:

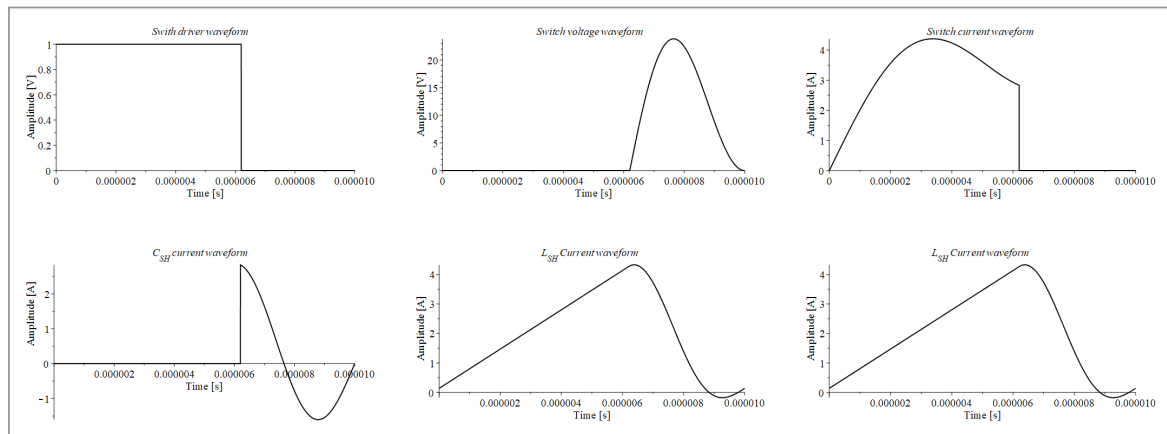


Figure A7. Model circuit waveforms of approach B.

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