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A 5.43 nV/ $\sqrt{\text{Hz}}$ Chopper Operational Amplifier Using Lateral PNP Input Stage with BJT Current Mirror Base Current Cancellation

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Abstract: This paper presents a low-noise chopper operational amplifier using a lateral PNP input stage with bipolar junction transistor (BJT) current mirror base current cancellation. The BJT has a lower noise characteristic than the metal–oxide–semiconductor (MOS) transistor, where low-noise characteristics can be achieved by implanting the BJT to the input stage of the amplifier; however, the base current of the BJT input stage causes low input impedance of the amplifier. The BJT current mirror base current cancellation technique is implemented to enhance the input impedance of the BJT input stage by canceling the base current. BJT current mirror base current cancellation is implemented with a simple scheme using NPN transistors with deep n-well in a generic complementary metal–oxide–semiconductor (CMOS) process. For further noise reduction with the BJT input stage, a chopper amplifier scheme is adopted to reduce low-frequency components such as $1/f$ noise terms in the low-frequency range. The prototype chip is fabricated in a 0.18- μm CMOS process. The active area of the prototype amplifier is 0.213 mm². The measured input-referred noise is 5.43 nV/ $\sqrt{\text{Hz}}$. The measured input base current of the amplifier with base current cancellation is 67.971 nA. The total amplifier current consumption is 278.3 μA , with a power supply of 3.3 V.

Keywords: low-noise operational amplifier; chopper amplifier; lateral PNP; BJT current mirror base current cancellation

1. Introduction

In recent years, various products of precision amplifiers for sensor readout applications have been reported [1–5], e.g., low-noise characteristics essential for low speed and precision-sensing readout circuits. Low-noise techniques such as autozeroing and chopper stabilization are widely implemented in low-noise circuit designs [6–10]. Autozeroing can achieve a low-noise characteristic; however, the noise level is limited by the high-frequency noise-folding. The chopper stabilization technique can also achieve a low-noise characteristic; however, ripples caused by modulated low-frequency noises occur, and a large low-pass filter (LPF) is needed to reject those ripples. The multipath amplifier scheme with chopper stabilization is suitable for precision-sensing, achieving low-noise and low-offset characteristics with a wide bandwidth [11–14]. The multipath amplifier scheme, however, has high circuit complexity, causing difficulties in circuit design.

Bipolar junction transistors (BJTs) can be implemented in the input stage of the amplifier for achieving lower noise characteristics than metal–oxide–semiconductor (MOS) transistors [15]. The implementation of BJTs in a complementary metal–oxide–semiconductor (CMOS) process has been

reported in previous works [16–21]. The implementation of a BJT into the input stage of an amplifier can achieve a low-noise characteristic; however, the biggest disadvantage of BJTs in the input stage of the amplifier is the low input impedance caused by the large input bias current caused by the base current [20].

In this paper, a low-noise chopper operational amplifier using a lateral PNP input stage with BJT current mirror base current cancellation is presented. The input stage of the amplifier is implemented with a custom-designed lateral PNP in a standard 0.18- μm CMOS process. The BJT current mirror base current cancellation scheme is implemented to cancel the base current and enhance input impedance. The BJT current mirror base current cancellation scheme is implemented with a simple scheme using NPN transistors with deep n-well. The chopper amplifier scheme is implemented for further noise reduction with the BJT input stage in the low-frequency range by reducing low-frequency components such as $1/f$ noise terms.

2. Circuit Implementation

The overall noise of an amplifier is majorly caused by the input differential pair, which means that the input transistors of the differential pair are the noise source of the amplifier. As shown in previous works, the BJT has a better low-noise characteristic than the MOS transistor when the same amount of bias current is supplied [15]. Vertical BJTs are supported by the process design kit (PDK) in a standard CMOS process. The supported vertical PNP of the standard CMOS process, however, has a limitation—for implementing to the input stage of the amplifier, the collector is tied with the substrate, which enables its use only in such cases as bandgap reference circuits [16]. Due to this limitation of the vertical BJT in circuit design, a lateral BJT is designed and implemented in this work. The input differential pair is implemented with lateral PNP in this work. The implemented lateral PNP is shown in Figure 1. The top view and cross-sectional view of the implemented lateral PNP are shown in Figures 1a,b. The lateral PNP is designed in a standard 0.18- μm CMOS process. The custom lateral PNP is designed with minimum length, satisfying the design rule of the standard 0.18- μm CMOS process. The lateral PNP is designed as a gated PNP, which is formed by gate polysilicon. The lateral PNP in this work is based on previously reported works [18–21]. The gate of the design lateral PNP is biased with a supply voltage of 3.3 V. The measured current gain (β) dependence on the voltage across the base and emitter (V_{BE}) of the implemented lateral PNP is shown in Figure 1c. The β dependence on V_{BE} shows the trend of β by the voltage sweep of V_{BE} across 0.4 to 1.0 V. The measured maximum β is 9.3. The low β is caused by the large base current, which causes a low input impedance of the amplifier.

The proposed low-noise chopper operational amplifier using a lateral PNP input stage with BJT current mirror base current cancellation is shown in Figure 2. The input stage of the amplifier is implemented with a custom-designed lateral PNP. The base current caused by the lateral PNP differential input leads to low input impedance. The BJT current mirror base current cancellation scheme is implemented to reduce the base current caused by the lateral PNP input stage. The base current cancellation control switches (SW_1 and SW_2) are integrated for controlling the base current cancellation. The proposed chopper amplifier is adopted with a folded cascode and a class-AB output stage. The integrated compensation capacitors C_{C1} and C_{C2} are 41.8 pF. The chopper clock signals are nonoverlapping clocks, and the chopper frequency (f_c) is 250 kHz.

The operation of the proposed BJT current mirror base current cancellation is shown in Figure 3. The BJT current mirror base current cancellation is implemented with a simple scheme using NPN transistors with deep n-well in a generic CMOS process. The base current flow before the base current cancellation operation is shown in Figure 3a. The output base currents I_{B1} and I_{B2} of the differential input pair Q_1 and Q_2 cause input bias currents I_{IN1} and I_{IN2} . The operation of the proposed BJT current mirror base current cancellation is shown in Figure 3b. The base current cancellation operates when the control switches SW_1 and SW_2 are turned on. The base currents I_{B1} and I_{B2} of the differential input pair Q_1 and Q_2 can be compensated by the base current cancellation. The collector currents I_{C1} and I_{C2}

generated by Q_1 and Q_2 flow through PNP transistors Q_3 and Q_4 . The collector currents I_{C1} and I_{C2} are the same as I_{C3} and I_{C4} of Q_3 and Q_4 , which can be expressed as (1) and (2).

$$I_{C1} = I_{C3} \quad (1)$$

$$I_{C2} = I_{C4} \quad (2)$$

The PNP transistors Q_3 and Q_4 copy and generate the same base currents as Q_1 and Q_2 by the collector currents I_{C3} and I_{C4} flowing through them. The generated base currents I_{B3} and I_{B4} are the same as the base currents I_{B1} and I_{B2} of input PNP transistors Q_1 and Q_2 as (3) and (4).

$$I_{B1} = I_{B3} \quad (3)$$

$$I_{B2} = I_{B4} \quad (4)$$

The generated base currents I_{B3} and I_{B4} of Q_3 and Q_4 are mirrored by the BJT current mirror generating $I_{COMPEN1}$ and $I_{COMPEN2}$ for base current compensation, which can be expressed as (5) and (6).

$$I_{B3} = I_{COMPEN1} \quad (5)$$

$$I_{B4} = I_{COMPEN2} \quad (6)$$

The input bias currents I_{IN1} and I_{IN2} are compensated by the compensation currents $I_{COMPEN1}$ and $I_{COMPEN2}$ by the proposed BJT current mirror base current cancellation, and the input bias currents I_{IN1} and I_{IN2} are ideally zero by the proposed compensation circuits. The input bias currents I_{IN1} and I_{IN2} compensated by base current compensation can be expressed as (7) and (8).

$$I_{IN1} = I_{COMPEN1} - I_{B1} \quad (7)$$

$$I_{IN2} = I_{COMPEN2} - I_{B2} \quad (8)$$

Figure 1. (a) Top view of implemented lateral PNP; (b) cross-sectional view of implemented lateral PNP; (c) measured β dependence on V_{BE} .

Figure 2. Schematic of low-noise chopper operational amplifier using a lateral PNP input stage with BJT current mirror base current cancellation.

Figure 3. (a) Before base current cancellation operation; (b) operation of proposed BJT current mirror base current cancellation.

3. Measurement Results

The die photograph of the fabricated low-noise chopper operational amplifier is shown in Figure 4. The prototype chopper operational amplifier is fabricated by a 0.18- μm CMOS process. The prototype chip has an amplifier-active area of 0.213 mm^2 . The measured total current consumption of the chopper operational amplifier is 278.3 μA , with a power supply of 3.3 V.

The measurement environment of the prototype chopper operational amplifier is shown in Figure 5. The prototype amplifier is tested on a designed printed circuit board (PCB) by a chip-on-board process (COB) connected by wire bonding. The DC power supply supplies 3.3 V of power, and the gate of the lateral PNP input stage is biased with 3.3 V. The waveform generator generates input pulses and sinusoidal signals for amplifier configuration tests. The dynamic signal analyzer is used for spectrum analysis, and a digital oscilloscope is used for signal acquisition.

Figure 4. Die photograph of prototype chopper operational amplifier.

Figure 5. Measurement environment of prototype chopper operational amplifier.

The open-loop gain measurement result of the proposed chopper operational amplifier is shown in Figure 6. The measured average open-loop gain is 115 dB, and the measured gain bandwidth (GBW) of the chopper operational amplifier is 2.30 MHz, with a chopper frequency of 250 kHz.

The measurement results of the input-referred noise are shown in Figure 7. The measured input-referred noise with the chopper off is shown in Figure 7a. The measured input-referred noise, with the chopper off at 1 Hz, is $36.3 \text{ nV}/\sqrt{\text{Hz}}$. The measured input-referred noise level with the chopper off is $7.31 \text{ nV}/\sqrt{\text{Hz}}$, with a noise-integrated bandwidth of 0.5 to 800 Hz. The measured input-referred noise with the chopper on, with a chopper frequency of 250 kHz, is shown in Figure 7b. The measured input-referred noise, with the chopper on at 1 Hz, is $29 \text{ nV}/\sqrt{\text{Hz}}$. The measured input-referred noise level with the chopper on is $5.43 \text{ nV}/\sqrt{\text{Hz}}$, with a noise-integrated bandwidth of 0.5 to 800 Hz. The measurement results show that the implementation of the BJT input stage can achieve a low-noise characteristic compared to previous works [13,14,22]. The measurement results, with the chopper off and on, show that the overall noise characteristic can be improved by using the chopper.

The measurement results of the input base current, with a chopper frequency of 250 kHz, are shown in Figure 8. The measured input base current without the proposed base current cancellation is 156.263 nA , which is shown in Figure 8a. The measured input base current with the proposed base current cancellation is 67.971 nA , which is shown in Figure 8b. The measurement results show that the proposed base current cancellation does not completely cancel the input base current; however, the input base current can be compensated by reducing the input base current by more than half of that before the base current cancellation operation.

The common mode rejection ratio (CMRR) measurement result of the proposed chopper operational amplifier is shown in Figure 9. The measured average CMRR is 115.1 dB , and CMRR at 60 Hz is 90.9 dB with a chopper frequency of 250 kHz.

The power supply rejection ratio (PSRR) measurement result of the proposed chopper operational amplifier is shown in Figure 10. The measured average PSRR is 66.6 dB , and PSRR at 60 Hz is 68.3 dB with a chopper frequency of 250 kHz.

Figure 6. Open-loop gain measurement result of the proposed chopper operational amplifier.

Figure 7. (a) Measured input-referred noise with the chopper off; (b) Measured input-referred noise with the chopper on.

Figure 8. (a) Measured input base current without base current cancellation; (b) measured input base current with base current cancellation.

Figure 9. Common mode rejection ratio (CMRR) measurement result of the proposed chopper operational amplifier.

Figure 10. Power supply rejection ratio (PSRR) measurement result of the proposed chopper operational amplifier.

The slew rate measurement result is shown in Figure 11. The slew rate measurement proceeded with a buffer configuration, with a loading output load of 10 k Ω and 120 pF. The input voltage signal is given, with a range of 1.315 V to 1.985 V and a frequency of 100 kHz. The measured rising and falling slew rates are each 0.609 V/ μ s.

The transient measurement result of the proposed chopper operational amplifier with a buffer configuration is shown in Figure 12. The buffer-transient measurement proceeded with a buffer configuration, with a loading output load of 10 k Ω and 120 pF. The input sinusoidal signal was given, with an amplitude of 250 mV and a frequency of 100 kHz. The measurement result shows that the chopper operational amplifier with a buffer configuration operates in a normal operational condition.

The transient measurement result of the proposed chopper operational amplifier with an inverting amplifier configuration is shown in Figure 13. Resistors of 5 and 10 k Ω were used for the inverting amplifier configuration, amplifying a gain of 2. The measurement result shows that the chopper operational amplifier with an inverting amplifier configuration operates in a normal operational condition.

Figure 11. Slew rate measurement result of the proposed chopper operational amplifier.

Figure 12. Transient measurement result of the proposed chopper operational amplifier with a buffer configuration.

Figure 13. Transient measurement result of the proposed chopper operational amplifier with an inverting amplifier configuration.

4. Discussion

Table 1 shows a performance summary and comparison with previously reported works. The noise efficiency factor (NEF) is calculated with current consumption, input-referred noise, and bandwidth for comparison of those amplifier performances [15]. The equation for calculating NEF can be expressed as Equation (9).

$$NEF = V_{rms,in} \cdot \sqrt{\frac{2 \cdot I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \quad (9)$$

$V_{rms,in}$ is the input-referred noise, I_{tot} is the amplifier's total current consumption, $4kT$ is the thermal voltage, and BW is the amplifier bandwidth.

The NEF of the proposed amplifier is 3.98 with amplifier GBW and noise integration bandwidth of 3 MHz, which is similar and comparable to previously reported works. The measured input-referred noise of 5.43 nV/√Hz shows that the implementation of a BJT as the input of the amplifier can improve the noise performance of the amplifier.

Table 1. Performance summary and comparison.

	This Work	[14]	[22]	[13]	[20]
Year	2020	2020	2011	2010	1995
Process (μm)	0.18	0.18	0.35	0.7	1.2
Input stage transistor	BJT	MOS transistor	MOS transistor	MOS transistor	BJT
Amplifier scheme	Chopper amplifier	Multipath amplifier	Multipath amplifier	Multipath amplifier	2-stage amplifier
Supply voltage (V)	3.3	1.8	2.5–5.5	5	± 2.5
Current consumption (μA)	278.3	96.7	1470	143	2100
DC gain (dB)	115	>137	>150	-	20.8 (closed loop)
BW (MHz)	2.30	3.16	4	1.8	122
Input referred noise ($\text{nV}/\sqrt{\text{Hz}}$)	5.43	11.8	5.9	10.5	3.2
Input bias current (nA)	67.971	-	0.072	<0.250	1680
CMRR (dB)	90.9	>125	>150	137	99.6
PSRR (dB)	68.3	>100	>150	120	67.6
Area (mm^2)	0.213	1.18	1.26	1.8	0.211
NEF	3.98 *	4.46	8.4	4.8	5.64

* Noise efficiency factor (NEF) with measured gain bandwidth (GBW) and noise integration bandwidth (BW) of 3 MHz.

5. Conclusions

In this paper, a low-noise chopper operational amplifier using a lateral PNP input stage with BJT current mirror base current cancellation is presented. The implementation of a BJT to the amplifier input stage can achieve improved noise performance compared to the amplifiers with a MOS transistor input stage due to the lower noise characteristic of BJTs. However, the base current of the BJT input stage causes a low input impedance of the amplifier. The proposed BJT current mirror base current cancellation, with a simple scheme, can reduce the output base current. The proposed amplifier is fabricated in a generic 0.18- μm CMOS process. The amplifier-active area is 0.213 mm^2 , and the total amplifier current consumption is 278.3 μA with a 3.3 V power supply. The measured input base current of the amplifier with base current cancellation was 67.971 nA, which shows that the proposed BJT current mirror base current cancellation scheme can compensate for the output base current of BJT input. The input-referred noise level is 5.43 $\text{nV}/\sqrt{\text{Hz}}$, with a NEF performance of 3.98. The proposed chopper operational amplifier achieved a low-noise characteristic and improved the input bias current using a lateral PNP input stage with BJT current mirror base current cancellation.

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