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Inductance Model of a Backside Integrated Power Inductor in 2.5D/3D Integration

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Featured Application: A fully integrated power inductor using a silicon interposer is proposed, which is appropriate for miniaturized power management applications.

Abstract: Inductor integration is of vital importance for miniaturization of power supply on chips. In this paper, a backside integrated power inductor is presented. The inductor is placed at the backside of a silicon interposer and connected to the front side metal layers by through-silicon vias (TSVs) for area saving and simple fabrication. An inductance model is proposed to effectively capture the total inductance of the power inductor by an analytical method. The results obtained from the analytical model and finite element method exhibit good agreement with various design parameters and the error between the proposed model and measurement remains less than 7.91%, which indicates that the proposed model can predict the inductance suitably.

Keywords: fully integrated inductor; inductance model; through-silicon vias (TSVs); mutual inductance; 3D integration

1. Introduction

An inductor is a fundamental component for electronic devices, which is used for energy storage and filtering, but it dominates in size and loss. To achieve its miniaturization and aid lowering the cost of the power supply on chip, monolithic integration of power inductors is essential [1–4]. Lots of design methodologies and fabrication technologies have been proposed for potential monolithic integration.

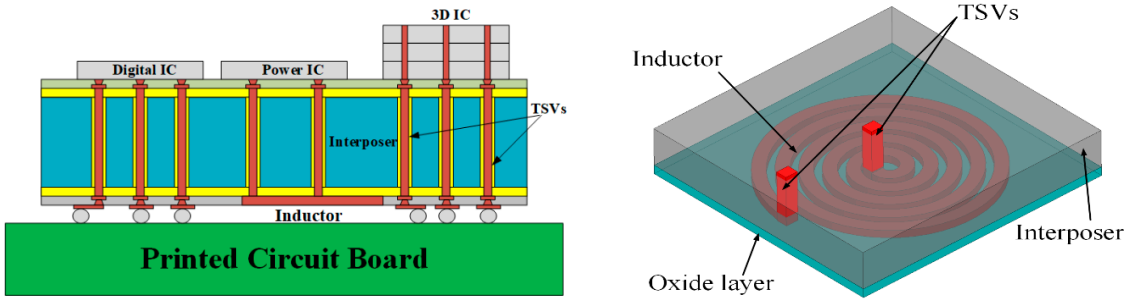
The increase in switching frequencies of power circuits up to megahertz can significantly reduce the inductor's size [5,6]. A tiny 0.47 µH inductor has been used in a commercial 8 MHz PWM synchronous Buck regulator [5]. A 250 MHz buck regulator has been implemented with a 12 nH wire-bond power inductor in [6]. However, such a high frequency will cause high power switching and result in poor efficiency (e.g., 71% [6]). Furthermore, the power inductor with low inductance easily introduces a high ripple current. Various magnetic core materials have been adopted to enhance the inductance density for monolithic integration of power inductors [7–9]. A 3D in-silicon magnetic core toroidal inductor is presented in [7], in which the magnetic powder-based core is embedded into an air-core inductor using a casting method. A 3D solenoid inductor that is embedded in the substrate and integrated an iron core is reported in [8]. However, the introduction of magnetic material not only causes a core saturation issue but also increases the design and fabrication complexity.

In this paper, a fully integrated air-core power inductor is proposed, which is developed for a high-density silicon-interposer based on 2.5D and 3D integrated circuits, and a compact analytical model has been derived to capture the total inductance of the proposed inductor, where the screw pitch and cross-sectional sharp are considered. Comparted to traditional circular coil method [10,11] and the model developed for coils with a circular section-area [12], the proposed model can offer a better

accuracy and is more suitable for the inductance prediction of power inductance fabricated with 2D planar technology.

2. Inductance Model Description

Figure 1a shows the cross-section schematic of a silicon-interposer-based 3D IC package, in which the interposer acts as bridges between the active chips and printed circuit board package [13,14]. In addition to the interconnection, the interposer provides the functionalities with passive components integration. Various integrated passive devices, such as TSV inductors, TSV capacitors and TSV filters, have been presented [15–17]. However, these studies focus on the utilization of tiny TSVs. The TSV-based solenoid inductor has a low inductance and is not suitable for power device applications. In this design, a fully integrated power inductor is proposed, as shown in Figure 1. The proposed inductor is designed to be placed at the backside of the interposer for efficiently utilizing the silicon area and can be connected to the front side power circuits through TSVs. A thin oxide dielectric is inserted between the inductor and silicon substrate to obtain a high-quality factor.



(**a**) (**b**)

Figure 1. Schematic of (**a**) the 3D IC package and (**b**) the 3D view of the proposed backside integrated power inductor.

Figure 2 shows the major fabrication steps of the proposed power inductors. Firstly, the via structure is formed at the front side of the interposer by deep reactive ion etching (Figure 2a). The etched via is then processed with an oxide dielectric, a Ta barrier and a Cu seed layer, followed by the acid Cu electroplating (Figure 2b). The Cu damascene technique [18] is adopted to fabricate the redistribution layers (RDLs) and the vias connecting the TSVs to the RDLs (Figure 2c). The topside of the interposer wafer is temporarily bonded to a carrier by adhesive and a back grinding is carried out to a few microns to the TSVs (Figure 2d). The proposed inductor is implemented by the RDLs at the backside with the Cu damascene method and the vias connecting the TSVs and the inductor are completed (Figure 2e). Finally, one de-bonds the carrier wafer and assembles the TSV module on the package substrate (Figure 2f).

With the help of the finite-element method simulation with HFSS software, the electrical performance of the proposed backside integrated inductor with a size of 1 mm^2 is investigated. Table 1 provides a performance comparison for the proposed backside integrated inductor with other state-of-the-art works. Where L, Q, f and R_{DC} are the inductor inductance, qualify factor, switching frequency and dc resistance, respectively; η is the inductor efficiency, which is estimated by the inductor parameters and the equation in [19,20] for power efficiency. Since the oxide dielectric provides a good isolation between the inductor and the silicon substrate, it is observed that the proposed inductor achieves a higher qualify factor, leading to a peak inductor efficiency of 87.3% for a typical voltage conversion ratio of 1.8 V:0.9 V and load current of 100 mA. On the contrary, substrate loss and eddy current loss significantly decrease the quality and efficiency of the silicon-core inductors and magnetic-core inductors. Furthermore, in comparison to the toroidal inductor, the proposed embedded inductor is more compatible with the standard CMOS process.

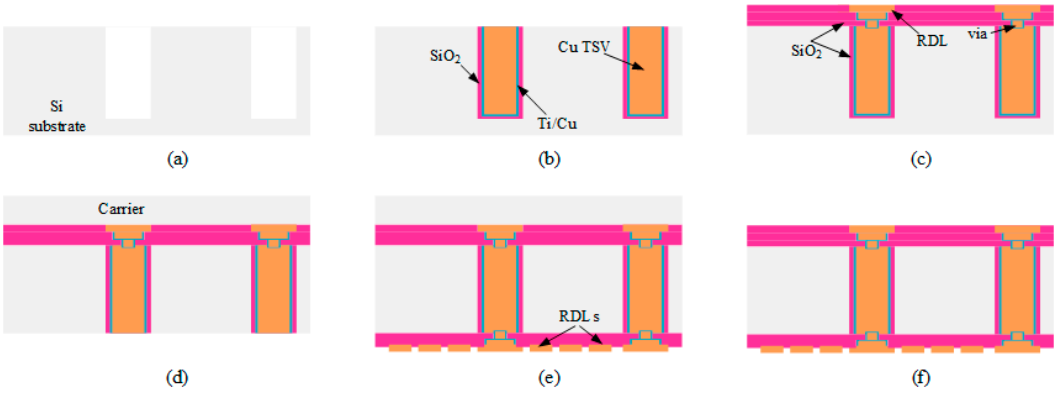


Figure 2. Schematic of the major fabrication steps:(**a**) via formation, (**b**) via filling, (**c**) RDLs and vias formation, (**d**) Temporary bonding and backside grinding, (**e**) inductor formation, (**f**) TSV module assemble.

Table 1. Comparison of the proposed backside integrated inductor with the prior integrated power inductors.

	Inductor Technology	L (nH)	Q@f	RDC (mΩ)	*H* (%)
This work	Backside integrated air core	208	15@32 MHz	1200	87.3
[19] 2011	Silicon embedded silicon core	15.8	5.5@16 MHz	291	53.2
[21] 2018	In-Si 3D toroid silicon core	43.67	9@20 MHz	1250	77.6
[8] 2019	In-Si 3D toroid magnetic core	229.5	1.74@5 MHz	2000	55.2
[7] 2019	In-Si 3D toroid magnetic core	112	11.5@12.5 MHz	265	90.7

Based on the above structure, the resistance–inductance–capacitance (RLC) model of the backside integrated inductor can be established. Considering that the inductance is one of the critical parameters for inductors in power management applications, this work focuses on the modeling and analysis of the inductance of the proposed inductor. For the basis analysis, it is assumed that the track width is w, the track spacing is s and the track thickness is t. The linked flux of the inductor determined its inductance. For a one-turn inductor, the overall inductance of the inductor is equal to its self-inductance. For multi-turn inductors, there is mutual coupling between each turn, and then the magnetic field strength through the inductor and the linked flux significantly increases with the number of turns, as shown in Figure 3. Therefore, the overall inductance of the inductor is the sum of the self-inductance and increased mutual inductance between each turn [22]. For the proposed Archimedean spiral coil with a rectangular cross section area and n concentric turns, the total inductance L_{T} can be written as the sum over the self-inductance L_{S} and the mutual inductance L_{M} of all turns,

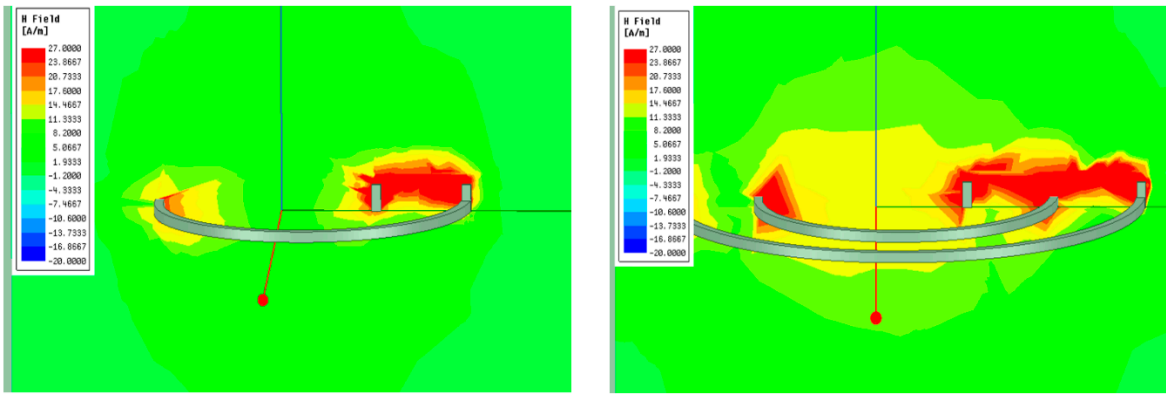
$$L_{\mathrm{T}} = L_S + L_M = L_S + \sum_{i=1}^{n} \sum_{j=1}^{n} M_{ij} \tag{1}$$

where M_{ij} represent the mutual inductance between the ith turn coil and jth turn coil. The overall self-inductance L_{S} can be further approximated as a function of coil geometry [23],

$$L_{\mathrm{S}} = \frac{\mu l_{eng}}{2\pi} \times \left(\log\left(\frac{2l_{eng}}{w+t} \right) + 0.5 + \frac{w+t}{3l_{eng}} \right) \tag{2}$$

where l_{eng} is the total length of the n-turn coil, and $\mu = 4\pi \times 10^{-7}$ H/m is the permittivity of the surrounding medium. For an Archimedean spiral coil with an inner radius R_0 and screw pitch p ($p = w + s$), l_{eng} can be calculated by

$$l_{eng} = \int_0^{2\pi \times n} \sqrt{\left(R_0 + \frac{p\theta}{2\pi}\right)^2 + \left(\frac{p}{2\pi}\right)^2} d\theta \tag{3}$$



(**a**) (**b**)

Figure 3. Magnetic field strength in (**a**) a one-turn coil and (**b**) a two-turn coil.

The mutual inductance M_{ij} can be calculated using the classical magnetic vector potential approach as [22,24–26]

$$M_{ij} = \frac{\mu_0}{4\pi} \frac{\vec{dl_i} \times \vec{dl_j}}{R} \tag{4}$$

For an Archimedean spiral coil, the tangent vector of point P ($R_i\cos\theta_1$, $R_i\sin\theta_1$, 0) on the ith coil and point Q ($R_j\cos\theta_2$, $R_j\sin\theta_2$, 0) on the jth coil can be derived as

$$\begin{cases} \vec{dl_i} = dx_i\vec{i} + dy_i\vec{j} \\ \quad = \frac{p}{2\pi}\left[(\cos\theta_1 - \theta_1\sin\theta_1)\vec{i} + (\sin\theta_1 + \theta_1\cos\theta_1)\vec{j}\right]d\theta_1 \\ \vec{dl_j} = dx_j\vec{i} + dy_j\vec{j} \\ \quad = \frac{p}{2\pi}\left[(\cos\theta_2 - \theta_2\sin\theta_2)\vec{i} + (\sin\theta_2 + \theta_2\cos\theta_2)\vec{j}\right]d\theta_2 \end{cases} \tag{5}$$

and then

$$\vec{dl_i} \times \vec{dl_j} = \frac{p^2}{4\pi^2}\begin{bmatrix} (1+\theta_1\theta_2)\cos(\theta_2 - \theta_1) - \\ (\theta_2 - \theta_1)\sin(\theta_2 - \theta_1) \end{bmatrix} d\theta_1 d\theta_2 \tag{6}$$

The distance between two points P and Q can be expressed as

$$R = \sqrt{\left(R_j\cos\theta_2 - R_i\cos\theta_1\right)^2 + \left(R_j\sin\theta_2 - R_i\sin\theta_1\right)^2} \tag{7}$$

Substituting Equation (5)–Equation (7) into Equation (4), M_{ij} can be obtained as

$$M_{ij} = \frac{\mu_0 p^2}{16\pi^3} \frac{(1+\theta_1\theta_2)\cos(\theta_2 - \theta_1) - (\theta_2 - \theta_1)\sin(\theta_2 - \theta_1)}{\sqrt{R_i^2 + R_j^2 - 2R_iR_j\cos(\theta_2 - \theta_1)}} \mathrm{d}\theta_1 \mathrm{d}\theta_2 \tag{8}$$

Substituting Equations (3) and (8) into Equation (1), the total inductance of the proposed Archimedean coil can be calculated.

3. Validation and Discussion

In this section, the inductances obtained from the proposed model, the traditional circular coil method (CCM), quasi-static electromagnetic simulation with Q3D, are compared [26]. Q3D is a fast-quasi-static electromagnetic field simulator and is good at RLCG parameter extraction. For the proposed power inductor with the inductance of ~1 µH, its switching frequency would not exceed 100 MHz. Therefore, Q3D can provide an accurate inductance extraction for the proposed power inductor. In the simulation environment, the two terminals of the inductor are defined as a source and sink, respectively, and the AC RL solver are adopted for inductance extraction. In the circular coil method [10,11], each loop is approximated as a circle and the radius of the ith turn is treated as $R_0 + (i-1)p$. The base parameters are w = 40 µm, t = 20 µm, s = 20 µm, R_0 = 20 µm and n = 26. As shown in Figure 4, the inductances with the proposed model agree well with the results of 3D simulators over various design parameters: the error with respect to the EM results is less than 9.5%, while the error of the traditional circular coil method is 40.2%. The comparison indicates that the proposed model can be used for inductance extraction of the fully integrated power inductor.

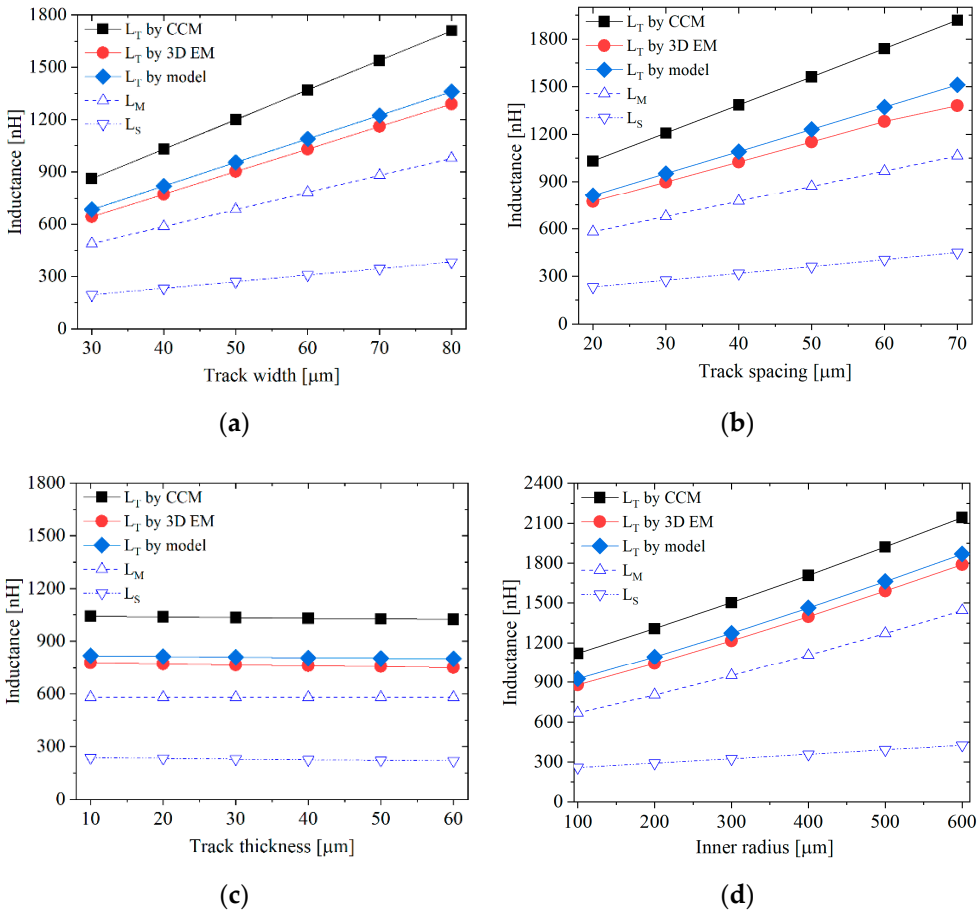


Figure 4. Impact of (**a**) track width, (**b**) track spacing, (**c**) track thickness and (**d**) inner radius on the total inductance.

Furthermore, the results in Figure 4a,b demonstrate that L_T increases with the track width w and track spacing s, due to the increased partial self-inductance and mutual inductance according to Equations (2) and (8). Since the variation in partial self-inductance and mutual inductance with track thickness t is little, it can be seen in Figure 4c that the impact of the parameter on L_T can be negligible.

Moreover, the results in Figure 4d show the overall inductance would increase with the inner radius of the inductor.

Table 2 investigates the computational efficiency of the model by comparing the simulation time of the proposed analytical model and 3D EM simulator using the parameters listed. The simulation was performed on an Intel i5 core with a processor speed of 3.0 GHz and 8 GB of RAM. It was found that lots of computational time can be saved using the proposed model.

Table 2. Comparison of computational efficiency.

Structure	This Model	3D EM Simulator
r_1 = 50 µm, n = 10	0.03 s	69.7 s
r_1 = 50 µm, n = 15	0.07 s	76.0 s
r_1 = 100 µm, n = 15	0.08 s	73.0 s
r_1 = 100 µm, n = 26	0.29 s	86.6 s
r_1 = 100 µm, n = 37	0.41 s	117.0 s

To verify the accuracy of the analytical expressions, the proposed model was applied to the fabricated power inductors. Taking into account the additional process steps for the 3D integration and the weak impact of the interposer materials on the inductor's performance, the proposed power inductor was fabricated with 2-layer Print Circuit Board (PCB) technology. In the emulated 3D integration environment shown in Figure 5a, the inductor is realized on the backside planar track. The vias in the PCB technology imitate the TSVs to connect the inductor to the frontside power circuits. Table 3 compares the inductances obtained from this model, the circular coil method (CCM) [10,11] and electrical measurement with a Hioko IM3570 Impedance Analyzer. By connecting the two terminals of the inductor to the two probes of the impedance analyzer, capable of measurement frequencies of 4 Hz to 5 MHz, the inductance at 1 MHz can be captured. It is observed that the proposed model shows a higher accuracy in comparison to CCM. The maximum error and average error of the proposed model are 7.91% and 3.72%, respectively, which indicates the feasibility of the proposed model for inductance prediction.

(**a**) (**b**)

Figure 5. (**a**) Schematic view of the fabricated power inductor and (**b**) its experimental setup.

Table 3. Comparison of the inductance results.

Size	This Model		CCM		Measurement
	Inductance (nH)	Error (%)	Inductance (nH)	Error (%)	Inductance (nH)
r_1 = 3 mm, n = 4	196.7	−2.64	182.2	−9.81	202
r_1 = 3 mm, n = 6	452.6	1.72	425.2	−4.40	445
r_1 = 3 mm, n = 8	814.6	1.96	796.4	−0.33	799
r_1 = 3 mm, n = 16	3725	6.29	4023.6	14.82	3504.4
r_1 = 6 mm, n = 4	419.1	−1.84	404.5	−5.27	427
r_1 = 6 mm, n = 6	931.1	2.56	888.2	−2.18	908
r_1 = 6 mm, n = 8	1635.3	4.62	1574.6	0.74	1563
r_1 = 6 mm, n = 16	6500	7.91	6749.2	12.05	6023.6
r_1 = 10 mm, n = 4	725.1	−5.96	742.9	−3.64	771
r_1 = 10 mm, n = 6	1608.6	−0.21	1594.6	−1.08	1612
r_1 = 10 mm, n = 10	4320.8	4.06	4256.9	2.53	4152
r_1 = 10 mm, n = 20	16200	5.49	17,269	12.45	15,357

4. Conclusions

In this paper, a power inductor integration technology for 2.5D/3D integrated power management applications is presented and experimentally demonstrated. The inductor can be integrated at the backside of the silicon interposer and interconnects with the frontside power circuits with TSVs. A compact and accurate inductance model is developed to capture the overall inductance of the proposed inductor. A comparison with 3D EM results shows that the proposed analytical model has a good prediction capability and a high computational efficiency. Furthermore, the model results show that the increase in track width, track spacing and inner radius of the inductor would increase the overall inductance, while the variation in the inductance with track thickness is less. Finally, the inductance from the proposed model and the measurements were compared, and an error of less than 7.91% was obtained.

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