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A New Split Gate Resurf Stepped Oxide UMOSFET Structure with High Doped Epitaxial Layer for Improving Figure of Merit (FOM)

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Featured Application: The split gate resurf stepped oxide with highly doped epitaxial layer (HDSGRSO) UMOSFET has extremely low on-state resistance, therefore, it can be used in synchronous rectification circuits to replace rectifier diodes to reduce rectification losses. It can greatly improve the efficiency of the DC/DC converter and there is no deadtime voltage caused by the Schottky barrier voltage. On the other hand, it can be applied to the high frequency switching due to its excellent dynamic characteristics.

Abstract: The split gate resurf stepped oxide with highly doped epitaxial layer (HDSGRSO) UMOSFET has been proposed. The epitaxial layer of HDSGRSO u-shape metal oxide semiconductor field effect transistor (UMOSFET) has been divided into three parts: the upper epitaxial layer, the lower epitaxial layer and the middle epitaxial layer with higher doping concentration. The research shows that the reduced SURface field (RESURF) active has been enhanced due to the high doped epitaxial layer, which can modulate the electric field distribution and reduce the internal high electric field. Therefore, the HDGRSO UMOSFET has a higher breakdown voltage (BV), a lower on-state specific resistance (R_{SP}) and a better figure of merit (FOM). According to the results of Technology Computer Aided Design (TCAD) simulations, the FOM (BV^2/R_{SP}) of HDSGRSO UMOSFET has been improved by 464%, and FOM ($R_{SP} \times Q_{gd}$) of HDSGRSO UMOSFET has been reduced by 27.9% compared to the conventional structure, respectively, when the BV is 240 V. Furthermore, there is no extra special process required in this advanced fabrication procedure, which is relatively cost-effective and achievable.

Keywords: UMOSFET; FOM; split gate; high doped epitaxial layer; electric field modulation

1. Introduction

The power MOSFET (metal oxide semiconductor field effect transistor) has been widely used in the analog and digital circuits. It is one of the most vital research fields to reduce the on-state specific resistance (R_{SP}) for a certain breakdown voltage (BV). However, the R_{SP} in conventional MOSFET (MOSFET) is limited by the 1D Silicon limit where the R_{SP} and the BV are oppositely affected by the doping concentration. In order to improve the tradeoff between R_{SP} and BV, the two-dimensional charge coupling method has been proposed [1]. There are two kinds of power MOSFET structures, one is the power Superjunction (SJ) MOSFET [2–4]. The SJ MOSFET can decrease the R_{SP}, however,

it is complicated to obtain high quality p-pillar and n-pillar in the production process. The second approach, called the resurf stepped oxide (RSO) U-shape MOSFET (UMOSFET), which use the electrode embedded within oxide coated deep trenches as a part of the drift region [5–10], but the input and gate transfer capacitances of this structure is relatively large. To solve this problem, the split-gate RSO (SGRSO) UMOSFET [11–20] has been proposed. However, some performances of SGRSO are less ideal than those of SJ MOS: when the BV is higher than 200 V, the phenomenon is more pronounced [21].

In recent years, several devices have been reported to improve the tradeoff between R_{SP} and BV on the same concept. For instance, the split-gate UMOSFET with the p-pillar [14], the double split-gate [16], linearly graded doping profile [22] or the slope side oxygen [23], etc. However, these new structures generally require extra specific process steps which means more costs and time. More seriously, some structures are difficult to achieve by controlling the process.

The split-gate resurf stepped oxide with high doped epitaxial layer (HDSGRSO) UMOSFET has been proposed. The epitaxial layer of HDGRSO UMOSFET has been divided into three parts: the upper epitaxial layer, the lower epitaxial layer and the middle epitaxial layer with higher doping concentration. The Technology Computer Aided Design (TCAD) simulation results show that the Reduced SURface Field (RESURF) active has been enhanced due to the high doped epitaxial layer, which can modulate the electric field distribution and reduce the internal high electric field. Therefore, the HDGRSO UMOSFET has a higher BV, a lower R_{SP} and a better FOM. Furthermore, there is no extra special process required in this advanced fabrication procedure, which is relatively cost-effective and achievable.

2. Device Structure and Mechanism

In order to achieve the desired charge-coupling, the split-gate electrode within the oxide coated trenches is designed to connect the source during operation in the blocking mode, as shown in Figure 1. The cross-sectional view of the HDSGRSO UMOSFET is presented in Figure 1b. Conventionally, the doping concentration of the n-drift is uniform. In this study, the epitaxial layer of HDGRSO UMOSFET has been divided into three parts with different doping concentration and thickness: the upper, the middle and lower epitaxial layers. The middle epitaxial layer has a higher doping concentration compared with the upper and lower epitaxial. In order to emphasize the modulation effect of the high doped epitaxial layer on the electric field, the doping concentrations of the upper and lower epitaxial layers are set to same, and the thickness of the high doped epitaxial layer is L_2.

In this work, we used the TCAD to compare the performance of two structures. The potential contours and the electric field distribution along the trench surface (cut2) and in the middle of Mesa active area (cut1) for two structures at V_{DS} = 240 V are represented as shown in the Figure 2. The doping concentration of the n-drift (N_D and N_2) was $1 \times 10^{15}/cm^{-3}$ and $5 \times 10^{15}/cm^{-3}$ for SGRSO and HDSGRSO UMOSFET, respectively, and the doping concentration of the high doped epitaxial layer was $1.5 \times 10^{16}/cm^{-3}$. It can be seen from the picture that the potential lines originally concentrated on the lower part moves to the upper part of the n-drift region, and the electric field of HDSGRSO UMOSFET distribution was more uniform than that of SGRSO UMOSFET. Furthermore, a small electric field peak appeared at the interface between the upper and the middle epitaxial layers, as shown in Figure 2, at −13.5 μm in the y-axis. Therefore, the high doped epitaxial layer can modulate the electric field distribution and reduce the internal high electric field to improve the BV.

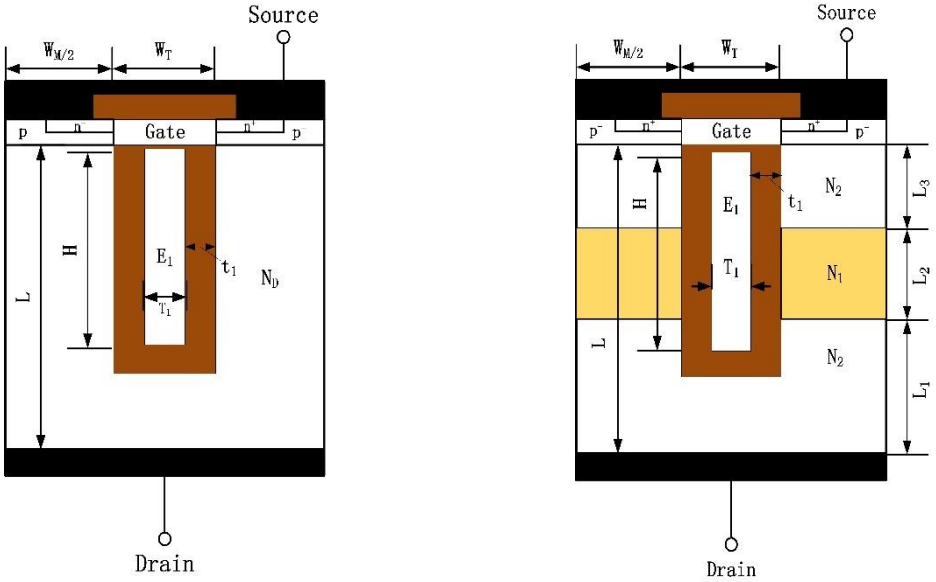

Figure 1. Cross section view of (**a**) split-gate resurf stepped oxide (SGRSO) and (**b**) split-gate resurf stepped oxide with high doped epitaxial layer (HDSGRSO) u-shape metal oxide semiconductor field effect transistor (UMOSFET).

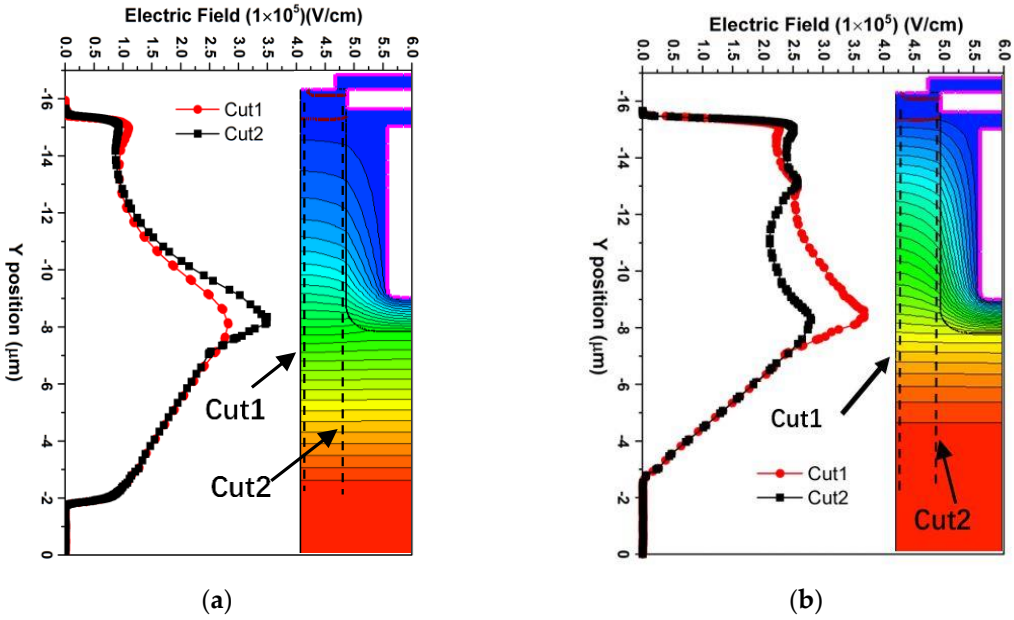

Figure 2. Potential distribution and electric field from cutlines comparing of the (**a**) SGRSO and (**b**) HDSGRSO UMOSFET at V_{DS} = 240 V.

Figure 3 shows the three-dimensional view of the electric field distributions for two structures with the same n-drift doping concentration (N_D and N_2) $5 \times 10^{15}/cm^{-3}$. The small electric field peak (at point A) brought by the high doped epitaxial layer is shown in the Figure 3b. It is obvious that the electric field in the drift region of HDSGRSO UMOSFET is more uniform than that of the SGRSO UMOSFET at the same n-drift doping concentration, and the volume under the electric field curved surface of HDSGRSO UMOSFET is bigger contrast to the SGRSO UMOSFET. As a result, the BV of HDSGRSO UMOSFET is 240 V, while that of SGRSO UMOSFET is 190 V.

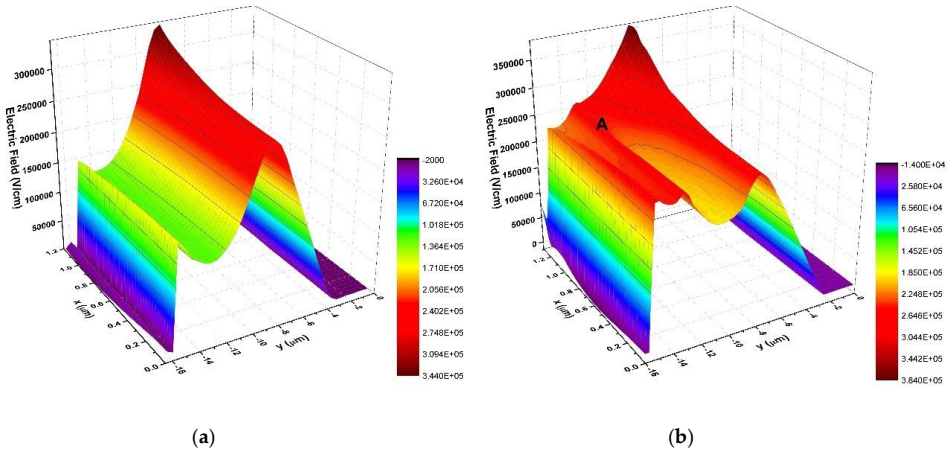

Figure 3. The three dimensions view of electric field distributions for the (**a**) SGRSO and (**b**) HDSGRSO UMOSFET with the same n-drift region doping concentration (N_D and N_2) 5×10^{15}/cm^{-3}.

3. Fabrication Procedure

Figure 4 exhibits the fabrication process and structure of the HDSGRSO UMOSFET. The fabrication process of epitaxial layer is the only difference compared to traditional processes. First, a 3.2 μm n-type epitaxial layer is formed on the N^+ substrate. Then, the middle and upper n-type epitaxial layer are formed on the first epitaxial in the same way. The doping concentration of the bottom and the upper epitaxial layers is the same, but the middle epitaxial layer has a higher doping concentration (a). Secondly, dry etching can be used to form the deep trench. An oxide layer is formed by thermally oxidized on the trench surface and then etched off to smooth the trench corner (b). Next, a 1.2 μm oxide is deposited to form the field oxide (c). Polysilicon is then deposited in the trench to form the source electrode which is surrounded by the field oxide (d). Afterwards, a thick oxide is deposited and etched back to separate the gate and the source electrode (e). Following, the gate oxide is formed by thermally oxidizing for 25 min under 1050 degrees dry oxygen conditions, and the polysilicon is deposited again to obtain the gate electrode (f). Subsequently, the p-body and n^+ source region are formed by implanted ions, respectively (g). Finally, a thick oxide is deposited on the gate surface to separate the gate and source metallic electrodes, and then the fabrication of the device is finished (h).

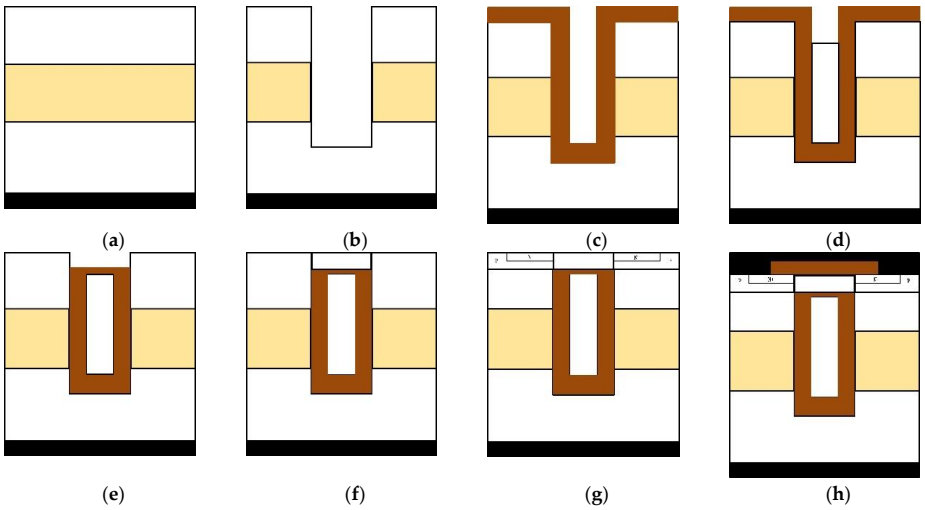

Figure 4. Fabrication procedure of the HDSGRSO UMOSFET.(**a**) Epitaxial layers are formed, (**b**) Trench is opened, (**c**) Thick oxide is deposited, (**d**) Polysilicon is deposited and etched back, (**e**) Thick oxide is deposited and etched back, (**f**) Gate oxide and gate poly are formed, (**g**) The p-body and n+ source region are formed, (**h**) Thick oxide and source metal are deposited.

4. Results and Discussion

Figure 5 shows the characteristics of the SGRSO and HDSGRSO UMOSFETs for same bias condition; the structural parameters adopted in the simulations are shown in the Table 1. The breakdown voltage for the two structures is shown in the Figure 5a, and the limit of drain current density is 1 μA/μm^2. It is obvious that the breakdown voltage of both is about 240 V. The relationship between the R_{SP} and gate voltage is shown in the Figure 5b for the two structures at V_{DS} = 0.3 V. It can be found that the R_{SP} of the HDSGRSO UMOSFET is much smaller than that of the SGRSO UMOSFET, and the gap between them increases with the increase of the gate voltage. The R_{SP} of the HDSGRSO UMOSFET can be reduced by 76%~79%, in contrast to the conventional structure at the same gate voltage.

Table 1. Structural parameters adopted in the simulations.

Parameter	Value
Trench depth (H_T)	7.5 μm
Gate depth(H_G)	1.0 μm
n^+ source junction depth	0.2 μm
p- body junction depth	0.8 μm
p- body doping concentration	1.5×10^{18} cm^{-3}
Trench width (W_T)	3.6 μm
Mesa Width (W_M)	3.2 μm
Width of E_1 (T_1)	1.6 μm
Thickness of field oxide (t_1)	1.2 μm
n-drift region doping concentration (N_D)	1×10^{15} cm^{-3}
Doping of lower epitaxial layer (N_2)	5×10^{15} cm^{-3}
Doping of middle epitaxial layer (N_1)	1.5×10^{16} cm^{-3}
Doping of upper epitaxial layer (N_2)	5×10^{15} cm^{-3}
Thickness of gate oxide	50 nm
Thickness of n^- drift region (L)	16 μm
Thickness of lower epitaxial layer (L_1)	3.2 μm
Thickness of middle epitaxial layer (L_2)	4 μm
Thickness of upper epitaxial layer (L_3)	8.8 μm
Height of source electrode of SGRSO (H)	6.3 μm

The drain I-V characteristics of the SGRSO and HDSGRSO UMOSFETs with same bias condition are shown in Figure 5c when the breakdown voltage is 240 V. It is obvious that the HDSGRSO UMOSFET has a relatively large current than that of SGRSO UMOSFET when the V_{GS} is 2 V, 5 V, 10 V and 15 V, respectively. Moreover, the current of the HDSGRSO UMOSFET when the V_{GS} is 5 V even exceeds the current of the SGRSO UMOSFET at 15 V especially. The transconductance of HDSGRSO and SGRSO UMOSFETs is shown in the Figure 5d. It is similar to the output characteristics of the two structures that the transconductance of HDSGRSO UMOS at the V_{GS} of 0.5 V is bigger than that of SGRSO UMOSFET when the V_{GS} is 1.5 V. The transconductance of HDSGRSO UMOSFET increases by approximately 178% contrast to the SGRSO UMOSFET, when the V_{GS} is 1.5 V.

An extensive analysis of the HDSGRSO UMOSFET has been given in contrast with SGRSO UMOSFET with the same structure parameters. The model of bandgap narrowing, concentration dependent mobility model, parallel electric field-dependent mobility model, Shockley-Read-Hall (SRH) model and impact-ionization model have been adopted in the simulation work [16].

Figure 6a shows the BV and FOM (BV^2/R_{SP}) at different doping concentrations of the n-drift region. Table 1 shows the parameters we adopted in the simulations. The BV of the two structures increases with the decreasing of the doping concentration of n-drift within the range of the 1×10^{15}/cm^{-3} -6×10^{15}/cm^{-3}. When the doping concentration of the drift region is 5×10^{15}/cm^{-3}, the FOM of HDSGRSO UMOSFET achieves the optimal value, which improved by 106% contrasted with the SGRSO UMOSFET, and the BV of HDSGRSO and SGRSO UMOSFETs were 239 V and 191 V respectively, which improved by 25.1%. It is worth noting that when the BV of the two structures was about 240 V, the FOM of HDSGRSO UMOSFET

improved by 402% in contrast to the SGRSO UMOSFET as the doping concentration of the drift region is $5 \times 10^{15}/cm^{-3}$ and $1 \times 10^{15}/cm^{-3}$ for HDSGRSO and SGRSO UMOSFETs. The BV and FOM (BV^2/R_{SP}) at different widths of the doped layer L_2 are shown in Figure 6b. It gets the optimal FOM and BV when the L_2 is 4 µm. The BV and FOM (BV^2/R_{SP}) at different thickness of the upper n-drift (L_3) is shown in Figure 6c when the L_2 is 4 µm. It achieves the highest FOM and BV when L_3 is 3.2 µm. Figure 6d shows the BV and FOM (BV^2/R_{SP}) at different doping concentrations of the high doped epitaxial layer when the n-drift region is $5 \times 10^{15}/cm^{-3}$. It is obvious the BV of the HDSGRSO UMOSFET is gradually increasing with the increase of the doping concentration of the high doped epitaxial layer. It gets optimal FOM and BV when the doping concentration of the high doped epitaxial layer is $1.5 \times 10^{16}/cm^{-3}$, because the modulation effect of the electric field in the n-drift gradually increases and reaches the optimal level with the increasing of the doping concentration of high doped epitaxial layer. However, when the doping concentration of the middle epitaxial layer is higher than $1.5 \times 10^{16}/cm^{-3}$, the charge balance in the n-drift will be broken and the BV will drop steeply.

Figure 7 shows the BV and FOM (BV^2/R_{SP}) at different thicknesses of the drift region. It indicates that there exists a saturated BV at a certain thickness. When the L is 14 µm, the FOM value and BV reaches the optimal value, respectively, and the BV is about 240 V. With the increase of epitaxial thickness, the R_{SP} gradually increases, resulting in the decrease of FOM. The L is 14 µm for HDSGRSO UMOSFET, whereas the L' is 16 µm for SGRSO UMOSFET when the BV is 240 V. Because of the enhancing of the electric field by high doped epitaxial layer, the breakdown occurs before the n-drift is depleted completely. Therefore, it can reduce the thickness of the epitaxial layer and R_{SP}. As a result, the FOM has been increased by 464% as compared with the SGRSO UMOSFET when the BV is about 240 V, according to the simulation results.

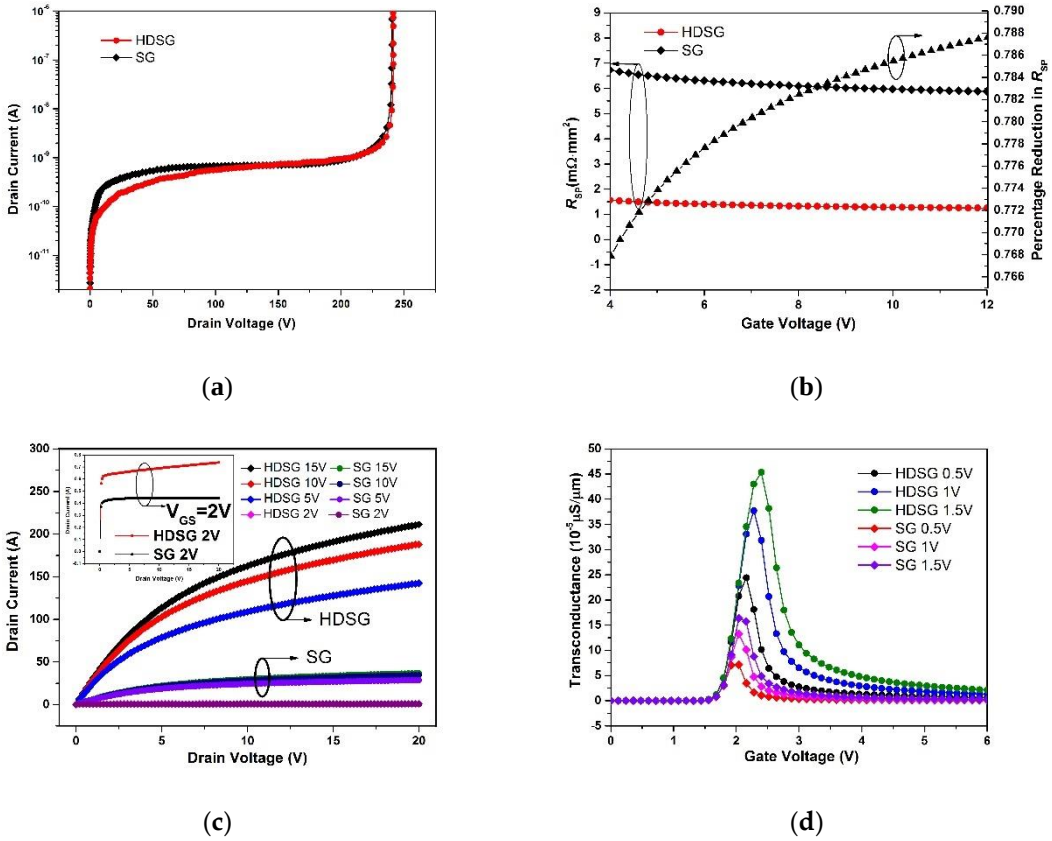

Figure 5. Drain I-V characteristics: (**a**) Breakdown Voltage (BV); (**b**) R_{SP} at different gate voltage with V_{DS} = 0.3 V and percentage reduction in R_{SP} as compared with the SGRSO UMOSFET; (**c**) output characteristics and (**d**) transconductance of two structures.

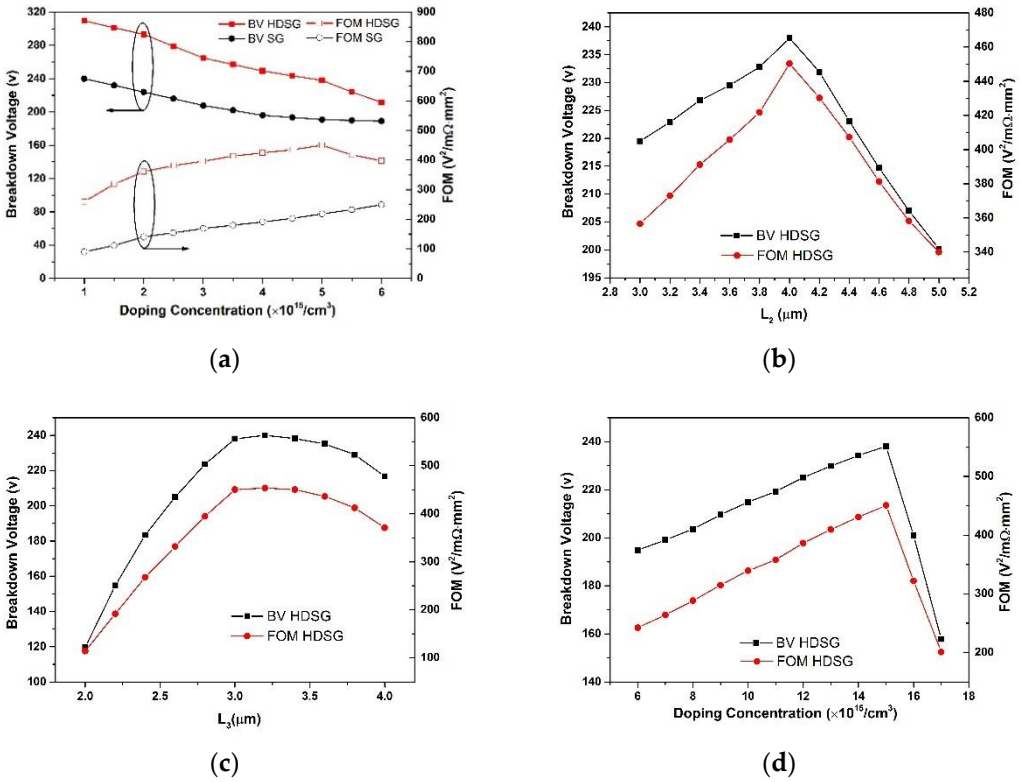

Figure 6. BV and FOM (BV^2/R_{SP}) at different (**a**) doping concentration of n-drift region; (**b**) L_2 (height of high doped epitaxial layer); (**c**) L_3 and (**d**) doping concentration of high doped epitaxial layer for HDSGRSO UMOSFET.

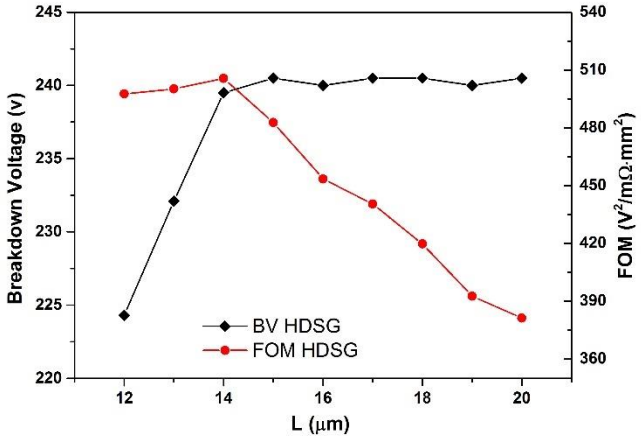

Figure 7. BV and FOM (BV^2/R_{SP}) of HDSGRSO UMOSFET at different n-drift region thickness.

For the power MOSFET used in the high frequency field, the switching losses is the most important part of the total power loss. The time period associated with the increase of the drain current and decrease of the drain voltage is determined by the charging of the device capacitances. The Figure 8a shows the input capacitances (C_{iss}) and reverse transfer capacitances (C_{rss}) of both structures when V_{GS} = 0 V and f = 1 MHz. The C_{rss} of the HDSGRSO UMOSFET has a slight increase in comparison with the ordinary structure because of the highly doped epitaxial layer. However, the capacitances difference between the two structures is gradually reduced as the drain voltage increases. When the drain voltage exceeds 120 V, the C_{rss} of the two structures are almost same. The C_{rss} of HDSGRSO and SGRSO UMOSFETs is 2 pF and 0.8 pF, respectively, at V_{DS} = 140 V. On the other hand, the doping concentration of the p-body is slightly reduced under the same boron dose due to the highly doped

epitaxial layer, which causes a slight reduction of the C_{iss} for HDSGRSO UNOSFET. It can be seen that the HDSGRSO UMOSFET has lower C_{iss} contrast to the SGRSO UNOSFET when the drain voltage increases from 0 to 140 V. The C_{iss} of HDSGRSO and SGRSO UMOSFETs is 1400 pF and 1490 pF, respectively, at V_{DS} = 140 V, which is of benefit to improve the switching speed of the HDSGRSO UMOSFET. The FOMs of $R_{SP} \times Q_{gd}$ have been adopted to compare the dynamic characteristics of two structures. The FOM ($R_{SP} \times Q_{gd}$) of HDSGRSO and SGRSO UMOSFETs is 180 and 250 mΩ·nC, as shown in the Figure 8b. The FOM of devices with high doped epitaxial layer structure was reduced by 27.9% in contrast to SGRSO UMOSFET because the introduction of the high doped epitaxial layer increases the doping concentration in the drift region, which makes the R_{SP} decrease greatly.

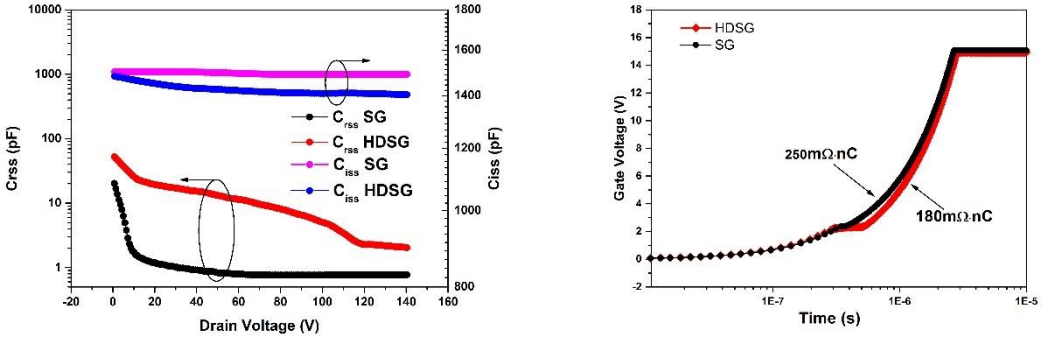

Figure 8. The *Crss* and *Ciss* (BV^2/R_{SP}) at different drain voltage (**a**) and (**b**) comparison of gate charge and $R_{SP} \times Q_{gd}$ for HDSGRSO and SGRSO UMOSFETs.

Table 2 shows the switching time and switching energy loss of two structures at 120 V, 4 A. The HDSGRSO UMSOFET has a lower turn-on delay time ($t_{d(on)}$) because of the smaller input capacitance, however, the rise time(t_r) of the HDSGRS UMOSFET is slightly higher due to the larger C_{rss}, which causes results in the turn-on loss (E_{on}) to be very close. On the other hand, the lager C_{rss} causes a certain increase of the turn-off delay ($t_{d(off)}$) time and fall time (t_f), which leads to an increase of turn-off loss (E_{off}) in contrast to the SGRSO UMOSFET, and this needs more research in the future. The performance of the HDSGRSO UMOSFET has been compared with the one-dimensional silicon limit and other works in Figure 9. The HDSGRSO UMOSFET has the lowest R_{SP} and the highest BV compared with the previous power UMOSFETs.

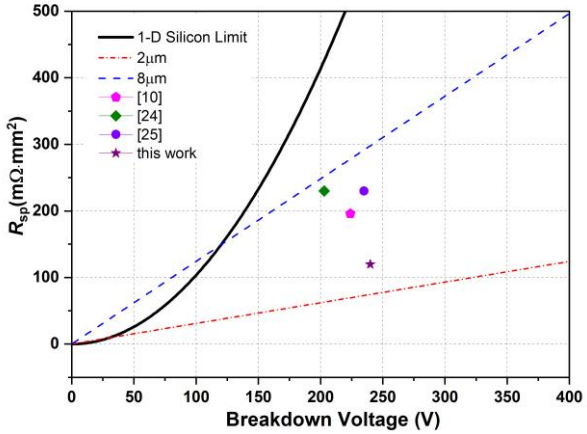

Figure 9. Performance comparing of one-dimensional silicon limit, two-dimensional charge-coupling limits for the pitches of 2 and 8 μm. Some references are [10,24,25] and this work.

Table 2. Switching time and switching energy loss of two structures.

	$t_{d(on)}$ (ns)	$t_{d(off)}$ (ns)	t_r (ns)	t_f (ns)	E_{on} (μJ)	E_{off} (μJ)
SGRSO	0.59	7.57	0.57	5.59	0.081	0.92
HDSGRSO	0.48	7.93	0.69	17.64	0.082	1.78

5. Conclusions

In this article, a split-gate resurf stepped oxide with high doped epitaxial layer (HDSGRSO) UMOSFET has been proposed. The epitaxial layer of HDGRSO UMOSFET has been divided into three parts: the upper epitaxial layer, the lower epitaxial layer and the middle epitaxial layer with higher doping concentration. The TCAD simulation results show that the RESURF active has been enhanced due to the high doped epitaxial layer, which can modulate the distribution of the electric field and reduce the internal high electric field. As a result, the BV of HDGRSO UMOSFET has been improved greatly. Meanwhile, the n-drift region has a higher doping concentration due to the high doped epitaxial layer, which can reduce the R_{SP} for a given BV. Therefore, the FOM of the device with high doped epitaxial can be improved significantly. According to the simulation results, the FOM (BV^2/R_{SP}) of HDSGRSO UMOSFET has been improved by 464%, and FOM ($R_{SP} \times Q_{gd}$) of HDSGRSO UMOSFET has been reduced by 27.9% compared to the conventional structure, respectively, when the BV is 240 V. Furthermore, the only difference between this procedure and the traditional procedure is the fabrication of the epitaxial layer, and no extra special process is required in this advanced fabrication procedure, which is relatively cost-effective and achievable.

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