Supplementary Materials: Prediction of a Two-Transistor Vertical QNOT Gate

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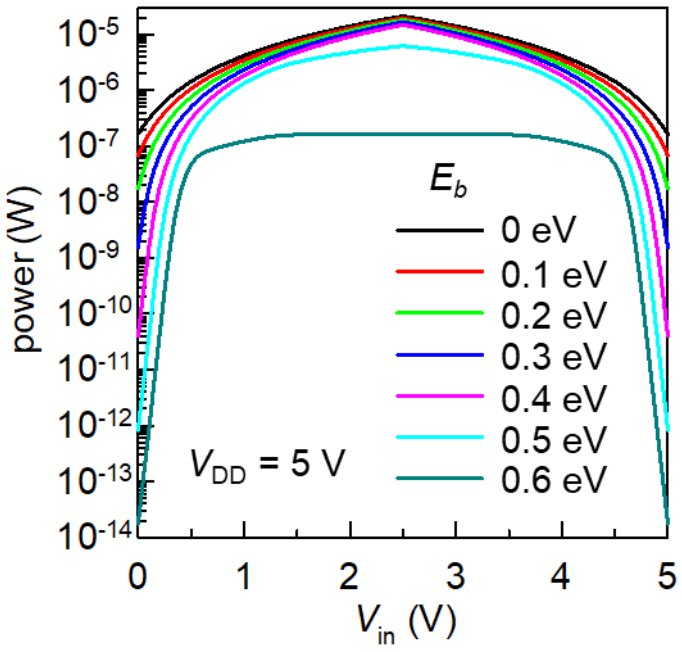

Figure S1. Power consumption.

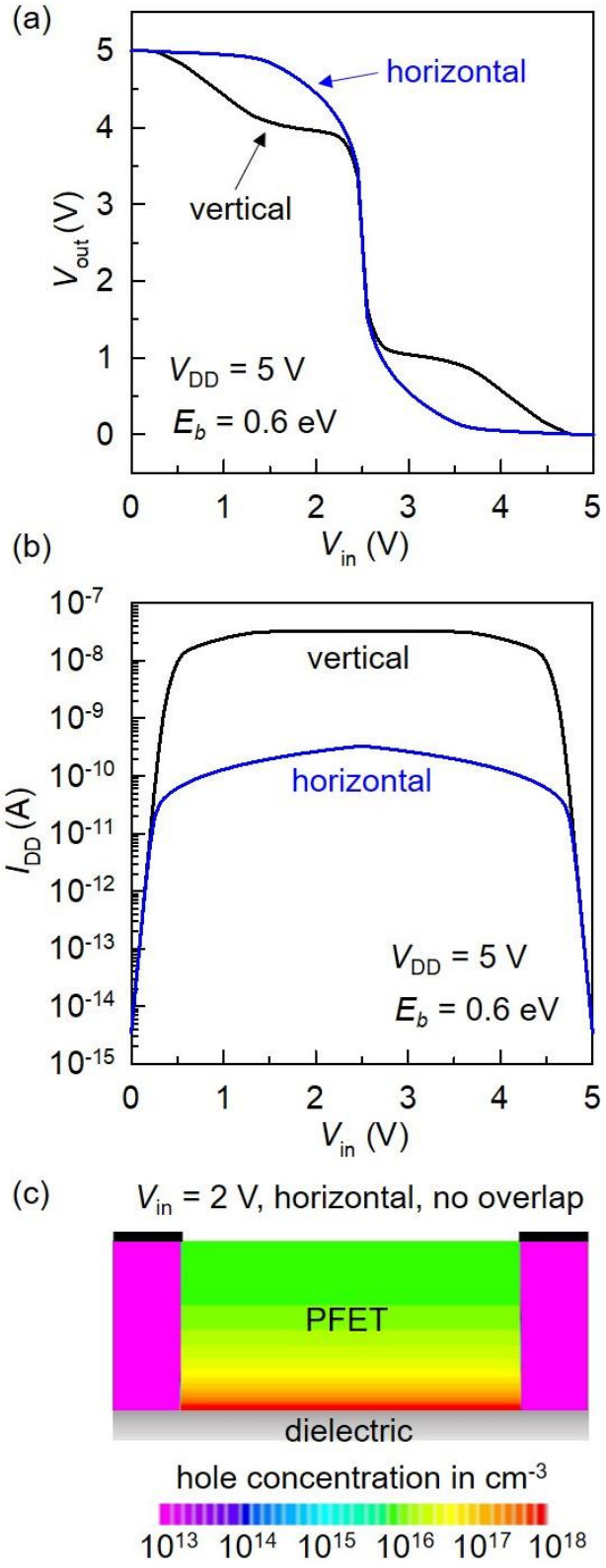

Figure S2. Vertical and horizontal inverter comparison: (**a**) VTC, (**b**) IDD comparison. (**c**) Hole concentration inside the PFET at Vin = 2 V (level "2") in the horizontal inverter.

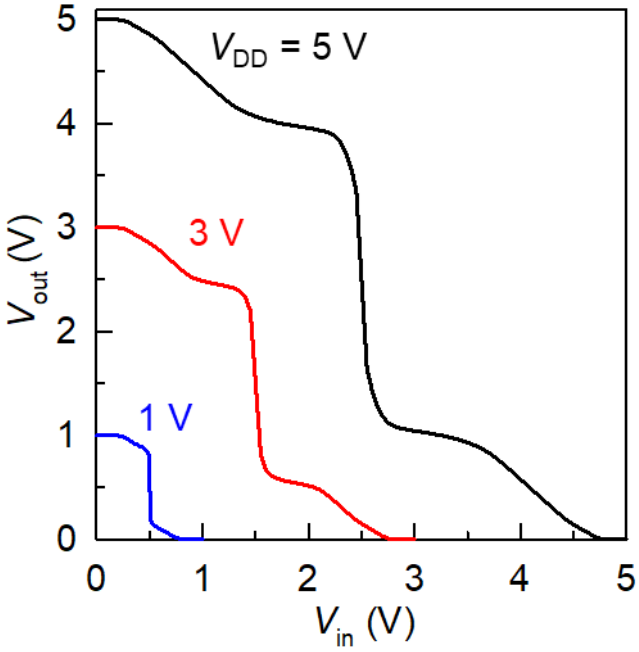

Figure S3. Scaling property.