Article

An Improved Investigation into the Effects of the Temperature-Dependent Parasitic Elements on the Losses of SiC MOSFETs

Yinong Zeng ¹, Yingping Yi ¹ and Pu Liu ^{2,*}

¹ Department of Electrical Engineering, University of Shanghai for Science and Technology, Shanghai 200082, China; yinongzeng@gmail.com (Y.Z.); yyp@usst.edu.cn (Y.Y.)

² College of Electrical and Information Engineering, Zhengzhou University of Light Industry, Zhengzhou 450011, China

* Correspondence: liupu1984@stu.xjtu.edu.cn

Received: 14 September 2020; Accepted: 12 October 2020; Published: 15 October 2020

Featured Application: The conclusion of this paper could serve as an important basis for the design guidelines of fast switching power converters.

Abstract: This paper presents an improved investigation into the effects of temperature-dependent parasitic elements on the silicon carbide (SiC) MOSFET power losses. Based on the physical knowledge of MOSFET, a circuit-level loss analytical model is proposed, which takes the parasitic elements of the power devices and the stray inductances of the Printed Circuit Board (PCB) traces into consideration. The state equations derived from the equivalent circuit of each stage is solved by iteration to calculate the loss in the switching transients. In order to study the temperature characteristic completely, the key parameters needed in the calculation are extracted from power device test platform based on Agilent B1505A. The loss assessment of the proposed analytical model with varied elements has been successfully substantiated by the experimental results of a 400-V, 15-A double-pulse-test bench. Finally, some practical knowledge about loss mechanisms is given to help estimate the power losses and optimize the efficiency of power converters.

Keywords: silicon carbide; MOSFET; parasitic elements; power losses

1. Introduction

In recent years, silicon carbide (SiC) has attracted extensive attention and has been gradually applied to power semiconductor devices due to its higher breakdown electric field, electron saturation velocity and thermal conductivity than conventional silicon (Si) materials [1–5]. In addition, increasing switching frequency has always been a common method to push up the power density and facilitate the miniaturization of switching converters by reducing the size of the passive components [6,7]. With a significant increase in switching speed, the effect of parasitic elements that mainly result from power semiconductor devices and PCB traces on switching performance can no longer be ignored and the losses become a crucial factor that determines the converter efficiency. Therefore, it is necessary to accurately calculate the loss of power devices and analyze the effects of the parasitic elements on it, helping designers to acquire in-depth knowledge of the switching loss mechanisms. There is considerable research in this filed. As discussed in [8], basically, investigation into loss can be classified into three categories. They are physical model, behavioral model, and analytical model (also called mathematical model).

Based on the knowledge of semiconductor physics and microelectronics, the physical model solves the characteristic expression of power devices by conducting the finite element analysis (FEA) [9–12].

The simulation results of physical model match the experimental results very well. However, this kind of model needs comprehensive parameters of the power device, such as gate oxide thickness, doping concentration in the channel, electron mobility, etc., which are difficult to obtain and the modeling process is rather complex and time-consuming, which is not suitable for circuit-level simulation.

The behavior model is widely used in the loss analysis because it has a good trade-off between the accuracy and simulation time. Based on the values obtained from parameter extraction (normally, device manufacturer provides these data or models on their website), the effect of parasitic elements including the junction capacitances of power devices and the stray inductances of the PCB traces on switching loss can be analyzed by circuit simulation software, e.g., PSpice or Saber, in which behavioral model of the MOSFET is used [13–15]. In [14], with specific modifications of the conventional Si power MOSFET model based on PSpice, an improved behavioral model is proposed for 10-kV SiC MOSFETs to validly predict switching loss. However, it cannot suffice to explain the switching loss mechanisms of the power device behind the simulation results.

The last method is the analytical model [16–24]. Generally, the switching loss expressions are derived from different equivalent circuits according to different stages on switching transients. The simplest and classical analytical model is the piecewise linear model, which is easier to obtain and solve than the aforementioned two model. However, there are many limitations in such a model; for example, ([16]) the analytical model only considers the gate resistance and the junction capacitances (the switching process is equivalent to the charging and discharging process of the RC circuit). In practice, especially in high-frequency operation, the effect of parasitic inductances cannot be totally ignored. Other analytical models that consider both junction capacitances and parasitic inductances have also been proposed. The effect of the parasitic elements on switching performance in low-voltage operation (the voltage lower than 40 V) has been extensively discussed in [17–20]. In low-voltage operation, the drain-source voltage may reach zero before the drain current reaches the steady-state value during the turn-on transients and the drain current may drop to zero before the drain-source voltage reaches bus voltage during the turn-off transients [19]. However, these particular cases will hardly happen to high-voltage MOSFETs. The analytical model of [21] considers the MOSFET–Snubber–Diode (MSD) configuration, whereas it treats the trans-conductance and the threshold voltage as a constant. In [23,24], the parasitic elements of the analytical model are extracted from the datasheet of the device vendor, but these models cannot reflect the temperature characteristics of the parasitic elements of the power devices. As a result, there are a lot of limitations in these analytical models.

For the sake of accuracy and computational efficiency, an improved analytical model that considers temperature-dependent parasitic elements of SiC MOSFET and the interaction between exterior parasitic inductances of PCB traces will be proposed. The paper is organized as follows: in Section 2, the basis of modeling is given. In Section 3, the turn-on and turn-off transients of the SiC MOSFET are divided into five stages, respectively, and then the state equations are derived from the equivalent circuits of each stages. In Section 4, a power device analysis platform is built to obtain the detailed temperature characteristics of the parasitic elements. In Section 5, the calculation results of this proposed analytical model will be verified by comparison with the experimental results of a 400-V, 15-A double-pulse test bench, then, the effects of the parasitic elements on loss will be comprehensive explained. Finally, a conclusion that can help engineer to design high-frequency power converters and minimize switching loss will be given in the Section 6.

2. The Basis of the Analytical Model

Figure 1 shows a simplified physical structure of Vertical Double-diffused MOSFET (VDMOSFET) considering the discrete package. There is an internal resistance due to the gate contact. The pad parasitic inductances and the internal bonding between the carbon silicon die and the package pads, which are relevant to the package technology, contribute to the total parasitic inductance in the power device. The only viable alternative to further lower the parasitic inductances is to concurrently address

the underlying package problem, using clip lead or sandwich package assembly methods to eliminate bond wires while maximizing the ratio of die area to package footprint [25]. As a unipolar device, the dynamic characteristics of SiC MOSFET are mainly determined by the charging and discharging process of the junction capacitances which are composed of oxide capacitances and depletion edge capacitances [26]. The width of depletion edge is related to the applied voltage between drain terminal and source terminal, so that the value of the junction capacitances is nonlinear. When a positive voltage applied between the gate terminal and source terminal, the depletion region gets wider towards the body, and it begins to drag the free electrons to the interface. As the density of the free holes of the body and the density of the free electrons of the interface becomes equal, the free electron layer is called the inversion layer (N channel).

Figure 1. Simplified physical view of a power MOSFET with the package.

Based on the above knowledge, the equivalent circuit of the MOSFET is obtained, as shown in Figure 2. The junction capacitances are represented by three nonlinear capacitances connected in parallel with each internal node. The parasitic inductances in series in each terminal of the device (the gate terminal also includes the internal resistance). The channel is the key element of modeling, which determines the accuracy of the model and should be carefully considered. The equivalent of the channel in the switching transients will be thoroughly discussed in the next section.

Figure 2. Equivalent circuit of MOSFET.

3. Analysis of the Switching Transients

The switching process of the MOSFET will be studied stage by stage in this section. A double-pulse test circuit is adopted for the modeling of MOSFET switching transients, as shown in Figure 3. The input is a constant voltage source V_{DD} and the load is a clamped-inductive load which can provide a constant

current I_{DD} . The gate signal V_{pulse} is assumed to flip between V_{SS} and V_{GG} with zero rise time and fall time in the analysis. In order to investigate the switching process better, two different external gate resistances R_{g_on} and R_{g_off} are used in the turn-on transients and turn-off transients, respectively. Similar to the MOSFET, the freewheeling diode is modeled by two parasitic inductances L_{c_1} and L_{a_1} and a parasitic resistance R_f in series with an ideal diode D_f , and then in parallel with a nonlinear junction capacitance C_f . In addition to these power devices, there also are a lot of stray inductances result from the PCB traces of the power loop, which are represented by L_{bus1} , L_{bus2} , L_{c_2} , L_{a_2} , L_{d_2} , L_{g_2} and L_{s_2} . In order to simplify the model and the equations, some parameters are merged in the equivalent circuit. $L_{d1} = L_{d_ext} + L_{d_int}$, $L_{g1} = L_{g_ext} + L_{g_int}$ and $L_{s1} = L_{s_ext} + L_{s_int}$ are denoted as the total parasitic inductances at each terminal of the MOSFET, respectively. It should be noted that the stray inductance of the ground lead of a measuring loop is hard to quantitatively analyze and its influence on the loss assessment can be ignored. Therefore, it was not considered in this model.

Figure 3. Analytical model of the double-pulse-test circuit considering parasitic elements.

3.1. Turn-On Switching Transients

Stage 1 $[t_0-t_1]$ turn-on delay time: Before the gate source voltage v_{gs} reaches the threshold voltage V_{th} , the SiC MOSFET power device is still in the cut-off region. At this stage, the value of the drain current i_d is assumed to be zero. According to Figure 4a and Kirchhoff's law, the following equations are obtained:

$$V_{GG} = R_{GG}i_g + L_g \frac{di_g}{dt} + v_{gs} + L_s \frac{di_s}{dt} \quad (1)$$

$$i_g = C_{gs} \frac{dv_{gs}}{dt} + C_{gd} \frac{dv_{gd}}{dt} \quad (2)$$

$$i_s = C_{gs} \frac{dv_{gs}}{dt} + C_{ds} \frac{dv_{ds}}{dt} \quad (3)$$

$$v_{gs} = v_{gd} + v_{ds} \quad (4)$$

$$i_g + i_d = i_s \quad (5)$$

where $R_{GG} = R_{g_on} + R_{g_int}$, $L_g = L_{g1} + L_{g2}$.

Figure 4. Equivalent circuits for the turn-on transients. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4 and Stage 5.

There are three independent state variables: the drain current i_d , the gate-source voltage v_{gs} and the drain-source voltage v_{ds} . The state equations derived from above equations are shown in Appendix A Equation (A1). As the power device is not activated, there is no switching loss P_{sw} during this period.

Stage 2 [t_1 – t_2] current rise time: When the gate source voltage v_{gs} goes beyond the threshold voltage V_{th} , the conductive pass (channel) enabling the current flow begins to form. Due to the fast speed of the SiC MOSFET power device, the drain current i_d surges, which generates the induced voltage across the parasitic inductances. This induced voltage deserves special attention, as it determines whether the drain current (i_d) will rise to its full value I_{DD} before or after the drain-source voltage v_{ds} drops to $v_{gs} - V_{th}$ (the boundary condition between the saturation region and the ohmic region of MOSFET). If the power device works in the saturation region, the channel of the SiC MOSFET can be equivalent to a voltage-controlled current source (the relationship between the channel current i_{ch} and gate-source voltage v_{gs} is governed by (6)), otherwise it can be equivalent to a nonlinear resistance which is related to the junction temperature T_j and the drain current i_d . Both of them are discussed as follows.

$$i_{ch} = g_f(v_{gs} - V_{th}) \quad (6)$$

where g_f is trans-conductance of the SiC MOSFET, which is also nonlinear.

Case I: The MOSFET works in the saturation region. In this situation, as shown in Figure 4b, the drain current i_d consists of three parts: the channel current i_{ch} and the current flowing through the junction capacitor C_{gd} and C_{ds} . The circuit equations can be expressed as:

$$V_{GG} = R_{GG}i_g + L_g \frac{di_g}{dt} + v_{gs} + L_s \left(\frac{di_d}{dt} + \frac{di_g}{dt} \right) \quad (7)$$

$$i_g = (C_{gs} + C_{gd}) \frac{dv_{gs}}{dt} - C_{gd} \frac{dv_{ds}}{dt} \quad (8)$$

$$v_{ds} = V_{DD} - v_f - L_p \frac{di_d}{dt} - L_s \frac{di_g}{dt} \quad (9)$$

$$i_d = g_f(v_{gs} - V_{th}) + C_{ds} \frac{dv_{ds}}{dt} - C_{gd} \frac{d(v_{gs} - v_{ds})}{dt} \quad (10)$$

$$v_f = R_f(i_d - I_{DD}) - V_f \quad (11)$$

where $L_p = L_{bus1} + L_{bus2} + L_c + L_a + L_d + L_s$, $L_c = L_{c1} + L_{c2}$, $L_a = L_{a1} + L_{a2}$, $L_d = L_{d1} + L_{d2}$, $L_s = L_{s1} + L_{s2}$.

Case II: The MOSFET works in ohmic region directly. As discussed above, the channel of MOSFET can be represented by a nonlinear resistance in this scenario. Therefore, (10) is changed to (12), and the rest remains unchanged.

$$i_d = \frac{v_{ds}}{R_{on}} + C_{ds} \frac{dv_{ds}}{dt} - C_{gd} \frac{d(v_{gs} - v_{ds})}{dt} \quad (12)$$

A new independent state variable i_d appears in this stage compared to the previous one, and the state equations derived from the above equations are shown in Appendix A Equation (A3). This stage ends when the drain current i_d reaches the bus current I_{DD} . The switching loss E_{sw} expression in this period is as follows.

$$E(I)_{sw_s2} = \int_{t_1}^{t_2} i_d v_{ds} dt \quad (13)$$

However, a more appropriate switching loss analysis is to replace (13) with (14), taking into account the assumption that the junction capacitances of MOSFET are only lossless energy buffers. The discrepancy between the two types of calculation methods will be further elucidated in Section 5 with the experimental verification.

$$E(II)_{sw_s2} = \int_{t_1}^{t_2} i_{ch} v_{ds} dt \quad (14)$$

Stage 3 [t2–t3] voltage falling time I: As the current is transferred to the SiC MOSFET, the SiC Schottky Diode (SBD) becomes capable of blocking the voltage; Figure 4c shows the equivalent circuit of this stage, and the drain-source voltage v_{ds} drops dramatically at the same time, if the *case I* occurs in the previous stage. The gate-source voltage v_{gs} is maintained at the Miller Plateau, because the gate current i_g is completely absorbed by the drain-source capacitance C_{ds} without flowing to the gate-source capacitance C_{gs} . Although SBD features zero reverse recovery current, the drain current i_d continues to increase since the charging current of junction capacitance C_f of the SiC SBD. Therefore, (11) is replaced by (15), and the rest remains unchanged. A resonant period begins in this moment, which induced by the oscillations between L_p and C_f . This stage ends when drain-source voltage v_{ds} decreases to $v_{gs} - V_{th}$.

$$\frac{dv_f}{dt} = \frac{i_d - I_{DD}}{C_f} \quad (15)$$

There are five independent state variables: the drain current i_g , the drain current i_d , the gate-source voltage v_{gs} , the drain-source voltage v_{ds} and the free freewheeling diode voltage v_f . The state equations at this stage are shown in Appendix A Equation (A4).

During this period, the two type of switching loss calculation as following:

$$E(I)_{sw_s3} = \int_{t_2}^{t_3} i_d v_{ds} dt \quad (16)$$

$$E(II)_{sw_s3} = \int_{t_2}^{t_3} i_{ch} v_{ds} dt \quad (17)$$

Stage 4 [t3–t4] voltage falling time II: When the drain-source voltage v_{ds} decreases to $v_{gs} - V_{th}$, the SiC MOSFET will come out of the saturation region and get into the ohmic region. As shown in Figure 4d, the channel is equivalent to a nonlinear resistance (also called on-state resistance) in this stage. Therefore, (10) is replaced by (18). The gate-source voltage v_{gs} breaks out of the Miller Plateau and begins to increase again. The drain-source voltage v_{ds} drops slightly in this period, and the drain current i_d drops back to I_{DD} simultaneously. The oscillations in the power loop will be damped by the stray resistance resulting from the PCB traces. In order to specify this point, a lumped resistance R_{stray} is added in the equivalent circuit, as same as the stray inductances, to compensate for the active power consumption and (9) should be replaced by (19). Once the drain-source voltage v_{ds} decreases to $i_d \cdot R_{on}$, this stage ends and the channel can be seen as completely conductive.

$$i_d = \frac{v_{ds}}{R_{on}} + C_{ds} \frac{dv_{ds}}{dt} - C_{gd} \frac{d(v_{gs} - v_{ds})}{dt} \quad (18)$$

$$v_{ds} = V_{DD} - v_f - R_{stray} i_d - L_p \frac{di_d}{dt} - L_s \frac{di_g}{dt} \quad (19)$$

The independent state variables at this stage remain unchanged and the state equations are shown in Appendix A Equation (A5). The switching loss in this period can be calculated as:

$$E(I)_{sw_s4} = \int_{t_3}^{t_4} i_d v_{ds} dt \quad (20)$$

$$E(II)_{sw_s4} = \int_{t_3}^{t_4} i_{ch} v_{ds} dt \quad (21)$$

Stage 5 [t4–t5] On-State Operation: The gate current i_g still continues to charge the gate-source capacitance C_{gs} until the gate-source voltage v_{gs} reaches the positive drive voltage V_{GG} . The state equations and the equivalent circuit are the same as the previous stage, while the loss at this stage is considered as conduction loss E_{cond} and can be calculated as:

$$E_{cond1} = \int_{t_4}^{t_5} i_d^2 R_{on} dt \quad (22)$$

3.2. Turn-Off Switching Transients

It is known that the turn-off switching transients are a reversely symmetrical process of the turn-on switching transients, in which the channel can also be equivalent to a nonlinear resistance, voltage-controlled current source, or an open circuit. Therefore, some repeated equations are omitted in the derivation of the stage equations for the turn-off switching transients.

Stage 6 [t6–t7] Turn-Off Delay Time: Before the gate source voltage v_{gs} reduces to the Miller Voltage V_{miller} , which is governed by (23), the SiC MOSFET power device operates in the ohmic region. It is assumed that the drain current i_d remains unchanged ($i_d = I_{DD}$) at this stage. As shown in Figure 5a,

the gate-source capacitance and the gate-drain capacitance are being discharged through R_g and L_s . The circuit equations are shown from (24) to (26):

$$V_{mil} = \frac{I_o}{g_f} + V_{th} \quad (23)$$

$$V_{SS} = R_{SS}i_g + L_g \frac{di_g}{dt} + v_{gs} + L_s \left(\frac{di_d}{dt} + \frac{di_g}{dt} \right) \quad (24)$$

$$i_g = (C_{gs} + C_{gd}) \frac{dv_{gs}}{dt} - C_{gd} \frac{dv_{ds}}{dt} \quad (25)$$

$$i_s = \frac{v_{ds}}{R_{on}} + C_{gs} \frac{dv_{gs}}{dt} + C_{ds} \frac{dv_{ds}}{dt} \quad (26)$$

where $R_{SS} = R_{g_off} + R_{g_int}$.

Figure 5. Equivalent circuits for the turn-off transients. (a) Stage 6 and Stage 7. (b) Stage 8. (c) Stage 9. (d) Stage 10.

As with the stage 1, there are three independent state variables: the drain current i_d , the gate-source voltage v_{gs} and the drain-source voltage v_{ds} , and the state equations derived from the above equations

are shown in Appendix A Equation (A6). Since the device is still activated, the loss during this period is conduction loss E_{cond} , which can be calculated as:

$$E_{cond2} = \int_{t_5}^{t_6} i_d^2 R_{on} dt \quad (27)$$

Stage 7 [t7–t8] Voltage Rising Time I: During this stage, the power device still works in the ohmic region until the drain-source voltage v_{ds} reaches $v_{gs} - V_{th}$. Therefore, the drain current i_d stays constant at I_{DD} and the gate-source voltage v_{gs} (almost) remains at the Miller voltage. The equivalent circuit and equations during this period are the same as the previous one, while the loss during this period is regarded as the switching loss E_{sw} and can be calculated as:

$$E(I)_{sw_s7} = \int_{t_6}^{t_7} i_d v_{ds} dt \quad (28)$$

$$E(II)_{sw_s7} = \int_{t_6}^{t_7} i_{ch} v_{ds} dt \quad (29)$$

Stage 8 [t8–t9] Voltage Rising Time II: When the drain-source voltage v_{ds} reaches $v_{gs} - V_{th}$, the device begins to operate in saturation region. Therefore, the channel is equivalent to a voltage-controlled current source, as shown in Figure 5b. The drain-source voltage v_{ds} continues to increase until the forward voltage v_f of the SBD decreases to the forward voltage $-V_f$. The voltage slew rate will be faster than in the previous stage, since the value of junction capacitance significantly decreases with the increase in drain-source voltage v_{ds} . A part of I_{DD} will be flowing through the freewheeling diode to discharge the C_f , which will be causing the drain current i_d drop. During this period, the channel current i_{ch} is also governed by (6). Hence the drain current i_d expression is changed to (10) and the rest of the circuit equations are the same as the stage 4 and the state equations are shown in Appendix A Equation (A8). During this period, the switching loss E_{sw} is given by (30) and (31).

$$E(I)_{sw_s8} = \int_{t_7}^{t_8} i_d v_{ds} dt \quad (30)$$

$$E(II)_{sw_s8} = \int_{t_7}^{t_8} i_{ch} v_{ds} dt \quad (31)$$

Stage 9 [t9–t10] Current Falling Time: When the freewheeling diode ceases to block the voltage, the current begins to divert from the MOSFET to the freewheeling diode rapidly, which will induce a voltage drop across the parasitic inductances and simultaneously incur a voltage overshoot on the drain-source voltage v_{ds} . Compare to the previous stage, the expression of the freewheeling diode voltage is replaced by (11) and the rest of circuit equations remain unchanged. This stage ends when the gate-source voltage v_{gs} decreases to V_{th} . The equivalent circuit is shown in Figure 5c.

$$E(I)_{sw_s9} = \int_{t_8}^{t_9} i_d v_{ds} dt \quad (32)$$

$$E(II)_{sw_s9} = \int_{t_8}^{t_9} i_{ch} v_{ds} dt \quad (33)$$

Stage 10 [t10–t11] Off-State Operation: After the gate-source voltage v_{gs} decreases to V_{th} , the device works in the cut-off region. For a similar reason, a lumped resistance is added in the circuit (shown in Figure 5d). This stage ends, when the gate-source voltage v_{gs} decreases to the negative drive voltage V_{SS} . The state equations are shown in Appendix A Equation (A9) Since the channel is inactive, there is

no power loss during this period. As discussed above, the power loss during the switching transient can be categorized and summarized as (34) to (37).

$$E(I/II)_{sw_on} = \sum_{i=2}^4 E(I/II)_{sw_si} \quad (34)$$

$$E(I/II)_{sw_off} = \sum_{i=7}^9 E(I/II)_{sw_si} \quad (35)$$

$$E_{cond} = E_{cond1} + E_{cond2} \quad (36)$$

$$E(I/II)_{total} = E(I/II)_{sw_on} + E(I/II)_{sw_off} + E_{cond} \quad (37)$$

4. Experimental Setup

Based on the proposed analytical model, except for the operating condition V_{DD} , I_{DD} , V_{GG} , and V_{SS} , the parameters needed in the calculation are the junction capacitances C_{gs} , C_{gd} , C_{gs} and C_f , the stray inductances of the PCB traces L_{bus} , L_{line} , the parasitic inductances of the terminal L_g , L_d , L_s , L_a and L_c , and the static characteristic of power devices: the trans-conductance g_f , the internal resistance R_{g_int} and R_f , the threshold voltage V_{th} , the forward voltage V_f , and on-state resistance R_{on} . Apart from the junction capacitances and the parasitic, stray inductances, all the other parameters are temperature dependent. Therefore, it is necessary to build a test platform for the measurement. The approaches to obtain these parameters can be divided into three categories.

4.1. Static Characteristic Test Platform

According to the standards of IEC 60747-8 [27] and datasheet of the device vendor [28,29], the static characteristic test platform based on Power Device Analyzer Curve Tracer (PDACT) Agilent B1505A with the heating plate was established to measure the static characteristic of SiC MOSFET C2M0025120D (Cree, 1200 V, 90 A) and SiC SBD C4D20120A (Cree, 1200 V, 90 A), as shown in Figure 6. Considering the materials and components that make up the package are not compatible with high temperature (usually lower than 175 °C) [30], the testing temperature ranges from 25 to 150 °C. It should be noted that the case temperature T_c obtained by infrared thermal camera is used to approximate the junction temperature T_j , since the latter is difficult to measure by conventional methods. The specific settings of each module are shown in Table 1.

Figure 6. Static characteristic test platform for power device.

Table 1. Preliminary setting of the state characteristic testing.

Static Characteristic	Part Number	Parameter	Gate-Source Voltage/Step	Applied Voltage/Step	Temperature/Step
Transfer characteristic	B1510A and B1512A	g_f	0 to 12 V/0.25 V	20 V (fixed)	25 to 150 °C/25 °C
Output characteristic		R_{on}	10 to 20 V/2 V	0 to 10 V/2 V	
Threshold voltage		V_{th}, V_f	0 to 5 V/0.1 V	10 V, $I_d = 15$ mA (fixed)	25 to 145 °C/10 °C
Junction capacitance	B1520A	$C_{iss}, C_{oss}, C_{iss}, C_f$	Sweep signal VAC = 25 mV, f = 1 MHz	Applied voltage 0 to 1000 V	Temperature/step 25 to 150 °C/25 °C

4.2. ANSYS Q3D Extractor

A common approach to measure the value of the stray inductance is computational electromagnetics [31], which relies on finite-element analysis (FEA) simulation (e.g., ANSYS Q3D Extractor) to solve Maxwell's equations through the PCB layout and component material information. The stray resistance and stray inductance, including both self-inductance and mutual-inductance, can be accurately extracted through this approach. However, in order to simplify the calculation, the mutual inductances are neglected in this analytical model.

4.3. Vector Network Analyzer

The parasitic inductance is mainly determined by the devices package. However, the above approach suffers from being time-consuming and having poor convergence, since the physical structure of a package is complex. There is a more practical approach which is based on Impedance Analyzer or Vector Network Analyzer (VNA) [32]. By calibrating the test system using a mathematical technique called vector error correction, VNA provides high measurement accuracy [33]. The power device is performed over a frequency range of 100 kHz to 200 MHz by Keysight VNA (E5061B). Since the MOSFET under zero applied voltage is equivalent to a second-order RLC circuit, as shown in Figure 7, it has a self-resonant frequency (SRF). The parasitic inductances and internal resistances can be calculated through its SRF [34]. The testing temperature also ranges from 25 to 150 °C.

Figure 7. Equivalent circuit of MOSFET under zero applied voltage.

5. Results

5.1. Experimental Results

The static characteristic parameters obtained from the above methods are shown in Figure 8e (the black scatter plot). All of these measured scatters require nonlinear fitting before they can be used for calculation. The extraction results of the stray inductances of PCB traces and the parasitic inductances of power device terminals are shown in Table 2, respectively. Due to the maximum difference of less than 5%, the parasitic inductances are treated as a constant (the average) in the later calculation. The internal resistance R_{g_int} and R_f obtained through VNA measuring are shown in

Figure 8f while the others, such as R_{s_int} and R_{d_int} , are ignored in the proposed model since their values are very small.

Figure 8. Measured scatters and fitted curve of the key parameters. (a) Trans-conductance g_f , (b) on-state resistance R_{on} , (c) threshold voltage v_{th} and forward voltage v_f , (d) junction capacitance of silicon carbide (SiC) Schottky diode (SBD) C_f , (e) output capacitance C_{oss} and reverse transfer capacitance C_{rss} , (f) internal resistance R_{g-int} and R_f .

Table 2. Extraction results of the stray and parasitic inductances.

	Parameter	L_{bus1}	L_{bus2}	L_{c2}	L_{a2}	L_{g2}	L_{d2}	L_{s2}	R_{stray}
Q3D	Value (nH)	51.24	72.85	4.25	4.12	6.39	12.08	1.71	1.85 Ω
	Package	TO-247-3				TO-220-2			
	Parameter	L_{g1} (nH)	L_{d1} (nH)	L_{s1} (nH)		$L_{a1} + L_{c1}$ (nH)			
VNA	Maximum	9.57 (@ 50 °C)	4.71 (@ 25 °C)	8.39 (@ 50 °C)		10.12 (@ 25 °C)			
	Minimum	9.13 (@ 75 °C)	4.54 (@ 125 °C)	8.06 (@ 150 °C)		9.79 (@ 100 °C)			
	Difference	4.77%	3.79%	4.21%		3.34%			
	Average	9.218	4.623	8.176		9.889			

5.2. Fitting to the Key Parameters

For the sake of a trade-off between the precision and simplicity, the polynomial fitting is adopted to fit the static characteristic curve of the SiC MOSFET C2M0025120D. An appropriate polynomial order is chosen to ensure the *R-squared* (coefficient of determination, a goodness of fit) higher than 0.995. The trans-conductance g_f and on-state resistance R_{on} can be regarded as a two-variable function

of V_{gs} and T_j and function of i_d and T_j , respectively. The fitting equations are given in (38) and (39), the fitted curves are shown in the Figure 8a,b.

$$g_f(v_{gs}, T_j) = p_{00} + p_{10}v_{gs} + p_{01}T_j + p_{20}v_{gs}^2 + p_{11}v_{gs}T_j + p_{02}T_j^2 + p_{30}v_{gs}^3 + p_{21}v_{gs}^2T_j + p_{12}i_dT_j^2 + p_{03}T_d^3 + p_{40}v_{gs}^4 + p_{31}v_{gs}^3T_j + p_{22}v_{gs}^2T_j^2 + p_{13}v_{gs}T_j^3 + p_{04}T_j^4 \quad (38)$$

where $p_{00} = -1.313$, $p_{10} = 2.74$, $p_{01} = 2.292 \times 10^{-4}$, $p_{20} = -1.287$, $p_{11} = -3.362 \times 10^{-2}$, $p_{02} = -9.872 \times 10^{-5}$, $p_{30} = -0.2086$, $p_{21} = 9.167 \times 10^{-3}$, $p_{12} = 9.789 \times 10^{-5}$, $p_{03} = 6.437 \times 10^{-8}$, $p_{40} = -8.4 \times 10^{-3}$, $p_{31} = -5.352 \times 10^{-4}$, $p_{22} = -1.034 \times 10^{-5}$, $p_{13} = -8.058 \times 10^{-8}$, $p_{04} = 2.109 \times 10^{-10}$.

$$R_{on}(i_d, T_j) = p_{00} + p_{10}i_d + p_{01}T_j + p_{20}i_d^2 + p_{11}i_dT_j + p_{02}T_j^2 + p_{30}i_d^3 + p_{21}i_d^2T_j + p_{12}i_dT_j^2 + p_{03}T_d^3 + p_{40}i_d^4 + p_{31}i_d^3T_j + p_{22}i_d^2T_j^2 + p_{13}i_dT_j^3 + p_{04}T_j^4 \quad (39)$$

where $p_{00} = 30.71$, $p_{10} = 0.03$, $p_{01} = -0.1388$, $p_{20} = 3.705 \times 10^{-4}$, $p_{11} = -2.019 \times 10^{-4}$, $p_{02} = 4.309 \times 10^{-3}$, $p_{30} = -1.091 \times 10^{-8}$, $p_{21} = -1.725 \times 10^{-6}$, $p_{12} = 2.894 \times 10^{-6}$, $p_{03} = -2.642 \times 10^{-5}$, $p_{40} = 6.933 \times 10^{-9}$, $p_{31} = -2.448 \times 10^{-9}$, $p_{22} = 2.817 \times 10^{-9}$, $p_{13} = -6.658 \times 10^{-9}$, $p_{04} = 6.943 \times 10^{-8}$.

The threshold voltage V_{th} , the forward voltage V_f , the gate internal resistance R_{g_int} and the freewheeling resistance R_f can be regarded as a single-variable function of the junction temperature T_j . The fitting equations are given from (40) to (43) and the fitted curves are shown from Figure 8c–f.

$$V_{th}(T_j) = 1.064 \times 10^{-5}T_j^2 - 0.006629T_j + 2.779 \quad (40)$$

$$V_f(T_j) = -0.001509T_j + 1.012 \quad (41)$$

$$R_{g_int}(T_j) = p_1T_j^3 + p_2T_j^2 + p_3T_j + p_4 \quad (42)$$

where $p_1 = 6.104 \times 10^{-8}$, $p_2 = 7.835 \times 10^{-6}$, $p_3 = -4.974 \times 10^{-3}$, $p_4 = 1.524$.

$$R_f(T_j) = 0.271T_j + 22.52 \quad (43)$$

Nevertheless, polynomial does not perform well in the junction capacitance versus the applied voltage curve fitting. According to [35,36], the input capacitance C_{iss} was treated as two discrete values and (44) is adopted to characterize the nonlinearity of the output capacitance C_{oss} and the reverse transfer capacitance C_{rss} (see Table 3). The transform relationship between C_{iss} , C_{rss} , C_{oss} and C_{gs} , C_{gd} , C_{ds} is shown in (45).

$$C = \frac{C_0}{(1 + \frac{v}{a})^b} \quad (44)$$

where v is the applied voltage, C_0 is the capacitance value under $v = 0$ V, a and b are two adjustment parameters extracted from the capacitance versus voltage curve.

$$\begin{cases} C_{iss} = C_{gs} + C_{gd} \\ C_{rss} = C_{gd} \\ C_{oss} = C_{gd} + C_{ds} \end{cases} \quad (45)$$

Table 3. Specification of nonlinear junction capacitances.

	0 V < v ≤ 10 V	10 V < v ≤ 400 V
C_f (pF)	$\frac{1500}{(1 + \frac{v_{ca}}{1.412})^{0.5047}}$	$\frac{1500}{(1 + \frac{v_{ca}}{1.387})^{0.5007}}$
C_{iss} (pF)	4000	3300
C_{oss} (pF)	$\frac{3850}{(1 + \frac{v_{ds}}{2.394})^{0.5895}}$	$\frac{3850}{(1 + \frac{v_{ds}}{1.154})^{0.4654}}$
C_{rss} (pF)	$\frac{1430}{(1 + \frac{v_{ds}}{1.041})^{0.774}}$	$\frac{1430}{(1 + \frac{v_{ds}}{0.03})^{0.4964}}$

5.3. Loss Assessment

Based on the discussion above, the flowchart in Figure 9 presents the calculation routine for applying the model. Compared with traditional method, the iterative method is adopted to solve the state equations, from which the numerical solution can be derived without simplification [37]. Therefore, the calculation accuracy is improved. As mentioned in the previous section, there are two switching loss calculation methods in this model. In turn-on transients, the calculation I will be less than calculation II, since the discharging current of C_{ds} and C_{gd} , which opposes the trend of the drain current is included in i_d . However, the turn-off loss of calculation I will be greater than calculation I due to the charging current of C_{ds} and C_{gd} . As a result, the two types of calculation would not vary the E_{total} but would instead vary the distribution of power losses between E_{sw_on} and E_{sw_off} .

Figure 9. Flowchart for loss assessment.

The experimental prototype of a 400-V, 15-A double-pulse-test setup is shown in Figure 10, in which the chip inductors are added to simulate the varied stray inductances.

Figure 10. Double-pulse-test setup with varied elements. (a) Top view. (b) Bottom view.

As stated in [38], the measurement system bandwidth should be higher than ten times the highest equivalent frequency of the measured signal, which can be approximated by

$$f = \frac{0.25}{\min(t_r, t_f)} \quad (46)$$

where t_r is the rise time, t_f is the fall time.

The typical rise/fall time of C2M0025120D is 32/28 ns. According to (46), the equivalent frequency is 8.9 MHz. The measurement system specified in Table 4 can meet the bandwidth requirement. It must be pointed out that for the sake of emulating the switching waveforms taken in the experiment, the induced voltage drops across the parasitic inductances of the package terminal; L_{s1} and L_{d1} have to be included in the analytical waveforms for v_{ds} , as they are intrinsic and inside the package.

Table 4. Specification of the measurement system.

Part No.	Description	Bandwidth	Measured Signal
RTH1004	Oscilloscope	500 MHz	
RT-ZI10	Passive probe	500 MHz	v_{ds}
TPP0201	Passive probe	200 MHz	v_{gs}
TCP0030A	Current probe	120 MHz	i_d

As shown in Figure 11, the switching waveforms of the proposed analytical model match the experiment well. Voltage and current overshoot are also important factors in the application of the power device, which should be considered together with the power losses. The quantitative comparison of loss and voltage and current overshoot is listed in Table 5. The maximum error is 7.13%, which proves the good accuracy of the model. The variation patterns of power losses with each parameter element can be worked out by the calculation, as shown in Figure 8, to present a further investigation into the loss mechanism and they will be demonstrated experimentally. The $\pm 10\%$ error bars of the experimental results are added to illustrate the accuracy. It can be seen that the calculation results are in good accordance with the experiment.

Figure 11. Comparison of switching waveforms between experiment and analytical model. (a) Turn-on switching waveform. (b) Turn-off switching waveform.

Table 5. Quantitative comparison of loss, voltage and current overshoot.

	Experiment	Calculation I	Error
$E_{sw-on}(\mu J)$	119.06	121.05	1.67%
$E_{sw-off}(\mu J)$	66.27	67.51	1.87%
$E_{cond}(\mu J)$	3.71	3.45	7.01%
$V_{os}(V)$	111.65	119.61	7.13%
$I_{os}(A)$	6.22	6.45	3.70%

$$* \text{Error} = \left| \frac{\text{Calculated value} - \text{Experimental value}}{\text{Experimental value}} \right| \times 100\%$$

Junction Temperature: In Figure 8, it can be seen that most of the key parameters are temperature-dependent. As a result, the temperature will affect the switching performances of SiC MOSFET obviously. The comparison of power losses between experiment and calculation with varied junction temperature T_j are illustrated in Figure 12a. It is easy to see that the increase in T_j reduces the turn-on loss and increases the turn-off loss contrarily. The conduction loss increases slightly, since the on-state resistance R_{on} is positively correlated with T_j . As a result, the total loss does not exhibit great variation at different T_j . In the turn-off transients, with the increased trans-conductance g_f affected by the rising junction temperature T_j , the Miller voltage will decrease consequently, which leads to a reduction in the current slew rate. Hence, the voltage overshoot decreases with the increase in T_j , as shown in Figure 12b.

Figure 12. Comparison between experiment and calculation under the influence of junction temperature T_j . (a) Power losses. (b) Voltage overshoot and current overshoot.

Gate Driver Resistance: Figure 13a presents the power losses with varied R_g . It shows that the switching loss (both turn-on and turn-off) exhibit distinctive increases with the increase in R_g , which is due to the slower switching speed resulting from larger R_g . For the same reason, the voltage and current overshoot will all decrease (see Figure 13b). It is necessary for designers to make a trade-off between switching speed and switching loss. The double-gate-resistances is a useful solution; a proper turn-on resistance to ensure the switching speed and a low turn-off resistance to discharge the C_{gs} fast.

Figure 13. Comparison between experiment and calculation under the influence of external driver resistance R_g . (a) Power losses. (b) Voltage overshoot and current overshoot.

Loop Parasitic Inductance: L_p denotes all the stray inductances along the power loop and the parasitic inductances of the terminal of the power devices. Figure 14a illustrates the power losses with varied L_p . It can be seen that the turn-on loss decreases obviously with the increase in L_p , because the greater L_p will induce a larger voltage drop in stage 2, so that the voltage falling time will be shorter. However, as shown in Figure 14b, the larger L_p will generate a larger voltage overshoot and current voltage.

Figure 14. Comparison between experiment and calculation under the influence of loop parasitic inductance L_p . (a) Power losses. (b) Voltage overshoot and current overshoot.

Common Source Stray Inductance: L_{s2} differ from other stray inductances of PCB traces since it co-exists in both the power stage and the gate drive stage. When the MOSFET works in the saturation region (the channel equivalent to a voltage-controlled current source), the fast-changing drain current will induce a voltage drop across L_{s2} , which provides a negative feedback to the gate drive stage. Hence, the effect of L_{s2} on switching loss is similar to R_g , as shown in Figure 15. In common engineering practice, the gate driver is normally placed next to the power device as close as possible to reduce this inductance.

Figure 15. Comparison between experiment and calculation under the influence of common source stray inductance L_{s2} . (a) Power losses. (b) Voltage overshoot and current overshoot.

External Gate Stray Inductance: The comparison of power losses, voltage overshoot and current overshoot between experiment and calculation with varied external gate stray inductance L_{g2} is illustrated in Figure 16a,b, respectively. There is no recognizable difference with varied L_{g2} . In fact, according to the circuit design guidelines, L_{g2} should be kept small to avoid the oscillations between L_g and C_{gs} .

Figure 16. Comparison between experiment and calculation under the influence of external gate stray inductance L_{g2} . (a) Power losses. (b) Voltage overshoot and current overshoot.

According to the aforementioned experimental and analytical investigation, the effects of the varied elements including the T_j , R_g , L_p , L_{s2} and L_{g2} on the power losses and voltage and current overshoot in the switching transients are summarized in Table 6.

Table 6. Quantitative comparison of loss, voltage and current overshoot.

Elements	T	R_g	L_p	L_{s2}	L_{g2}
E_{sw-on}	↓	↑	↓	↑	→
E_{sw-off}	↑	↑	→	↑	→
E_{total}	→	↑	↓	↑	→
V_{os}	↓	↓	↑	↓	→
I_{os}	→	↓	↑	↓	→

↑/↓, denotes increase/decrease with the increase in the varied element; → denotes no obvious change the with the increase in the varied element.

6. Conclusions

This paper has presented an improved analytical loss model which takes the parasitic elements of the power devices and the stray inductances of the PCB traces into consideration. A comprehensive power device test platform is built to extract the key temperature-dependent parameters in the calculation. The measurement results show that the trans-conductance g_f , on-state resistance R_{on} , threshold voltage v_{th} and internal resistance R_{g-int} are sensitive to junction temperature. The switching waveforms of the proposed analytical model successfully match the experiment results of a 400-V, 15-A double-pulse-test bench. In addition, the variation patterns of power losses both in calculation and experiments can be summarized as follows.

(1) The increase in the gate driver resistance R_g or the common stray inductance L_{s2} will increase the total loss while decreasing the voltage overshoot and the current overshoot at the same time. In common practical applications, the gate driver resistance R_g is the only component that can be changed. Therefore, it should be chosen to compromise the conflicts between power loss and device stresses.

(2) The increase in the loop parasitic inductances L_p will decrease the total loss while increasing the voltage overshoot and the current overshoot in the meantime.

(3) The total loss does not change obviously with the varied junction temperature T_j and the varied external gate stray inductance L_{g2} .

The summarized conclusions above are expected to assist PCB layout design in practical applications of the SiC MOSFET, which is aimed at achieving a low power loss with proper device stresses. Future studies will be dedicated to varied circuits based on this study.

Author Contributions: Y.Z. and Y.Y. conceived and designed the study; Y.Z. gave the theoretical and data analysis; Y.Y. and P.L. revised the whole manuscript; Y.Z. wrote the paper. All authors have read and agreed to the published version of the manuscript.

Funding: This research was full supported by the National Key R&D Program of China (Grant No. 2018YFB0106300).

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{di_d}{dt} \\ \frac{dv_{gs}}{dt} \\ \frac{dv_{ds}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-R_{GG}}{L_g+L_s} & \frac{-1}{L_g+L_s} & 0 \\ \frac{C_{ds}+C_{gd}}{C_\Delta} & 0 & 0 \\ \frac{C_\Delta}{C_{gd}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_g \\ v_{gs} \\ v_{ds} \end{bmatrix} + \begin{bmatrix} \frac{V_{GG}}{L_g+L_s} \\ 0 \\ 0 \end{bmatrix} \quad (A1)$$

where, $C_\Delta = C_{gd}C_{gs} + C_{ds}(C_{gs} + C_{ds})$

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{di_d}{dt} \\ \frac{dv_{gs}}{dt} \\ \frac{dv_{ds}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-L_p R_{GG}}{L^*} & \frac{L_s R_f}{L^*} & \frac{-L_p}{L^*} & \frac{L_s}{L^*} \\ \frac{L_s R_{GG}}{L^*} & \frac{-(L_g+L_s)R_f}{L^*} & \frac{L_s}{L^*} & \frac{-(L_g+L_s)}{L^*} \\ \frac{C_{ds}+C_{gd}}{C^*} & \frac{C_{gd}}{C^*} & \frac{-C_{gd}g_f}{C^*} & 0 \\ \frac{C_{gd}}{C^*} & \frac{C_{gs}+C_{gd}}{C^*} & \frac{-g_f(C_{gs}+C_{gd})}{C^*} & 0 \end{bmatrix} \begin{bmatrix} i_g \\ i_d \\ v_{gs} \\ v_{ds} \end{bmatrix} + \begin{bmatrix} \frac{L_p}{L^*} & \frac{-L_s}{L^*} & \frac{-L_s R_f}{L^*} & \frac{-L_s}{L^*} & 0 \\ \frac{-L_s}{L^*} & \frac{L_g+L_s}{L^*} & \frac{(L_g+L_s)R_f}{L^*} & \frac{L_g+L_s}{L^*} & 0 \\ 0 & 0 & 0 & 0 & \frac{C_{gd}g_f}{C^*} \\ 0 & 0 & 0 & 0 & \frac{g_f(C_{gs}+C_{gd})}{C^*} \end{bmatrix} \begin{bmatrix} V_{GG} \\ V_{DD} \\ I_{DD} \\ V_f \\ V_{th} \end{bmatrix} \quad (A2)$$

where, $L^* = L_p(L_g + L_s) - L_s^2$, $C^* = (C_{gs} + C_{gd})(C_{ds} + C_{gd}) - C_{gd}^2$.

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{di_d}{dt} \\ \frac{dv_{gs}}{dt} \\ \frac{dv_{ds}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-L_p R_{GG}}{L^*} & \frac{L_s R_f}{L^*} & \frac{-L_p}{L^*} & \frac{L_s}{L^*} \\ \frac{L_s R_{GG}}{L^*} & \frac{-(L_g+L_s)R_f}{L^*} & \frac{L_s}{L^*} & \frac{-(L_g+L_s)}{L^*} \\ \frac{C_{ds}+C_{gd}}{C^*} & \frac{C_{gd}}{C^*} & 0 & \frac{-C_{gd}}{C^* R_{on}} \\ \frac{C_{gd}}{C^*} & \frac{C_{gs}+C_{gd}}{C^*} & 0 & \frac{-(C_{gs}+C_{gd})}{C^* R_{on}} \end{bmatrix} \begin{bmatrix} i_g \\ i_d \\ v_{gs} \\ v_{ds} \end{bmatrix} + \begin{bmatrix} \frac{L_p}{L^*} & \frac{-L_s}{L^*} & \frac{-L_s R_f}{L^*} & \frac{-L_s}{L^*} \\ \frac{-L_s}{L^*} & \frac{L_g+L_s}{L^*} & \frac{(L_g+L_s)R_f}{L^*} & \frac{L_g+L_s}{L^*} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{GG} \\ V_{DD} \\ I_{DD} \\ V_f \end{bmatrix} \quad (A3)$$

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{di_d}{dt} \\ \frac{dv_{gs}}{dt} \\ \frac{dv_{ds}}{dt} \\ \frac{dv_f}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-L_p R_{GG}}{L^*} & 0 & \frac{-L_p}{L^*} & \frac{L_s}{L^*} & \frac{L_s}{L^*} \\ \frac{L_s R_{GG}}{L^*} & 0 & \frac{L_s}{L^*} & \frac{-(L_g+L_s)}{L^*} & \frac{-(L_g+L_s)}{L^*} \\ \frac{C_{ds}+C_{gd}}{C^*} & \frac{C_{gd}}{C^*} & \frac{-g_f C_{gd}}{C^*} & 0 & 0 \\ \frac{C_{gs}+C_{gd}}{C^*} & \frac{C_{gs}+C_{gd}}{C^*} & \frac{-g_f (C_{gs}+C_{gd})}{C^*} & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_g \\ i_d \\ v_{gs} \\ v_{ds} \\ v_f \end{bmatrix} + \begin{bmatrix} \frac{L_p}{L^*} & \frac{-L_s}{L^*} & 0 & 0 \\ \frac{-L_s}{L^*} & \frac{L_g+L_s}{L^*} & 0 & 0 \\ 0 & 0 & \frac{g_f C_{gd}}{C^*} & 0 \\ 0 & 0 & \frac{g_f (C_{gs}+C_{gd})}{C^*} & 0 \\ 0 & 0 & 0 & \frac{-1}{C_f} \end{bmatrix} \begin{bmatrix} V_{GG} \\ V_{DD} \\ V_{th} \\ I_{DD} \end{bmatrix} \quad (A4)$$

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{di_d}{dt} \\ \frac{dv_{gs}}{dt} \\ \frac{dv_{ds}}{dt} \\ \frac{dv_f}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-L_p R_{GG}}{L^*} & \frac{R_{stray} L_s}{L^*} & \frac{-L_p}{L^*} & \frac{L_s}{L^*} & \frac{L_s}{L^*} \\ \frac{L_s R_{GG}}{L^*} & \frac{-R_{stray} (L_g+L_s)}{L^*} & \frac{L_s}{L^*} & \frac{-(L_g+L_s)}{L^*} & \frac{-(L_g+L_s)}{L^*} \\ \frac{C_{ds}+C_{gd}}{C^*} & \frac{C_{gd}}{C^*} & 0 & \frac{C_{gd}}{C^*} & 0 \\ \frac{C_{gs}+C_{gd}}{C^*} & \frac{C_{gs}+C_{gd}}{C^*} & 0 & \frac{-(C_{gs}+C_{gd})}{C^*} & 0 \\ 0 & \frac{1}{C_f} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_g \\ i_d \\ v_{gs} \\ v_{ds} \\ v_f \end{bmatrix} + \begin{bmatrix} \frac{L_p}{L^*} & \frac{-L_s}{L^*} & 0 \\ \frac{-L_s}{L^*} & \frac{L_g+L_s}{L^*} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_f} \end{bmatrix} \begin{bmatrix} V_{GG} \\ V_{DD} \\ I_{DD} \end{bmatrix} \quad (A5)$$

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{dv_{gs}}{dt} \\ \frac{dv_{ds}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-R_{SS}}{L_g+L_s} & \frac{-1}{L_g+L_s} & 0 \\ \frac{C_{ds}+C_{gd}}{C_{\Delta}} & 0 & \frac{-C_{gd}}{C_{\Delta} R_{on}} \\ \frac{C_{gd}}{C_{\Delta}} & 0 & \frac{-(C_{ds}+C_{gd})}{C_{\Delta} R_{on}} \end{bmatrix} \begin{bmatrix} i_g \\ v_{gs} \\ v_{ds} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_g+L_s} & 0 \\ 0 & \frac{C_{gd}}{C_{\Delta}} \\ 0 & \frac{C_{ds}+C_{gd}}{C_{\Delta}} \end{bmatrix} \begin{bmatrix} V_{SS} \\ I_{DD} \end{bmatrix} \quad (A6)$$

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{di_d}{dt} \\ \frac{dv_{gs}}{dt} \\ \frac{dv_{ds}}{dt} \\ \frac{dv_f}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-L_p R_{SS}}{L^*} & 0 & \frac{-L_p}{L^*} & \frac{L_s}{L^*} & \frac{L_s}{L^*} \\ \frac{L_s R_{SS}}{L^*} & 0 & \frac{L_s}{L^*} & \frac{-(L_g+L_s)}{L^*} & \frac{-(L_g+L_s)}{L^*} \\ \frac{C_{ds}+C_{gd}}{C^*} & \frac{C_{gd}}{C^*} & \frac{-g_f C_{gd}}{C^*} & 0 & 0 \\ \frac{C_{gs}+C_{gd}}{C^*} & \frac{C_{gs}+C_{gd}}{C^*} & \frac{-g_f (C_{gs}+C_{gd})}{C^*} & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_g \\ i_d \\ v_{gs} \\ v_{ds} \\ v_f \end{bmatrix} + \begin{bmatrix} \frac{L_p}{L^*} & \frac{-L_s}{L^*} & 0 & 0 \\ \frac{-L_s}{L^*} & \frac{L_g+L_s}{L^*} & 0 & 0 \\ 0 & 0 & \frac{g_f C_{gd}}{C^*} & 0 \\ 0 & 0 & \frac{g_f (C_{gs}+C_{gd})}{C^*} & 0 \\ 0 & 0 & 0 & \frac{-1}{C_f} \end{bmatrix} \begin{bmatrix} V_{SS} \\ V_{DD} \\ V_{th} \\ I_{DD} \end{bmatrix} \quad (A7)$$

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{di_d}{dt} \\ \frac{dv_{gs}}{dt} \\ \frac{dv_{ds}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-L_p R_{SS}}{L^*} & \frac{L_s R_f}{L^*} & \frac{-L_p}{L^*} & \frac{L_s}{L^*} \\ \frac{L_s R_{SS}}{L^*} & \frac{-(L_g+L_s) R_f}{L^*} & \frac{L_s}{L^*} & \frac{-(L_g+L_s)}{L^*} \\ \frac{C_{ds}+C_{gd}}{C^*} & \frac{C_{gd}}{C^*} & \frac{-C_{gd} g_f}{C^*} & 0 \\ \frac{C_{gs}+C_{gd}}{C^*} & \frac{C_{gs}+C_{gd}}{C^*} & \frac{-g_f (C_{gs}+C_{gd})}{C^*} & 0 \end{bmatrix} \begin{bmatrix} i_g \\ i_d \\ v_{gs} \\ v_{ds} \end{bmatrix} + \begin{bmatrix} \frac{L_p}{L^*} & \frac{-L_s}{L^*} & \frac{-L_s R_f}{L^*} & \frac{-L_s}{L^*} \\ \frac{-L_s}{L^*} & \frac{L_g+L_s}{L^*} & \frac{(L_g+L_s) R_f}{L^*} & \frac{L_g+L_s}{L^*} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{C_{gd} g_f}{C^*} \\ 0 & 0 & 0 & \frac{g_f (C_{gs}+C_{gd})}{C^*} \end{bmatrix} \begin{bmatrix} V_{SS} \\ V_{DD} \\ I_{DD} \\ V_f \\ V_{th} \end{bmatrix} \quad (A8)$$

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{di_d}{dt} \\ \frac{dv_{gs}}{dt} \\ \frac{dv_{ds}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-L_p R_{SS}}{L^*} & \frac{L_s (R_f+R_{stray})}{L^*} & \frac{-L_p}{L^*} & \frac{L_s}{L^*} \\ \frac{L_s R_{SS}}{L^*} & \frac{-(L_g+L_s) (R_f+R_{stray})}{L^*} & \frac{L_s}{L^*} & \frac{-(L_g+L_s)}{L^*} \\ \frac{C_{ds}+C_{gd}}{C^*} & \frac{C_{gd}}{C^*} & 0 & 0 \\ \frac{C_{gs}+C_{gd}}{C^*} & \frac{C_{gs}+C_{gd}}{C^*} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_g \\ i_d \\ v_{gs} \\ v_{ds} \end{bmatrix} + \begin{bmatrix} \frac{L_p}{L^*} & \frac{-L_s}{L^*} & \frac{-L_s R_f}{L^*} & \frac{-L_s}{L^*} \\ \frac{-L_s}{L^*} & \frac{L_g+L_s}{L^*} & \frac{(L_g+L_s) R_f}{L^*} & \frac{L_g+L_s}{L^*} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{SS} \\ V_{DD} \\ I_{DD} \\ V_f \end{bmatrix} \quad (A9)$$

References

1. Baliga, B.J. *Fundamentals of Power Semiconductor Devices*; Springer: New York, NY, USA, 2008.
2. Ning, P.; Wang, F.; Ngo, K.D. High-temperature SiC power module electrical evaluation procedure. *IEEE Trans. Power Electron.* **2011**, *26*, 3079–3083. [\[CrossRef\]](#)
3. Han, D.; Noppakunkajorn, J.; Sarlioglu, B. Efficiency comparison of SiC and Si-Based bidirectional DC-DC converters. In Proceedings of the 2013 IEEE Transportation Electrification Conference and Expo (ITEC), Piscataway, NJ, USA, 16–19 June 2013; pp. 1–7.
4. Josifovic, I.; Popovic-Gerber, J.; Ferreira, J.A. Improving SiC JFET switching behavior under influence of circuit parasitic. *IEEE Trans. Power Electron.* **2012**, *27*, 3843–3854. [\[CrossRef\]](#)
5. Yan, Q.; Yuan, X.; Geng, Y.; Charalambous, A.; Wu, X. Performance evaluation of split output converters with SiC MOSFETs and SiC schottky diodes. *IEEE Trans Power Electron.* **2017**, *32*, 406–422. [\[CrossRef\]](#)

6. Kadavelugu, A.; Baek, S.; Dutta, S.; Bhattacharya, S.; Das, M.; Agarwal, A.; Scofield, J. High-frequency design considerations of dual active bridge 1200 V SiC MOSFET dc-dc converter. In Proceedings of the 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 6–11 March 2011; pp. 314–320.
7. Wang, Y.; de Haan, S.W.H.; Ferreira, J.A. Potential of improving PWM converter power density with advanced components. In Proceedings of the 2009 13th European Conference on Power Electronics and Applications, Barcelona, Spain, 8–10 September 2009; pp. 1–10.
8. Ren, Y.; Xu, M.; Zhou, J.; Lee, F.C. Analytical loss model of power MOSFET. *IEEE Trans. Power Electron.* **2006**, *21*, 310–319.
9. Rainer, K.; Alberto, C. A physics-based compact model of SiC power MOSFETs. *IEEE Trans. Power Electron.* **2016**, *31*, 5863–5870.
10. Kumar, P.; Bhowmick, B. A physics-based threshold voltage model for hetero-dielectric dual material gate Schottky barrier MOSFET. *Int. J. Numer. Model.* **2018**, *31*, 1–11. [\[CrossRef\]](#)
11. Boram, Y.; Yeong-Hun, P.; Ji-Woon, Y. Physics-based compact model of transient leakage current caused by parasitic bipolar junction transistor in gate-all-around MOSFETs. *Solid State Electron.* **2020**, *164*, 1–12.
12. Potbhare, S.; Goldsman, N.; Lelis, A.; McGarrity, J.M.; McLean, F.B.; Habersat, D. A physical model of high temperature 4H-SiC MOSFETs. *IEEE Trans. Electron. Devices* **2008**, *55*, 2029–2039. [\[CrossRef\]](#)
13. Fu, R.; Grekov, A.; Peng, K.; Santi, E. Parasitic modeling for accurate inductive switching simulation of converters using SiC devices. In Proceedings of the 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, USA, 15–19 September 2013; pp. 1259–1265.
14. Wang, J.; Zhao, T.; Li, J.; Huang, A.Q.; Callanan, R.; Husna, F. Characterization, modeling, and application of 10-kV SiC MOSFET. *IEEE Trans. Electron Devices* **2008**, *55*, 1798–1806. [\[CrossRef\]](#)
15. Sun, K.; Wu, H.; Lu, J.; Xing, Y.; Huang, L. Improved modeling of medium voltage SiC MOSFET within wide temperature range. *IEEE Trans. Power Electron.* **2014**, *29*, 2229–2236. [\[CrossRef\]](#)
16. Jin, M.; Gao, Q.; Wang, Y.; Xu, D. A temperature-dependent sic MOSFET modeling method based on MATLAB/Simulink. *IEEE Access* **2018**, *6*, 4497–4505. [\[CrossRef\]](#)
17. Zhang, Z.; Eberle, W.; Yang, Z.; Liu, Y.; Sen, P. Optimal design of resonant gate driver for buck converter based on a new analytical loss model. *IEEE Trans. Power Electron.* **2008**, *23*, 653–666. [\[CrossRef\]](#)
18. Eberle, W.; Zhang, Z.; Liu, Y.; Sen, P. A practical switching loss model for buck voltage regulator. *IEEE Trans. Power Electron.* **2009**, *24*, 700–713. [\[CrossRef\]](#)
19. Rodríguez, M.; Rodríguez, A.; Miaja, P.F.; Lamar, D.G.; Zúniga, J.S. An insight into the switching process of power MOSFETs: an improved analytical losses model. *IEEE Trans. Power Electron.* **2010**, *25*, 1626–1640. [\[CrossRef\]](#)
20. Wang, J.; Chung, H.S. Impact of parasitic elements on the spurious triggering pulse in synchronous buck converter. *IEEE Trans. Power Electron.* **2014**, *29*, 6672–6685. [\[CrossRef\]](#)
21. Wang, J.; Li, R.T.; Chung, H.S. An investigation into the effects of the gate drive resistance on the losses of the MOSFET–Snubber–Diode configuration. *IEEE Trans. Power Electron.* **2012**, *27*, 2657–2672. [\[CrossRef\]](#)
22. Wang, J.; Chung, H.S.; Li, R.T. Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance. *IEEE Trans. Power Electron.* **2013**, *28*, 573–590. [\[CrossRef\]](#)
23. Liang, M.; Zheng, T.Q.; Li, Y. An improved analytical model for predicting the switching performance of SiC MOSFETs. *J. Power Electron.* **2016**, *16*, 374–387. [\[CrossRef\]](#)
24. Christen, D.; Biela, J. Analytical switching loss modeling based on datasheet parameters for MOSFETs in a half-bridge. *IEEE Trans. Power Electron.* **2019**, *34*, 3700–3710. [\[CrossRef\]](#)
25. Williams, R.K.; Darwish, M.N.; Blanchard, R.A.; Siemienieć, R.; Rutter, P.; Kawaguchi, Y. The trench power MOSFET—Part II: application specific VDMOS, IDMOS, packaging, and reliability. *IEEE Trans. Electron Devices* **2017**, *64*, 692–712. [\[CrossRef\]](#)
26. Mihir, M.; Shanmin, A.; Nance, E.; Frank, S.S. Datasheet driven silicon carbide power MOSFET model. *IEEE Trans. Power Electron.* **2014**, *29*, 2220–2228.
27. IEC 60747-8:2010.Semiconductor Devices—Discrete Devices—Part 8: Field-Effect Transistors. Available online: <https://webstore.iec.ch/publication/3289> (accessed on 18 July 2019).
28. CREE SiC MOSFET C2M0025120D Datasheet. Available online: <https://www.wolfspeed.com/media/downloads/161C2M0025120D.pdf> (accessed on 24 July 2019).

29. CREE SiC Diode C4D20120D Datasheet. Available online: <https://www.wolfspeed.com/media/downloads/106/C4D20120D.pdf> (accessed on 8 August 2019).
30. Lee, H.; Smet, V.; Tummala, R. A review of sic power module packaging technologies: Challenges, advances, and emerging issues. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *8*, 239–255. [CrossRef]
31. Liu, Z.; Huang, X.; Lee, F.C.; Li, Q. Package parasitic inductance extraction and simulation model development for the high voltage cascade GaN HEMT. *IEEE Trans. Power Electron.* **2014**, *29*, 1977–1985. [CrossRef]
32. Liu, T.; Wong, T.T.Y.; Shen, Z.J. A new characterization technique for extracting parasitic inductances of sic power MOSFETs in discrete and module packages based on two-port s-parameters measurement. *IEEE Trans. Power Electron.* **2018**, *33*, 9819–9833. [CrossRef]
33. Keysight Technologies, Application Note 1287-9, In-Fixture Measurements Using Vector Network Analyzers. 2017. Available online: <https://www.keysight.com/cn/zh/assets/7018-06814/application-notes/5968-5329.pdf> (accessed on 6 May 2020).
34. Liu, T.; Feng, Y.; Ning, R.; Wong, T.T.; Shen, Z.J. Extracting parasitic inductances of IGBT power modules with two-port S-parameter measurement. In Proceedings of the 2017 IEEE Transportation Electrification Conference and Expo (ITEC), Chicago, IL, USA, 22–24 June 2017; pp. 281–287.
35. Chen, K.; Zhao, Z.; Yuan, L.; Lu, T.; He, F. The impact of nonlinear junction capacitance on switching transient and its modeling for SiC MOSFET. *IEEE Trans. Electron. Devices* **2015**, *62*, 333–338. [CrossRef]
36. Costinett, D.; Maksimovic, D.; Zane, R. Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies. *IEEE Trans. Power Electron.* **2015**, *30*, 985–995. [CrossRef]
37. Ahmed, M.R.; Todd, R.; Forsyth, A.J. Predicting SiC MOSFET behavior under hard-switching, soft-switching, and false turn-on conditions. *IEEE Trans. Ind. Electron.* **2017**, *64*, 9001–9011. [CrossRef]
38. Wang, J.; Chung, S.H. A novel RCD level shifter for elimination of spurious turn-on in the bridge-leg configuration. *IEEE Trans. Power Electron.* **2015**, *30*, 976–984. [CrossRef]

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

© 2020 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).