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A Secondary Reconfigurable Inverter and Its Control Strategy

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Featured Application: First, this article proposes a topology of a secondary reconfigurable inverter. When the power semiconductor devices in the three-phase six-switch (TPSS) inverter is faulty, removing the faulty IGBT (Insulated Gate Bipolar Transistor), the remaining power switches and the DC side powers can be reconstructed as the three-phase four-switch (TPFS) structure. If another power switch in the reconfigured inverter is faulty, the reconfigured inverter can be reconfigured again. The fault-tolerant space is much larger than that of a traditional inverter. Second, this article proposes a switch-pulse-resetting algorithm. The general control strategy connects the constant-voltage, constant-frequency control with the switch pulse resetting algorithm. It need not change the control algorithm when the proposed reconfigurable inverter transforms the normal running state into the faulty running state.

Abstract: This article proposes a topology of the secondary reconfigurable inverter and the corresponding fault-tolerant control strategy. When the secondary reconfigurable inverter is operating normally, its topology structure is the TPSS circuit. When the power semiconductor devices in the inverter are faulty, the inverter circuit needs to be reconfigured. After removing the faulty power semiconductor devices, the remaining power semiconductor devices and the DC side powers are reconstructed as the TPFS structure to keep the system running normally. This article also proposes a switch-pulse-resetting algorithm. This paper adopts the control strategy connecting the constant-voltage, constant-frequency control method with the switch pulse resetting algorithm. It need not change the control algorithm when the proposed reconfigurable inverter is transformed from the normal running state into the faulty running state. The inverter dependability is greatly improved. Finally, the feasibility and effectiveness of the proposed second reconfigurable inverter topology and control strategy are verified by simulation and experiment.

Keywords: secondary reconfigurable; switch pulse resetting; three-phase four-switch

1. Introduction

With the development of power electronics technology, voltage source inverters have been widely used [1–4]. The power semiconductor devices of the inverter and its control circuit constitute the weakest link, which is vulnerable to being faulty. Its reliability problems have not been solved effectively [5–7]. The usual faults in the inverter are short circuits and open circuits of power semiconductor devices. The wrong triggering signals, the auxiliary power failure, the device over-voltage breakdown, the avalanche breakdown, and the thermal breakdown can lead to a short circuit fault on the power semiconductor device. Since the existence of a short circuit fault time is too short, it is hard to diagnose. Hence, the diagnosis and protection of short circuit faults are mostly based on the design of the

hardware circuit. This has been summarized in the literature [8]. The fast fuse can also be put into the inverter circuit to turn the short circuit fault into the open circuit, which uses the open circuit diagnosis method to handle the faults. It is therefore convenient to implement the topology reconfiguration and the fault-tolerant control strategy [9,10]. The main reasons causing the open circuit of the power switches are the device rupture, the bonding line breaking or welding, the loss of driving signals or the circuit failure, etc. A power semiconductor device fault will make the inverter operate in an abnormal state and affect the system performance, and the voltage and current stresses of the other devices will be increased. The system will crash, so it must be diagnosed in time.

To improve the dependability of inverters, fault-tolerant strategies have been investigated by a large number of studies. These can be divided into redundant and nonredundant fault-tolerant strategies. Redundant fault-tolerant strategies include switch-redundant topologies [9], neutral leg topologies [10], additional phase leg topologies [11], cascaded inverter topology [12], etc. In the modular multilevel inverter, many standardized redundant modules are integrated into the branch to allow the system redundancy [13]. However, these solving methods are often complex. The nonredundant fault-tolerant inverter structure reconstructs the faulty inverter. Three-phase four-switch (TPFS) inverters have been intensively researched as the fault-tolerant topology structure when a three-phase six-switch (TPSS) inverter is faulty, where one phase terminal is connected to the midpoint of the DC side capacitors. The TPFS inverter can improve the system reliability and has the potential for quick recovery of partial system performance [14,15]. The development of the four-switch inverter technology in the field of motor drive is relatively mature [16–30], including DC Motors, IM Drives etc. However, it was not fault-tolerant. The literature [28,29] has adopted the traditional fault-tolerant TPFS inverter in the microgrid. However, the control strategy was complicated. There are many fault-tolerant control strategies when an open circuit fault occurs. Fault-tolerant control strategies have been proposed for diodes of NPC (neutral point clamped) inverters [31], flying-span capacitor inverters [32], cascade multilevel inverters [33,34], T-type three-level inverters [35,36], etc.. Additional TRIACS (TRIode alternating current semiconductor) are added for fault-tolerant operations [31–38].

However, if the traditional fault-tolerant inverter undergoes a power semiconductor device fault on any bridge, the bridge arm needs to be removed, and the control algorithm in the normal running state needs to be converted into the control algorithm in the faulty state, which is complicated. In response to these problems, a topology of a secondary reconfigurable inverter and the corresponding control strategy are proposed in this article. The reconfigurable fault-tolerant space is much larger than that of the traditional fault-tolerant inverter. This article also proposes a switch-pulse-resetting algorithm. The inverter can be kept stable running with the proposed control strategy, which needs not change the control algorithm converting the normal running state into the faulty running state.

This article is organized as follows. Section 2 proposes the topology structure of the secondary reconfigurable inverter. The equivalent circuits in the first faulty state and second faulty state are given separately, and the operating principle of the reconfigurable inverter is analyzed. The normal operating principle and faulty operating principle of the secondary reconfigurable inverter are analyzed, and then the relationship between the normal state and the fault state of the corresponding DC side voltage is obtained. In addition, the switch pulse resetting algorithm is proposed. In Section 3, the feasibility and effectiveness of the proposed second reconfigurable inverter topology and control strategy are verified by simulation and experiment. Section 4 presents the conclusions.

2. Materials and Methods

2.1. The Topology Structure of the Secondary Reconfigurable Inverter

The topology structure of the proposed secondary reconfigurable inverter is shown in Figure 1. The inverter DC side voltage is provided by battery storage, which can ideally be considered as two DC sources with equal voltage value. V_1–V_6 are the power semiconductor devices IGBT, which constitute the three-phase inverter circuit. TR_{13}, TR_{35}, TR_b and TR_w are the TRIACS, which consist of

the secondary reconfigurable circuit. A series of LC filters are used to inhibit higher harmonics and excessive short-circuit current. When the secondary reconfigurable inverter is operating normally, it is a TPSS inverter circuit.

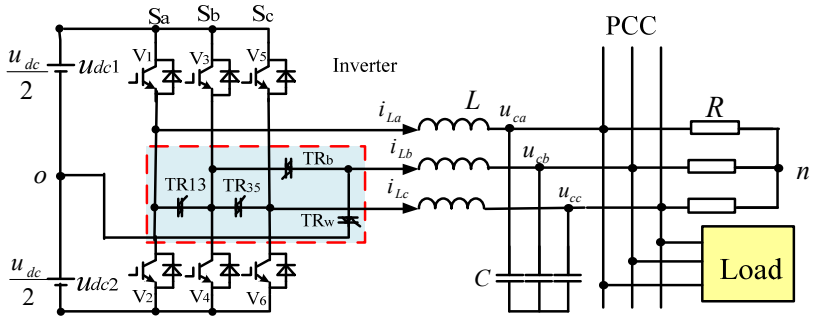


Figure 1. The topology structure of the proposed secondary reconfigurable inverter.

The usual faults for the inverter are the short circuit and the open circuit of the power semiconductor devices. When the power semiconductor devices in the inverter encounter a short-circuit fault, the corresponding fast fuses will be fused, and the short-circuit fault is transformed into the open-circuit fault. The secondary reconfigurable inverter circuit is formed by cutting off the fault switches and connecting with the corresponding Triacs. When one or two of the power switch is faulty, the relationship among the corresponding Triacs and power switches are shown in Table 1.

Table 1. Secondary reconfigurable inverter switching status.

Case	First Fault	On	Reconfigured Phases	Second Fault	Reconfigured Phases	Switch Pulse Resetting
0	/	TR_b	/	/	/	/
1	V_1	TR_w and TR_{13}	S_a (V_3, V_2) S_b (C_1, C_2)	/	/	$T_{v3} = T_{v1}$
2	V_1	TR_w and TR_{13}	/	V_2	S_a (V_3, V_4) S_b (C_1, C_2)	$T_{v4} = T_{v2}$
3	V_2	TR_w and TR_{13}	S_a (V_1, V_4) S_b (C_1, C_2)	/	/	$T_{v4} = T_{v2}$
4	V_2	TR_w and TR_{13}	/	V_1	S_a (V_3, V_4) S_b (C_1, C_2)	$T_{v3} = T_{v1}$
5	V_3	TR_w	S_b (C_1, C_2)	/	/	/
6	V_3	TR_w and TR_{13}		V_2	S_a (V_1, V_4) S_b (C_1, C_2)	$T_{v4} = T_{v2}$
7	V_3	TR_w and TR_{35}	/	V_6	S_c (V_5, V_4) S_b (C_1, C_2)	$T_{v4} = T_{v6}$
8	V_4	TR_w	S_b (C_1, C_2)	/	/	/
9	V_4	TR_w and TR_{13}		V_1	S_a (V_3, V_2) S_b (C_1, C_2)	$T_{v3} = T_{v1}$
10	V_4	TR_w and TR_{35}		V_5	S_c (V_3, V_6) S_b (C_1, C_2)	$T_{v3} = T_{v5}$
11	V_5	TR_w and TR_{35}	S_c (V_3, V_6) S_b (C_1, C_2)	/	/	$T_{v3} = T_{v5}$
12	V_5	TR_w and TR_{35}		V_4	S_c (V_3, V_6) S_b (C_1, C_2)	$T_{v6} = T_{v4}$
13	V_6	TR_w and TR_{35}	S_c (V_5, V_4) S_b (C_1, C_2)	/		$T_{v4} = T_{v6}$
14	V_6	TR_w and TR_{35}		V_3	S_c (V_5, V_4) S_b (C_1, C_2)	$T_{v5} = T_{v3}$
15	V_1 and V_2	TR_w and TR_{13}	S_a (V_3, V_4) S_b (C_1, C_2)	/	/	$T_{v3} = T_{v1}$,$T_{v4} = T_{v2}$
16	V_3 and V_4	TR_w	S_b (C_1, C_2)	/	/	
17	V_5 and V_6	TR_w and TR_{35}	S_c (V_3, V_4) S_b (C_1, C_2)	/	/	$T_{v3} = T_{v1}$,$T_{v4} = T_{v2}$
18	V_1 and V_4	TR_w and TR_{13}	S_a (V_3, V_2) S_b (C_1, C_2)	/	/	$T_{v3} = T_{v1}$,$T_{v2} = T_{v4}$
19	V_2 and V_3	TR_w and TR_{13}	S_a (V_1, V_4) S_b (C_1, C_2)	/	/	$T_{v1} = T_{v3}$,$T_{v4} = T_{v2}$
20	V_3 and V_6	TR_w and TR_{35}	S_c (V_5, V_4) S_b (C_1, C_2)	/	/	$T_{v5} = T_{v3}$,$T_{v4} = T_{v6}$
21	V_4 and V_5	TR_w and TR_{35}	S_c (V_3, V_6) S_b (C_1, C_2)	/	/	$T_{v3} = T_{v5}$,$T_{v6} = T_{v4}$

In Table 1, consider cases 1 and 2 as examples. When the power switch V_1 in the TPSS inverter circuit is faulty, turn on the Triacs TR_wandTR_{13}. Sending the pulse of V_1 to be the pulse of V_3 means that $T_{v3} = T_{v1}$. The DC side voltage source can be considered as the b-phase bridge of the inverter, which constitutes the TPFS inverter circuit. V_4 stops working. The reconstructed phases are S_a(V_3, V_2) and S_b(C_1, C_2). The reconstructing process is shown in Figure 2a, which is the first fault tolerance. Now the

inverter is running in a fault-tolerant state. If V_2 is also faulty, V_3 and V_4 construct phase $S_a(V_3, V_4)$, sending the pulse of V_2 to be the pulse of V_4, $T_{v4} = T_{v2}$, which is the secondary reconfiguration as shown in Figure 2b. Other cases have a similar switch process.

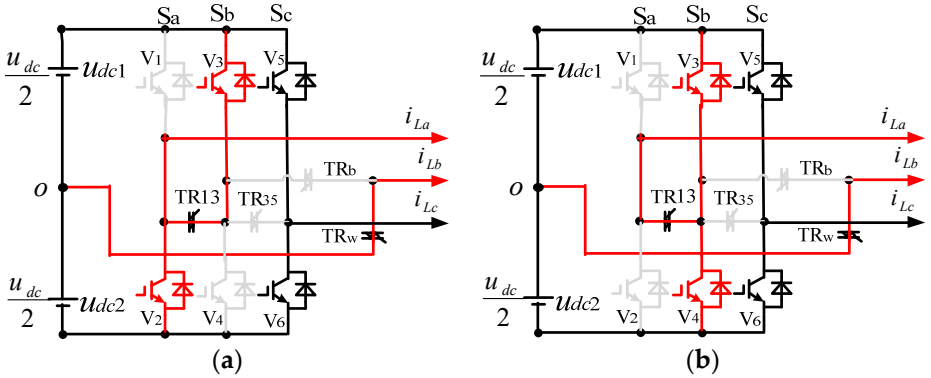


Figure 2. The secondary reconfiguring process of the inverter: (**a**) the first reconfiguration; (**b**) the secondary reconfiguration.

The traditional reconfigurable fault-tolerant inverter is shown in Figure 3.

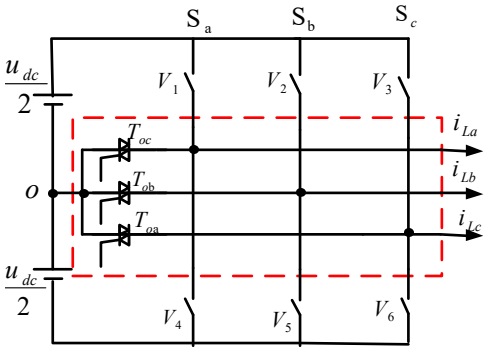


Figure 3. The traditional reconfigurable fault-tolerant inverter.

From Figure 3, it can be seen that if one or two of the power switches in the traditional fault-tolerant inverter are faulty, the whole bridge needs to be removed. The relationship between the corresponding Triacs and power switches are shown in Table 2.

Table 2. The traditional inverter switching status.

Case	Fault	On	Reconfigured Phases
0	/	/	/
1	V_1	T_{oc}	S_a (C_1, C_2)
2	V_4	T_{oc}	S_a (C_1, C_2)
3	V_2	T_{ob}	S_b (C_1, C_2)
4	V_5	T_{ob}	S_b (C_1, C_2)
5	V_3	T_{oa}	S_c (C_1, C_2)
6	V_6	T_{oa}	S_c (C_1, C_2)
7	V_1 and V_4	T_{oc}	S_a (C_1, C_2)
8	V_2 and V_5	T_{ob}	S_b (C_1, C_2)
9	V_3 and V_6	T_{oa}	S_c (C_1, C_2)

According to Table 2, the fault-tolerant space is small with just nine cases. The topology of the secondary reconfigurable inverter proposed in this paper greatly improves the fault-tolerant space. According to Table 1, the proposed secondary reconfigurable inverter has 21 fault-tolerant cases.

Therefore, compared with the traditional inverter, the proposed secondary reconfigurable inverter has a broader fault-tolerant space. The fault-tolerant space of the proposed secondary reconfigurable inverter is improved greatly. Moreover, the control algorithm in a normal operation state needs to be converted into the control algorithm in the faulty state, which is complicated.

2.2. Analysis of the Fault Tolerant Inverter Operating Principle

2.2.1. Analysis of the Switching Mode

When the secondary reconfigurable inverter is running in the faulty state, the faulty power switch is removed. The remaining power switches of the two bridges can be reconfigured to keep operating. Each switching mode of the TPFS inverter has the corresponding switching mode as the TPSS inverter in a normal state. Varieties of switching modes and current paths of the TPSS inverter circuit and the reconfigured TPFS inverter circuit are shown in Figure 4.

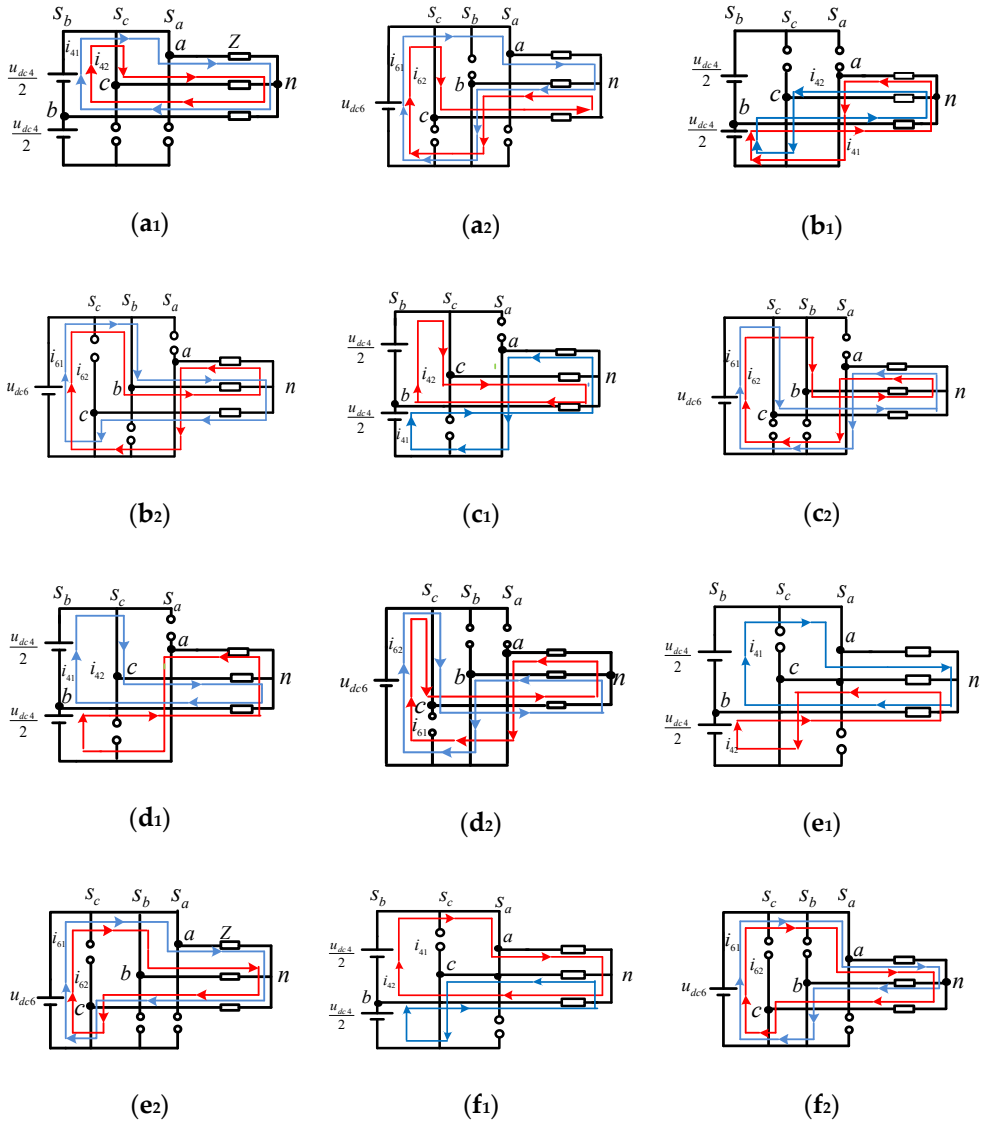


Figure 4. Switching modes and current paths (S_a, S_c) for the faulty state and (S_a, S_b, S_c) for the normal state: (**a1**) (1,1); (**a2**) (1, 0, 1); (**b1**) (0,0); (**b2**) (0,1, 0); (**c1**) (0,1); (**c2**) (0,1, 1); (**d1**) (0,1); (**d2**) (0,0, 1); (**e1**) (1,0); (**e2**) (1,1, 0); (**f1**) (1,0); (**f2**) (1,0, 0).

In switching mode (a_1), there are two current paths, i_{41} and i_{42}, which both flow from the upper-half source of the DC-side source, which is equivalent to the condition that the b-phase lower-half bridge is

connected and the upper bridge arm is cut off in the TPSS inverter circuit. At the moment, two current paths, i_{61} and i_{62}, also exist in the TPSS inverter circuit.

According to the switching mode (a_1) in Figure 4, the two current paths i_{41} and i_{42} satisfy the following equations, respectively.

$$i_{41} = \frac{\frac{u_{dc4}}{2}}{2Z} = \frac{u_{dc4}}{4Z} \tag{1}$$

$$i_{42} = \frac{\frac{u_{dc4}}{2}}{2Z} = \frac{u_{dc4}}{4Z} \tag{2}$$

Therefore the three-phase output voltages of the reconfigurable inverter circuit are

$$u_{an4} = i_{41}Z = \frac{u_{dc4}}{4} \tag{3}$$

$$u_{cn4} = i_{42}Z = \frac{u_{dc4}}{4} \tag{4}$$

$$u_{bn4} = (i_{41} + i_{42})Z = \frac{u_{dc4}}{2} \tag{5}$$

In switching mode (a_2), the two current paths i_{61} and i_{62} of the normal inverter circuit satisfy the following equations, respectively.

$$i_{61} = \frac{u_{dc6}}{2Z} \tag{6}$$

$$i_{62} = \frac{u_{dc6}}{2Z} \tag{7}$$

Then, the three-phase output voltages of the normal inverter circuit are defined by the following equations respectively.

$$u_{an6} = i_{61}Z = \frac{u_{dc6}}{2} \tag{8}$$

$$u_{cn6} = i_{62}Z = \frac{u_{dc6}}{2} \tag{9}$$

$$u_{bn6} = (i_{61} + i_{62})Z = u_{dc6} \tag{10}$$

Let the three-phase output voltages of the reconfigurable inverter circuit be equal to the three-phase output voltages of the normal inverter circuit, respectively. Hence,

$$\begin{cases} u_{an4} = u_{an6} \\ u_{bn4} = u_{bn6} \\ u_{cn4} = u_{cn6} \end{cases} \tag{11}$$

That is to say,

$$u_{dc4} = 2u_{dc6} \tag{12}$$

Connecting Equation (12) with the Equations (1), (2), (6) and (7), it can be derived that the output current of the inverter satisfies the following equations

$$i_{41} = i_{61} \tag{13}$$

$$i_{42} = i_{62} \tag{14}$$

Similar results can be obtained in other switching modes, which are not repeated here. By setting the DC side voltage value of the reconfigurable inverter to be twice the DC-side voltage in the normal state, we can control the inverter according to the switching state shown in Table 1, no matter if the inverter is running in a faulty state or in a normal state. The normal output voltage and output current can be obtained in both states.

2.2.2. The Control Strategy for the Reconfigurable Inverter

When the power semiconductor devices of the secondary reconfigurable inverter are faulty, the TPSS inverter circuit is reconfigured as the TPFS inverter circuit. The relationship between the pulse signals produced by the SPWM (Sinusoidal Pulse Width Modulation) and the on–off states of each power semiconductor device is shown in Table 1. T_{v1}–T_{v6} are the 6-channel modulation signals.

The switch-pulse-resetting algorithm is also proposed in this article. This article adopts the control strategy connecting the voltage–frequency control strategy with the switch-pulse-resetting algorithm. The flow figure of the control strategy is seen in Figure 5.

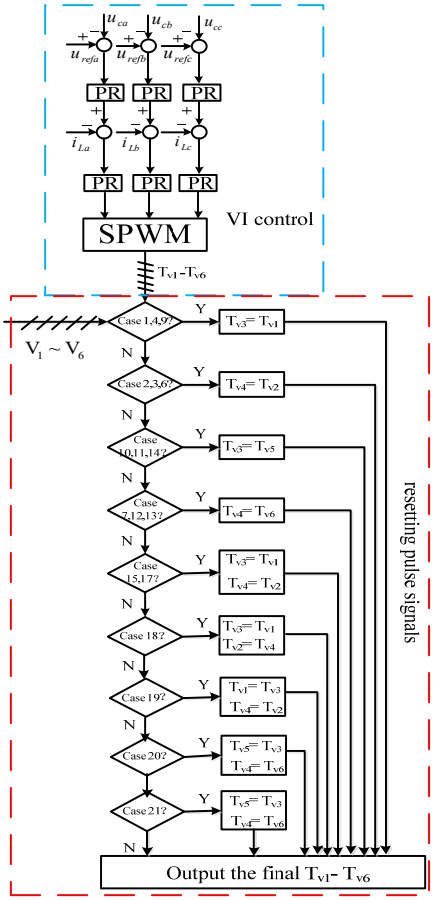


Figure 5. The proposed control strategy flow figure.

In Figure 5, the signals produced by VI control are put into SPWM, and then the initial 6-channel pulse signals T_{v1}–T_{v6} are obtained by the SPWM. According to the on–off states of the 6 power semiconductor devices V_1–V_6, whether each pulse signal needs to alter or not is determined by the on–off states of 6 power semiconductor devices V_1–V_6. Finally, the device outputs the resetting pulse signals T_{v1}–T_{v6} according to the red box in the Figure 5. There is no need for other cases to alter the initial pulse signals: Figure 5 shows that it need not alter the control algorithm when the system running from the normal state into the faulty state.

3. Results and Discussion

3.1. Simulation Results and Discussion

The circuit model of the secondary reconfigurable inverter shown in Figure 1 was built in MATLAB/Simulink platform to verify the feasibility and effectiveness of the proposed reconfigurable

inverter in this article. This paper adopts the controlling strategy connecting the constant-voltage, constant-frequency control method and the switch pulse resetting algorithm.

The main parameters of the reconfigurable inverter applied in islanded micro-grid are shown the following Table 3.

Table 3. The main parameters of the simulation model.

Main Parameters	Value
Reference voltage amplitude U_m\V	220
Reference voltage frequency f\Hz	50
DC side voltage u_{dc}\V	400/800
IGBT switch frequency\kHz	10
Output side filter inductance L_0\mH	1.2
Output side filter capacitance C_0\μF	4000
Load resistance value R_L\Ω	12
Load inductance value L_L\mH	1.4
K_p of PR	0.6
K_R of PR	500

The simulation waveforms of the reconfigurable inverter applied to the islanded microgrid in the normal operating state and various faulty states are shown as follows. Set the system operating in normal state during 0–0.1 s and operating in the faulty state during 0.1–0.2 s.

The simulation results of the inverter without reconfigurable structure are shown in Figure 6, which include the waveforms of the output voltages, the output currents and the deviations between output voltages with reference voltages. Figure 7 shows the simulation results of the inverter with a reconfigurable structure.

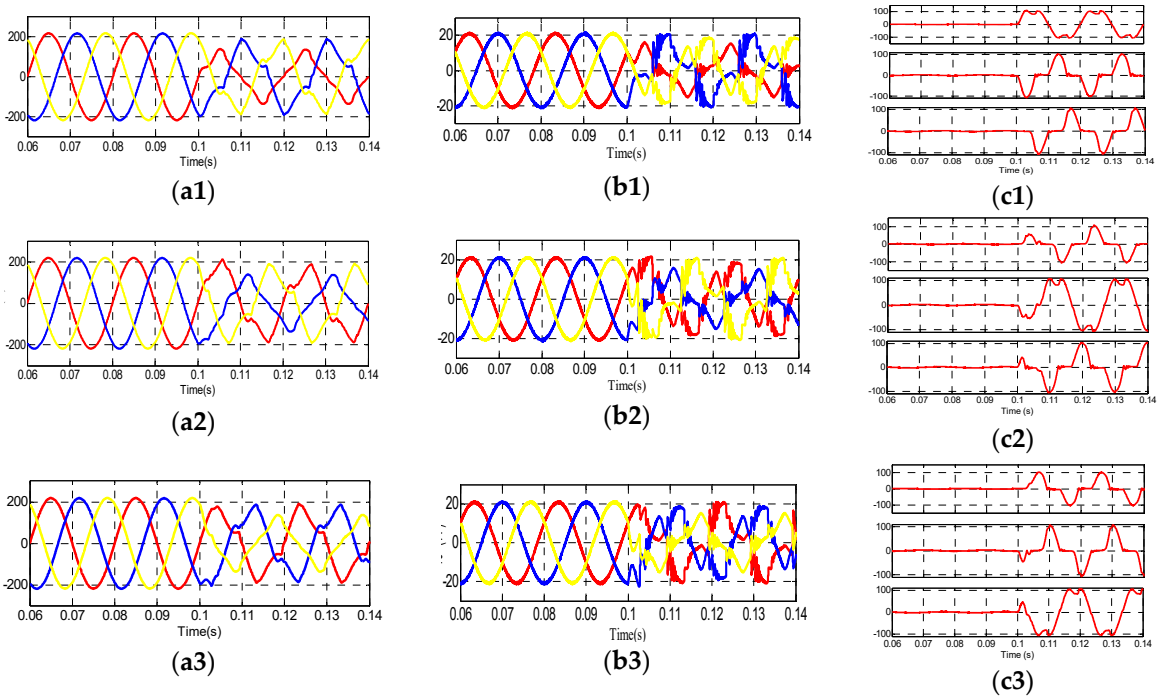
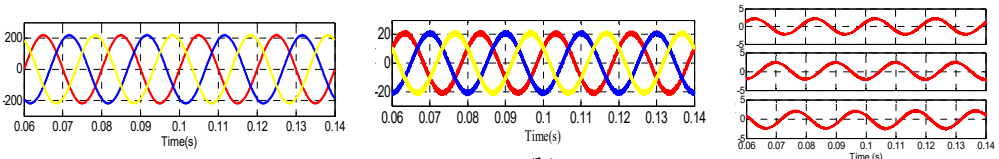


Figure 6. Simulation results of the non-reconfigurable inverter: (**a1**) output voltages under faulty phase a; (**a2**) output voltages under faulty phase b; (**a3**) output voltages under faulty phase c; (**b1**) currents under faulty phase a; (**b2**) currents under faulty phase b; (**b3**) currents under faulty phase c; (**c1**) voltage deviations under faulty phase a; (**c2**) voltage deviations under faulty phase b; (**c3**) voltage deviations under faulty phase c.



(**a**) (**b**) (**c**)

Figure 7. Simulation results of the reconfigurable inverter under faulty phase a: (**a**) output voltages; (**b**) currents; (**c**) voltage deviations.

When the DC side voltage is set as 400 V and without reconfigurable structure in the inverter, Figure 6a1,b1,c1 show output voltages, currents and deviations between the output voltage with the reference voltage corresponding to faulty phase a, respectively. Figure 6a2,b2,c2 show output voltages, currents and deviations between the inverter output voltage with the reference voltage corresponding to faulty phase b, respectively. Figure 6a3,b3,c3 show output voltages, currents and deviations between the inverter output voltage with the reference voltage corresponding to faulty phase c, respectively. It can be seen from the waveforms that the inverter voltages and the currents of the inverter are the expected standard sinusoidal waves when the inverter is running in the normal state at 0–0.1 s. Moreover, the deviation among the inverter output voltage with reference voltage is very small at about 3 V. After 0.1 s, the inverter is running in the faulty state. The inverter output voltage and output current are seriously distorted, and a three-phase imbalance appears. The deviation among inverter output voltage with reference voltage is too large.

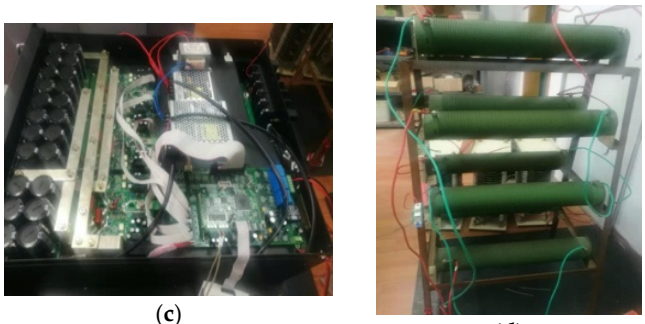
Take case 1 in Table 1 as an example to verify the feasibility and validity of the proposed topology and the control algorithm in this simulation. The power switch V_1 is faulty, and the inverter is reconstructed from TPSS to TPFS to be fault-tolerant. The DC voltage is set as 800 V in the reconfigurable inverter. Figure 7a–c are output voltages, currents and deviations between the output voltage with the reference voltage, respectively. All waveforms can be kept the same before and after the inverter is reconfigured because a power switch is broken at 0.1 s. If another power switch is faulty, the same output voltages and currents are obtained as the results in the first reconfiguration. Figure 7 represents the similar simulating waveforms of other cases in Table 1. That is to say, whether the inverter is reconfigured or not because of one or two power switches being broken, the output voltages and currents are similar to the reference voltages and currents. Therefore, the simulation results verify the feasibility and effectiveness of the proposed secondary reconfigurable inverter topology and control strategy.

3.2. Experimental Results and Discussion

To further verify the feasibility and effectiveness of the proposed circuit topology of secondary reconfigurable inverter for the islanded microgrid, the experimental platform of the reconfigurable inverter was built. The system parameters were the same as the simulation parameters. DSP(digital signal processor) TMS320F2812 was used to generate pulses for the fault-tolerant inverter. Images of the experimental setups are shown in Figure 8. The main circuit board has a good and compact structural layout. The DC side voltages are provided by the rectifier. The loads are the resistors.

(**a**) (**b**)

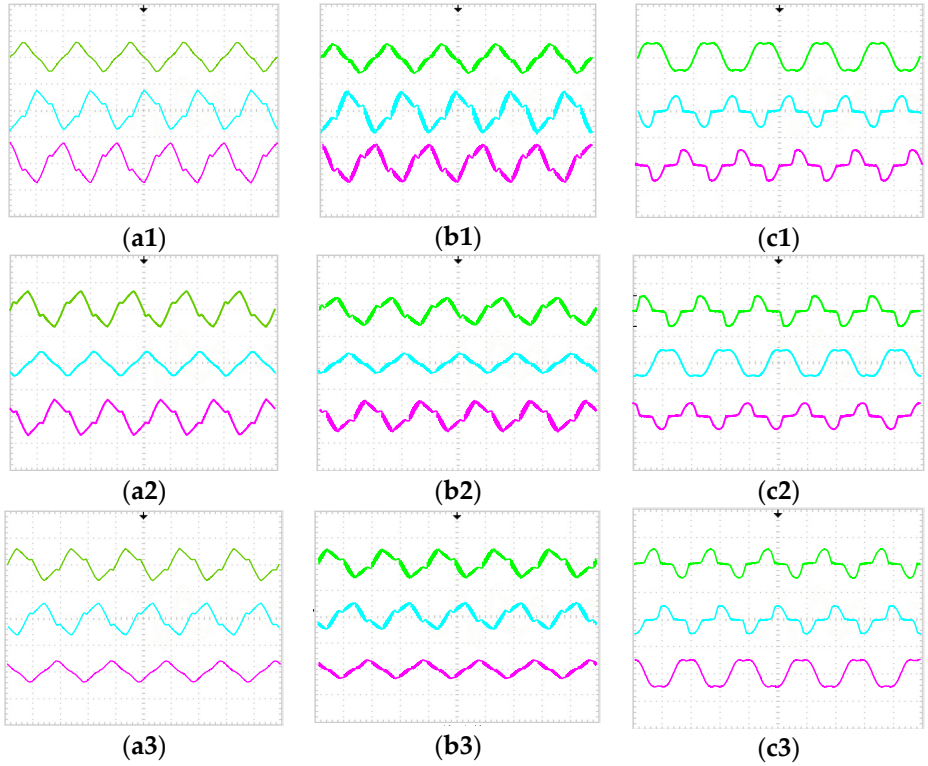
Figure 8. *Cont.*



(**c**) (**d**)

Figure 8. The experiment setup: (**a**) the main circuit board; (**b**) DSP; (**c**) the rectifier; (**d**) the load.

When the DC side voltage is set as 400 V in the non-reconfigurable inverter that is faulty, in phase a, phase b and phase c, the experimental results are shown in Figure 9. Figure 9a1–a3 show output voltages corresponding, respectively, to faulty phase a, b and c with the vertical axis 100 V/grid and horizontal axis 10 ms/grid. Figure 9b1–b3 show output currents corresponding, respectively, to faulty phase a, b and c with the vertical axis 30 A/grid and horizontal axis 10 ms/grid. Figure 9c1–c3 show the voltage deviations between output voltages and reference voltages corresponding, respectively, to faulty phase a, b and c with the vertical axis 50 V/grid and horizontal axis 10 ms/grid. This can be seen from the waveforms being distorted seriously and three-phase imbalance when the inverter is operating in a faulty state. The voltage deviations between output voltages and reference voltages are too large.



(**a1**) (**b1**) (**c1**)

(**a2**) (**b2**) (**c2**)

(**a3**) (**b3**) (**c3**)

Figure 9. The experimental results of the non-reconfigurable inverter (**a1**) output voltages under faulty phase a; (**a2**) output voltages under faulty phase b; (**a3**) output voltages under faulty phase c; (**b1**) currents under faulty phase a; (**b2**) currents under faulty phase b; (**b3**) currents under faulty phase c; (**c1**) voltage deviations under faulty phase a; (**c2**) voltage deviations under faulty phase b; (**c3**) voltage deviations under faulty phase c.

Take case 1 in Table 1 as an example to verify the feasibility and validity of the proposed topology and the control algorithm. The power switch V_1 is faulty, and the inverter is reconstructed from TPSS to TPFS. Figure 10a1,a2 show output voltages corresponding to faulty phase a with the vertical axis 100 V/grid and horizontal axis 10 ms/grid. Figure 10b1,b2 show output currents corresponding to faulty phase a with the vertical axis 30 A/grid and horizontal axis 10 ms/grid. Figure 10c1,c2 show the voltage deviations between output voltages and reference voltages with the vertical axis 50 V/grid and horizontal axis 10 ms/grid. When the DC side voltage is set as 800 V in the reconfigurable inverter to be fault-tolerant, the experimental results of the changing process from a normal state to fault-tolerant state are shown in Figure 10a1,b1,c1. Since the DC side voltage satisfies all DC voltage conditions, it can be seen that the fault-tolerant waves are similar to the normal ones after the transient state. The inverter output voltages and output currents are standard sinusoidal waves. The deviation among inverter output voltage with reference voltage is small, and the steady experimental results are shown in Figure 10a2–c2. All the output waveforms after the inverter is reconstructed are similar to those in normal states. Other cases in Table 1 have similar results. Experimental results further verified the feasibility and validity of the proposed secondary reconfigurable topology and the control algorithm.

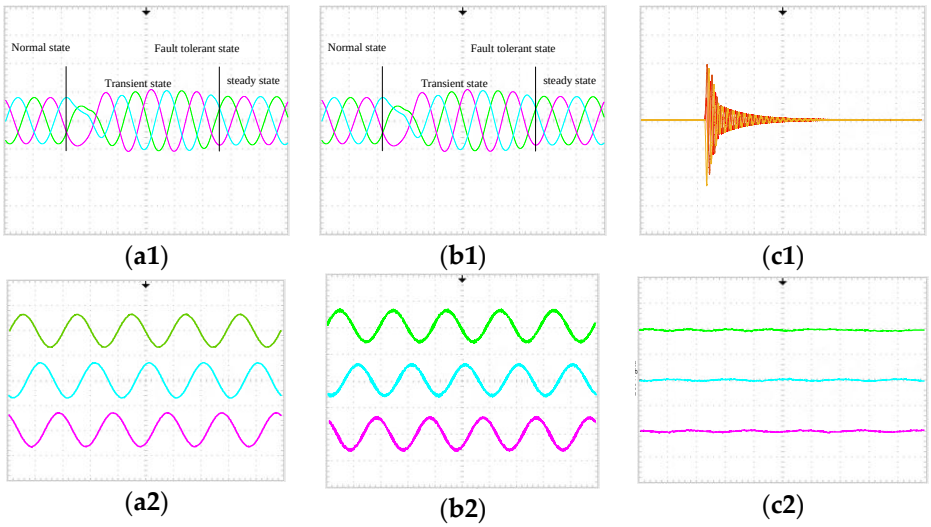


Figure 10. The experimental results of the reconfigurable inverter under faulty V_1 (**a1**) dynamic output voltages; (**a2**) steady output voltages; (**b1**) dynamic currents; (**b2**) steady currents; (**c1**) dynamic voltage deviation; (**c2**) steady voltage deviation.

4. Conclusions

This article proposes a novel secondary reconfigurable inverter and the corresponding fault-tolerant control strategy. When the power semiconductor devices in the inverter are faulty, removing the faulty power semiconductor devices, the remaining power semiconductor devices and the DC source are remodeled to keep the inverter running. The fault-tolerant space is much larger than that of traditional inverter. This article has analyzed the relationship between the DC side voltages in a faulty state and in a normal state, given the corresponding control strategy and the switch-pulse-resetting algorithm. It need not change the control algorithm when the proposed reconfigurable inverter transforms the normal state into the faulty state. The simulation model was built in a normal state and various faulty states. The simulation and experimental results verify the feasibility and effectiveness of the proposed reconfigurable inverter topology structure and the control strategy.

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