


Article

Low Voltage Delay Element with Dynamic Biasing Technique for Fully Integrated Cold-Start in Battery-Assistance DC Energy Harvesting Systems

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Abstract: This paper proposes an ultra-low voltage delay element for battery-assistance DC energy harvesting systems. By inserting a low voltage level shifter (VLS), a wider voltage range is obtained to bias the body of the delay element. Thus, both the voltage transfer curve (VTC) and the DC gain of the delay element are enhanced. Due to the introduction of the VLS, the cold start-up ring oscillator constituted by the proposed delay element can achieve oscillation under an extremely low input voltage. The fully integrated cold start-up ring oscillator with 21 stages of the proposed element is implemented in a standard 180 nm complementary metal oxide semiconductor (CMOS) process. The post-layout experimental results indicate that the cold start-up ring oscillator can retain oscillation when the power supply voltage (VDD) is 24 mV under a typical corner at room temperature. The output voltage swing of the cold start-up ring oscillator based on the proposed delay element is improved by more than 55% under VDD = 40 mV compared with a stacked inverter-based cold start-up ring oscillator. Monte Carlo (MC) simulation from 100 samples shows the enhanced output swing with the proposed delay element under process variation.

Keywords: battery-assistance; cold start-up; energy harvesting; ring oscillator; dynamic biasing technique; low-voltage cold start; on/off resistance ratio

1. Introduction

How to prolong battery life is one of the main goals for researchers and engineers around the world. Analog/Radio Frequency (RF) circuit modules usually dominate the power consumption of whole systems. Although low power research has driven the power consumption of analog/RF modules into sub-mW [1], it is still challenging to enable a system to work for more than ten years without battery replacement. The emergence of the internet of things (IoT) requires thousands of nodes to achieve the connection of everything. Battery replacement for those nodes will have an overwhelming cost and be an obstacle in the deployment of the IoT application. To solve this issue, the energy harvesting technique as a potential candidate has attracted massive research [2–14].

Both the battery-less energy harvesting system [2–12] and the battery-assistance energy harvesting system [13,14] have been reported upon in the literature, as shown in Figure 1. For the battery-less energy harvesting system, as indicated in Figure 1a, the issue of battery replacement is fundamentally solved and all the energy consumed by loads is harvested from the surrounding environment. The surplus energy is stored on an off-chip supercapacitor. The main issue for the battery-less energy harvesting system is the start-up period of the system, as the surrounding energy may not

be able to activate the whole system during the initial phase. However, the battery-assisted energy harvesting system employs a rechargeable battery as an energy reservoir, which stores available energy in advance, as shown in Figure 1b; and the surplus energy can also be stored on this rechargeable battery. Although the battery-assisted energy harvesting system cannot totally solve the issue of battery replacement, this solution can reduce the frequency of battery replacement and realize self-charging for the rechargeable battery. Thus, the battery-assisted energy harvesting system can aggressively prolong battery life compared with conventional battery-powered IoT nodes.

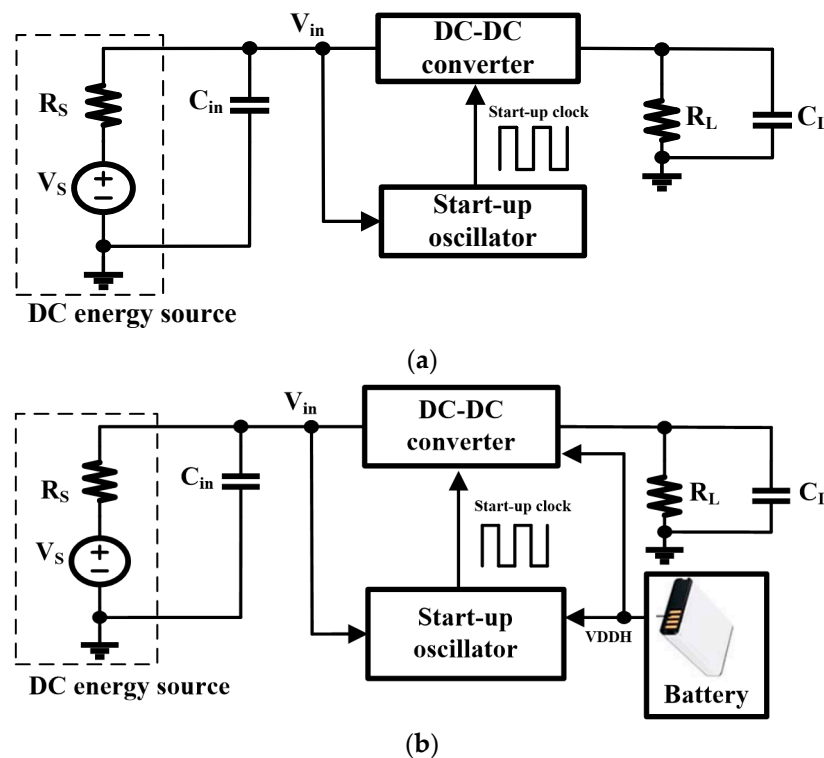


Figure 1. General categories for energy harvesting systems: (a) battery-less energy harvesting system [2–12]; (b) battery-assistance energy harvesting system [13,14].

One of the main issues for both battery-less energy harvesting systems and battery-assistance energy harvesting systems is how to activate the whole system when the input voltage is not enough. This application scene is the most common mode, as the voltage generated by the surrounding sources is low and unstable. Thus, how to achieve a low voltage cold start-up has attracted extensive research over the past few years [2–12]. Several techniques have been reported to solve this issue, which can be divided into four categories: i.e., the mechanical method [2], the transformer-based method [3], the inductor-based method [4], and the fully integrated method [5–12]. Although the first three methods can realize an extremely low cold start voltage, usually below 50 mV, it is difficult to integrate the core devices with other circuits in one die. Thus, it not only makes the cost increase but also enlarges the form factor. To achieve a fully integrated solution, a cold start-up scheme based on a ring oscillator is a kind of fully integrated solution and has attracted massive research [5–12].

To ensure that the cold start-up ring oscillator can achieve oscillation under a low voltage, several techniques have been proposed from circuit level [5–12,15]. However, the minimal cold start-up voltage in these works is still not enough to achieve a start-up below 30 mV. In this paper, a low voltage start-up ring oscillator based on the proposed low voltage delay element is presented for battery-assistance DC energy harvesting systems. A high voltage (V_{DDH}) generated by the battery is employed to assist the oscillation of the cold start-up ring oscillator under an extremely low input voltage (V_{in}).

The rest of the paper is organized as follows. Section 2 is a literature review of the published low voltage delay element, which can be employed in the fully integrated cold start-up ring oscillator. Section 3 illustrates the proposed low voltage delay element. Section 4 presents the post-layout experimental results and a comparison with prior arts. Finally, a conclusion is drawn in Section 5.

2. Literature Review

This section includes three subsections. First, the basics of an inverter are presented in Section 2.1, such as the voltage transfer curve (VTC) and DC gain. Then, the fundamental limit on the power supply of the low voltage delay element is discussed in Section 2.2. Finally, an overview of the low voltage delay element for cold start-up ring oscillators is summarized in Section 2.3.

2.1. VTC and DC Gain of Inverters

For a general inverter, the VTC is used to describe the characteristic between the input node and the output node. When the input voltage is low, as the pull-down transistor is shut down and the pull-up transistor is turned on, the output voltage is high. Similarly, the output voltage is low when the input voltage is high, as indicated in Figure 2a. However, with a reduction in the supply voltage (VDD), the VTC exhibits a gradual flattening trend, like the curve of VDD = 20 mV in Figure 2a. This trend is caused by the deteriorating ratio between the on-current and the off-current, i_{on}/i_{off} . With the reduction of VDD, i_{on} aggressively declines. When i_{on} is less than i_{off} , the output voltage cannot flip with the change of input voltage and a flattening trend is formed.

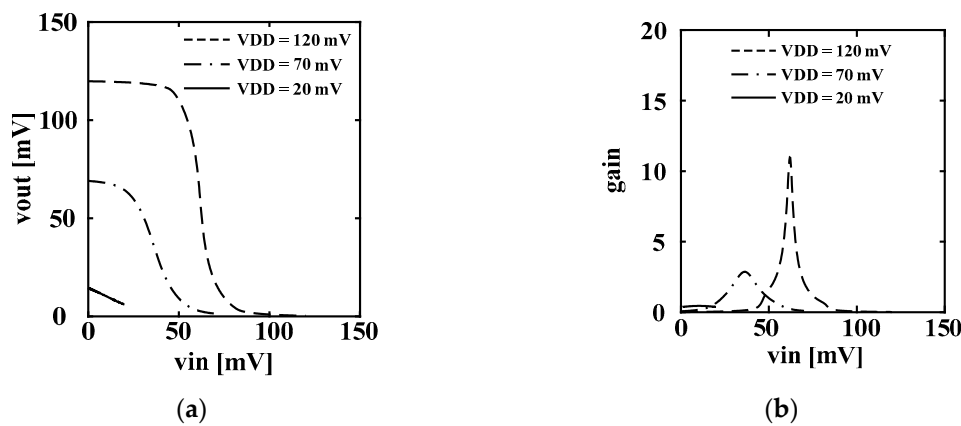


Figure 2. Voltage transfer curve (VTC) and gain curves of an inverter with a reduction in supply voltage: (a) VTC; (b) DC gain curves.

The DC gain of an inverter can be obtained by taking the derivative of the curves in Figure 2a, as shown in Figure 2b. The maximum DC gain occurs at the moment when the output voltage flips. This can be interpreted as follows. When the input voltage is low, the output is high as the pull-up transistor is on, so the DC gain is zero. Similarly, when the input voltage is high, the output is low as the pull-down transistor is on, so the DC gain is also zero. At the moment when the output voltage flips, the DC gain A of a general inverter can be written as in (1):

$$A = \frac{g_{mN} + g_{mP}}{g_{dsN} + g_{dsP}} \quad (1)$$

where g_{mN} and g_{mP} are the small-signal transconductance of N-type MOS (NMOS) and P-type MOS (PMOS) transistors, respectively. g_{dsN} and g_{dsP} are the small-signal output conductance of the NMOS and PMOS transistors, respectively. With the reduction of VDD, the DC gain aggressively declines, as indicated in Figure 2b. When VDD is 20 mV, the DC gain is much smaller than 1.

2.2. Fundamental Limit on Minimum Supply Voltage

According to the analysis in Section 2.1, a minimal supply voltage exists when an inverter loses its binary switching capability. Many research papers [15–20] have focused on this issue. Based on Meindl's fundamental limit [16], this minimum operation voltage V_{dd_limit} is given as follows in (2):

$$V_{dd_limit} = 2V_T \times \ln[1 + S_S / (\ln 10 \times V_T)] \quad (2)$$

where V_T is the thermal voltage and S_S is the sub-threshold slope.

To obtain a more intuitive understanding, S_S is affected by the channel depletion region capacitance per unit area (C_d) and the gate oxide capacitance per unit area (C_{ox}), as indicated in (3):

$$S_S = \ln 10 \times V_T \times (1 + C_d / C_{ox}) \quad (3)$$

For a more advanced process node, as the depth of the gate oxide layer is thinner, C_{ox} is larger and the corresponding S_S is smaller. Thus, the circuits implemented in an advanced process node can work under a lower supply voltage regardless of the leakage current. It is worth noting that, for a certain process node, C_{ox} is fixed and V_T is a physical constant. Thus, only C_d is controlled by the biasing voltage.

However, the leakage current is inevitable. Thus, with the reduction of VDD, the swing of the output signal will be deteriorated due to the decreased ratio of i_{on}/i_{off} . For the large signal analysis of a general inverter, during the low-to-high transition at the output node, the final output voltage (V_H) is decided by the leakage current. Assume that the on-resistance of PMOS is R_{on} , which is inversely proportional to the on-current i_{on} , and the off-resistance of NMOS is R_{off} , which is inversely proportional to the off-current i_{off} . Thus, V_H at a fully charged condition can be expressed as in (4):

$$V_H = \frac{R_{off}/R_{on}}{1 + R_{off}/R_{on}} \times V_{DD} \propto \frac{i_{on}/i_{off}}{1 + i_{on}/i_{off}} \quad (4)$$

Similarly, during the high-to-low transition at the output node, the final voltage (V_L) at a fully discharged condition is obtained as in (5):

$$V_L = \frac{1}{1 + R_{off}/R_{on}} \times V_{DD} \propto \frac{1}{1 + i_{on}/i_{off}} \quad (5)$$

According to (4) and (5), it is obvious that the swing of the output voltage ($V_{swing} = V_H - V_L$) is influenced by the ratio of R_{off}/R_{on} or i_{on}/i_{off} . Larger R_{off}/R_{on} or i_{on}/i_{off} indicates an increased V_{swing} . However, with the reduction of VDD and the scaling down of process, both R_{off} and i_{on} decrease, and both R_{on} and i_{off} increase; thus, R_{off}/R_{on} or i_{on}/i_{off} becomes smaller. Finally, V_{swing} also shrinks.

Therefore, to maximize the output voltage swing, R_{off}/R_{on} or i_{on}/i_{off} is required to maximize. As the influence of R_{off}/R_{on} and i_{on}/i_{off} on V_{swing} is almost equivalent, i_{on}/i_{off} is used in the following discussion to simplify the analysis.

2.3. Overview of Low-Voltage Delay Elements for Cold Start-Up Ring Oscillator

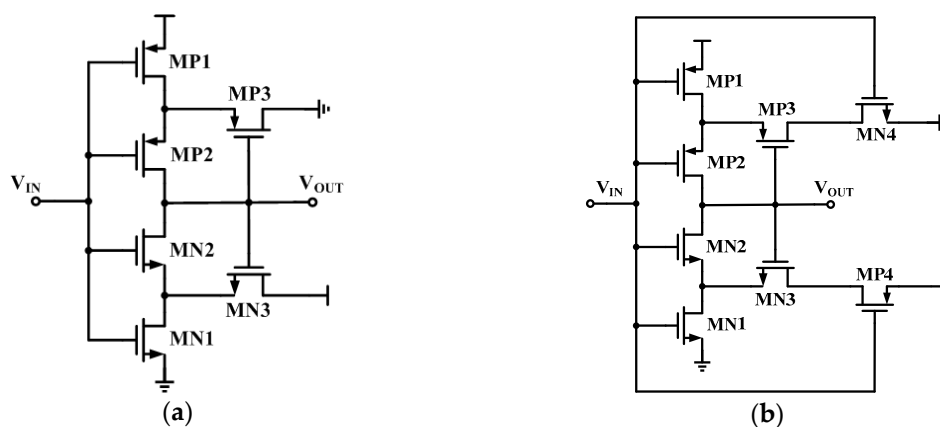
To achieve a fully integrated cold start-up scheme for DC energy sources (i.e., thermal and light sources), several low-voltage delay elements for cold start-up ring oscillators have already been reported [5–12,15]. Table 1 summarizes these works and the reported cold start voltage. The reported minimal cold start voltage in the literature is 36 mV [15]. Compared with other non-fully integrated solutions [2–4], this minimal cold start voltage is still not enough to meet a practical situation.

Table 1. Summary of the cold start-up ring oscillator.

Ref.	Process (nm)	Cold Start Voltage (mV)
[5]	65	95
[6]	180	70
[7]	180	60
[8]	65	68 ^A /150 ^B /210 ^C
[9–12]	180	37 ^B /57 ^C
[15]	180	36 ^B

^A Schematic-level simulation; ^B post-layout simulation; ^C measurement.

As shown in Figure 3a, to ensure the low voltage operation of an inverter, a Schmitt trigger (ST) logic inverter has been proposed [21–24]. The output signal was used to steer out the leakage current from the signal path so that the voltage between the drain and the source V_{ds} was minimized to zero. Thus, the leakage current caused by V_{ds} was reduced and the signal swing was improved. However, as the output voltage V_{out} always lagged the change of input voltage V_{in} , the state change of the internal nodes in this structure was suppressed due to the feedback signal. To solve this issue, a new delay element, termed selective ST logic, was proposed [6], as presented in Figure 3b. Transistors MN4 and MP4 were inserted and controlled by the input signal, so that the feedback signal would be disabled when the input signal changed. With this configuration, the drawback of the ST logic inverter was overcome. In Figure 3c, the authors [8] proposed a stacked inverter which removed the feedback path and corresponding transistors MN3 and MP3 in Figure 3b, so that both the pull-up transistor MP2 and pull-down transistor MN2 were floated by two input signal controlled inverters between the supply rail and the ground rail. To obtain a better i_{on}/i_{off} at a lower supply voltage, two stacked inverters were used to replace the two input signal controlled inverters in Figure 3c, as indicated in Figure 3d [9]. Although a larger output swing was achieved with this configuration, the loading condition of the input signal also increased and the switching speed was sacrificed. To further enhance the performance of the ultra-low voltage delay element, a novel delay element is proposed in the next section, where a voltage level shifter (VLS) is inserted to assist the body biasing. Thus, the high voltage from the battery in the battery-assistance DC energy harvesting system is used to bias the body, and the threshold voltage of the core inverter is dynamically adjusted with the input signal. Finally, the charging current is enhanced and i_{off}/i_{on} is improved.

**Figure 3.** Cont.

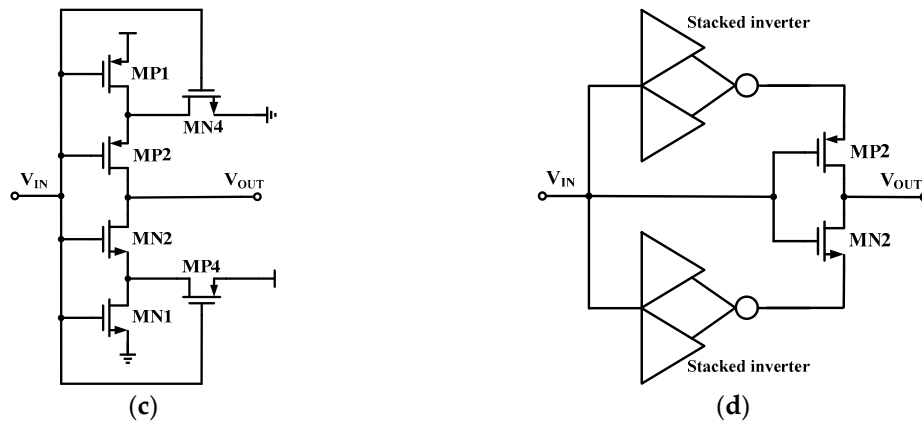


Figure 3. Circuit of already published delay elements: (a) Schmitt trigger inverter [21]; (b) selective Schmitt trigger inverter [6]; (c) stacked inverter [8]; (d) redundant inverter [9].

3. Proposed Low Voltage Delay Element

The proposed low voltage delay element is presented in detail in this section. The abovementioned works [6,8,9,21] focus on the fact that the leakage current can be declined by reducing the voltage difference between the source and the drain of transistors when they are off. However, i_{on}/i_{off} can also be enhanced by increasing i_{on} . To enhance i_{on} when the transistors are on, the threshold voltage is dynamically adjusted with the change of input signal. As shown in Figure 4a, M3 and M4 are replaced by deep n-well (DNW) transistors and their bodies are connected together with the output of VLS. Meanwhile, the input of VLS is controlled by the input signal and VLS is powered by VDDH. Thus, with the help of VLS, the input signal is shifted into a high voltage domain and higher voltage swing is obtained to bias the body of the DNW transistors. Finally, the threshold voltage of the DNW transistors is reduced with the input signal and the enhanced i_{on} is obtained.

However, the main issue is that the complementary phase in the low voltage domain is required for conventional VLSs. In most cases, the complementary phase is obtained through an inverter. As mentioned in Section 2.2, due to the fundamental limit on the power supply of a delay element, it is extremely difficult to obtain the complementary phase under a low VDD, such as below 30 mV. Thus, VLS without the need of a complementary phase is a preferred candidate for the proposed low voltage delay element. Accordingly, a VLS published in previous literature [25], as shown in Figure 4b, is inserted to assist the realization of the proposed low voltage delay element. The detailed description of this VLS is included in previous research [25]. When the input voltage is low, the bodies of M3 and M4 are also low and the threshold voltage of M3 is reduced, and thus i_{on} is enhanced. Similarly, when the input voltage is high, the bodies of M3 and M4 are high and the threshold voltage of M3 and M4 is increased and reduced, respectively. Finally, the leakage current through M3 becomes smaller and the discharging current through M4 becomes larger. The enhanced i_{on}/i_{off} indicates that the proposed low voltage delay element can ensure normal operation under a lower supply voltage and a wider voltage swing is obtained.

As shown in Figure 4c,d, the VTC and DC gain curve are obtained by schematic-level simulation under a typical process corner at room temperature. DC gain during the flipping moment is about 1.5, which indicates that the binary switching ability still keeps under this condition. Figure 4e presents the simulated oscillation of the 21-stage ring oscillator with the proposed delay element. Due to the improved gain, it is observed that the 21-stage ring oscillator can start and sustain oscillation under an input voltage as low as 20 mV with a typical process corner at room temperature. However, when parasitic parameters of the physical layout are extracted for a more accurate evaluation of the proposed delay element, the minimal oscillation voltage of the 21-stage ring oscillator will be deteriorated, which will be illustrated in the next section.

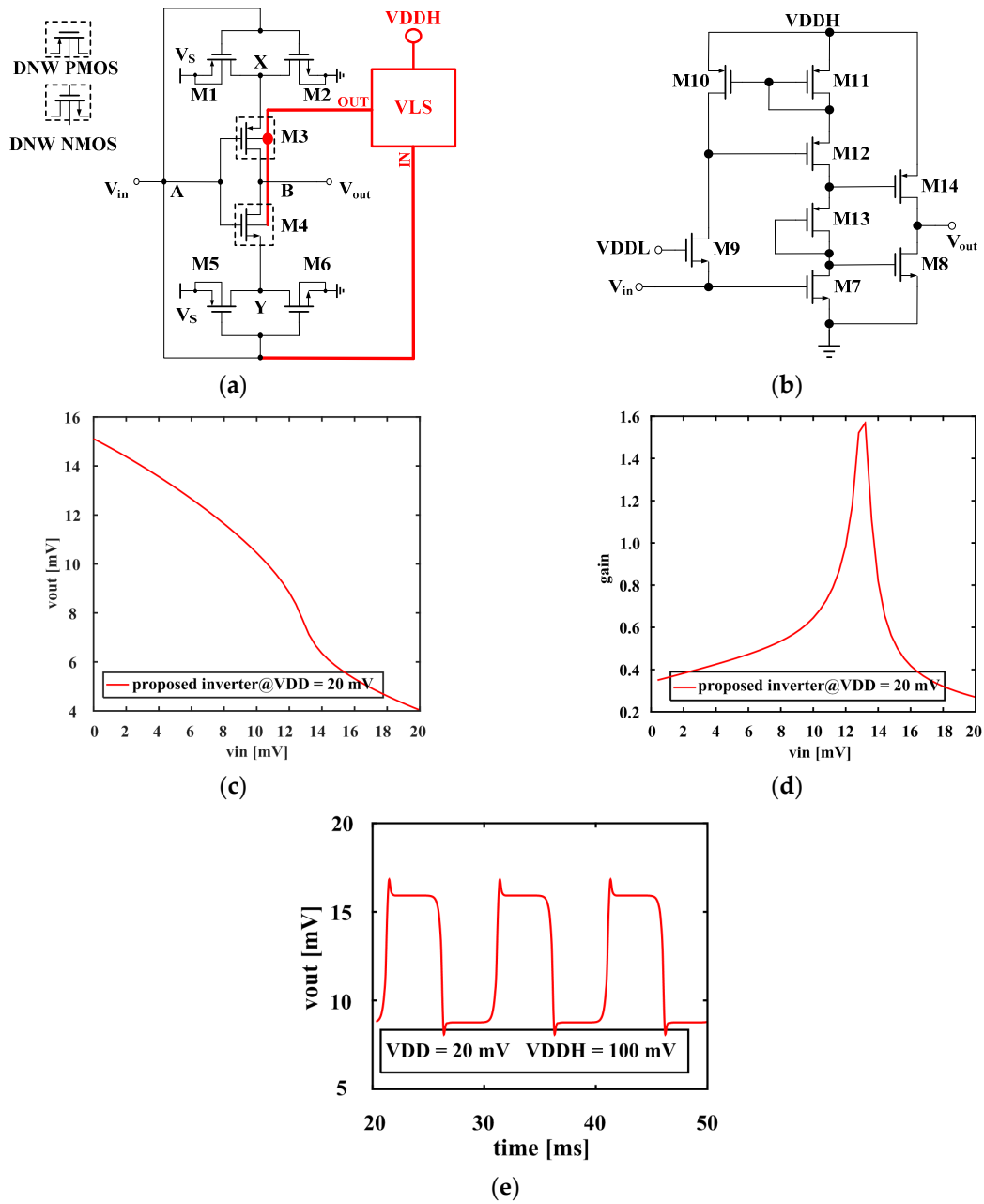


Figure 4. Circuit-level of the proposed low voltage delay element and the corresponding schematic-level simulation results with high voltage (V_{DDH}) = 100 mV: (a) proposed delay element; (b) voltage level shifter (VLS) reported in previous literature [25]; (c) VTC under power supply voltage (V_{DD}) = 20 mV; (d) DC gain under V_{DD} = 20 mV; (e) simulated oscillation of 21-stage ring oscillator with the proposed delay element under V_{DD} = 20 mV.

4. Layout and Post-Layout Experimental Results

In this section, the post-layout experimental results are presented. First, the size and the layout of the proposed low voltage delay element for the cold start-up ring oscillator are presented in Section 4.1. Next, the post-layout simulation of the proposed low voltage delay element is shown in Section 4.2. Finally, the post-layout experimental results of the cold start-up ring oscillator based on the proposed low voltage delay element are illustrated in Section 4.3.

4.1. Layout of Ring Oscillator

To evaluate the performance of the proposed low voltage delay element, a 21-stage cold start-up ring oscillator based on the proposed delay cell, which is the minimal system, was implemented in a standard 180 nm CMOS process. The dimension of the transistors in the proposed delay element is listed in Table 2.

Table 2. Transistor dimensions of the proposed delay element.

Transistor	Width (μm)	Length (μm)	Transistor	Width (μm)	Length (μm)
M1	2.28	0.25	M8	0.22	0.18
M2	1.80	0.60	M9	0.22	0.18
M3	3.80	0.25	M10	0.22	0.18
M4	1.80	0.60	M11	0.22	0.18
M5	0.76	0.25	M12	0.22	0.18
M6	5.58	0.60	M13	0.22	0.18
M7	0.22	0.18	M14	0.22	0.18

The physical layout of the cold start-up ring oscillator is shown in Figure 5, which occupies an area of $290\ \mu\text{m} \times 90\ \mu\text{m}$, which is much less than the cold start-up scheme based on LC oscillators and off-chip inductors. Every transistor is enclosed by a guard ring considering the reliability.

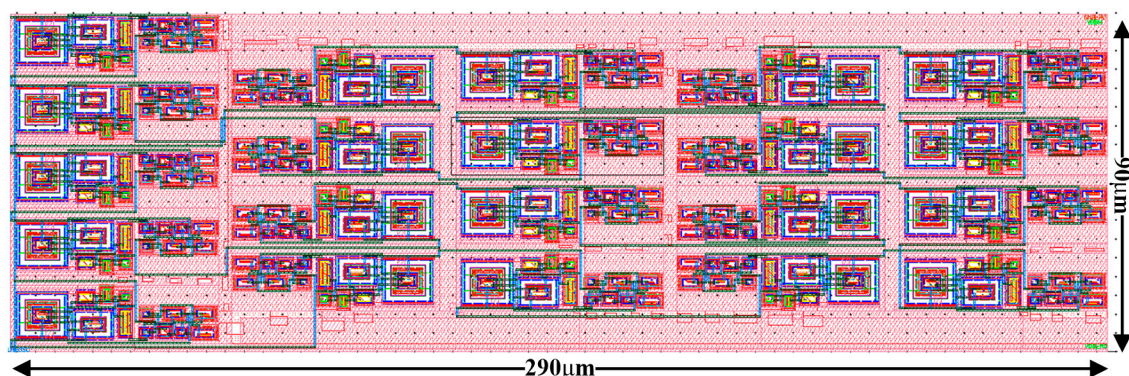


Figure 5. Physical layout of the cold start-up ring oscillator with 21 stages based on the proposed delay element.

The post-layout experimental validation was conducted on a Cadence Spectre simulator. Calibre xRC was used to extract the parasitic capacitors, resistors, and diodes in the physical layout.

4.2. Post-layout Experimental Results of Proposed Delay Element

To obtain the VTC of the proposed low voltage delay element, a DC sweep of the input voltage was conducted in Cadence and the output voltage was observed. Meanwhile, the DC gain was obtained from the VTC. As shown in Figure 6a,b, the VTC and DC gain of the proposed delay element was presented as under $V_{DD} = 24\ \text{mV}$. Figure 6c,d indicate the VTC and DC gain as under $V_{DD} = 30\ \text{mV}$. It is obvious to observe that the DC gain becomes larger with the increase of V_{DD} . As indicated in Figure 6e,f, the VTC and DC gain comparison under $V_{DD} = 40\ \text{mV}$ between the proposed delay element and the stacked inverter previously reported [8] is shown. It features a wider output voltage swing. A 191.7% improvement in DC gain was achieved compared with the stacked inverter.

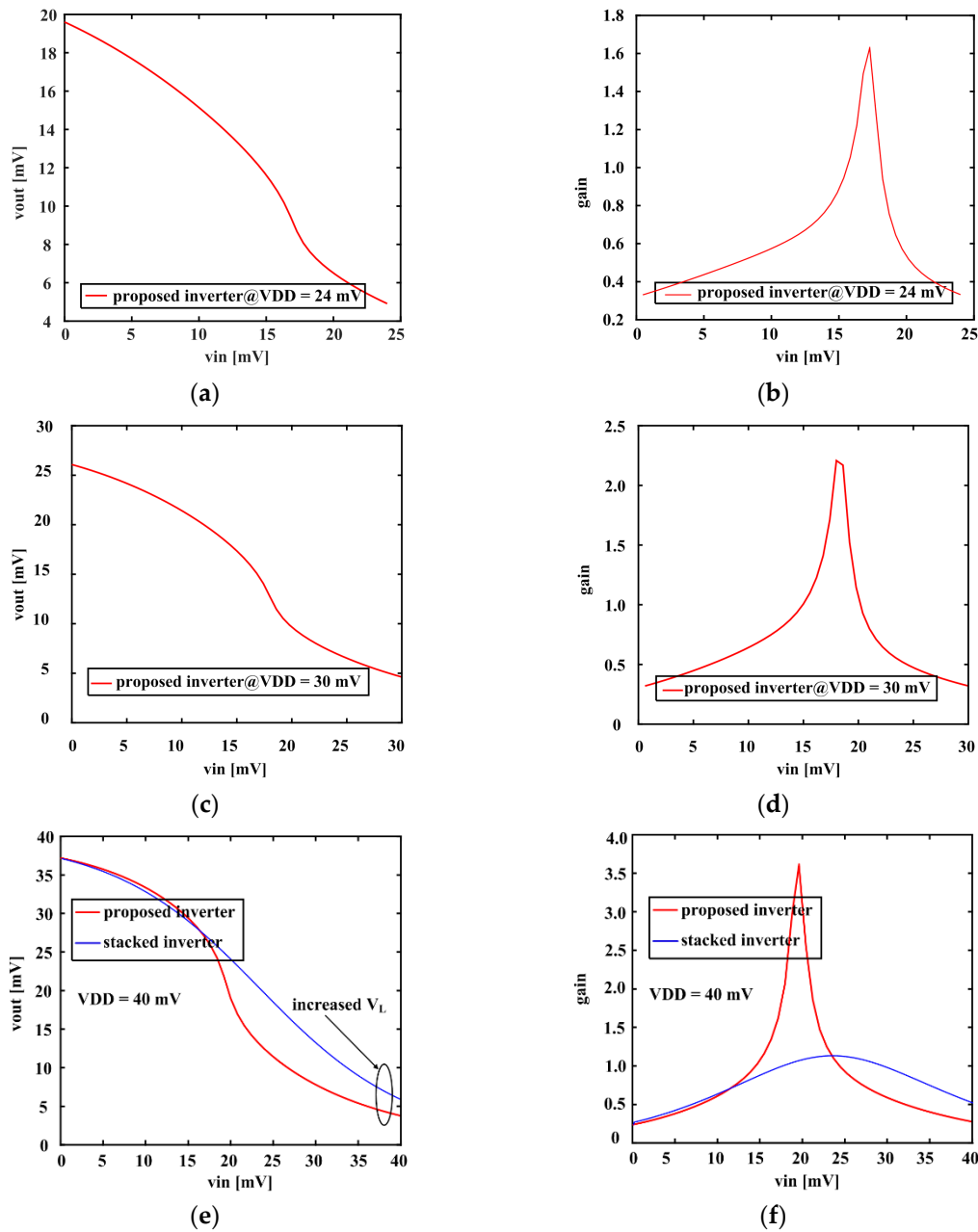


Figure 6. Post-layout experimental results of VTC and DC gain under different VDD with $V_{DDH} = 100$ mV: (a) VTC under $V_{DD} = 24$ mV; (b) DC gain under $V_{DD} = 24$ mV; (c) VTC under $V_{DD} = 30$ mV; (d) DC gain under $V_{DD} = 30$ mV; (e) VTC comparison between the proposed delay element and the stacked delay element; (f) gain comparison between the proposed delay element and the stacked delay element.

4.3. Post-Layout Experimental Result Comparison of Ring Oscillator with Two Different Delay Elements

A post-layout transient experiment was conducted to validate the proposed delay element by the minimal system (cold start-up ring oscillator) under different VDD. The accuracy of the transient analysis was set as conservative with the max step of $0.1 \mu\text{s}$.

Figure 7 shows the simulated cold start-up ring oscillator based on the proposed low voltage delay element and comparison with the stacked inverter based ring oscillator. As shown in Figure 7a, in contrast to the schematic-level simulation presented in Figure 4e, the cold start-up ring oscillator cannot oscillate under $V_{DD} = 23$ mV and $V_{DDH} = 100$ mV at a typical corner with room temperature; and Figure 7b shows that the oscillation starts under $V_{DD} = 24$ mV and $V_{DDH} = 100$ mV. Under

$V_{DD} = 30$ mV and $V_{DDH} = 100$ mV, the cold start-up ring oscillator based on the proposed delay element can still sustain oscillation, as shown in Figure 7c. A comparison with the stacked inverter based ring oscillator is shown in Figure 7d. It indicates that a 55% improvement in output voltage swing is obtained under $V_{DD} = 40$ mV.

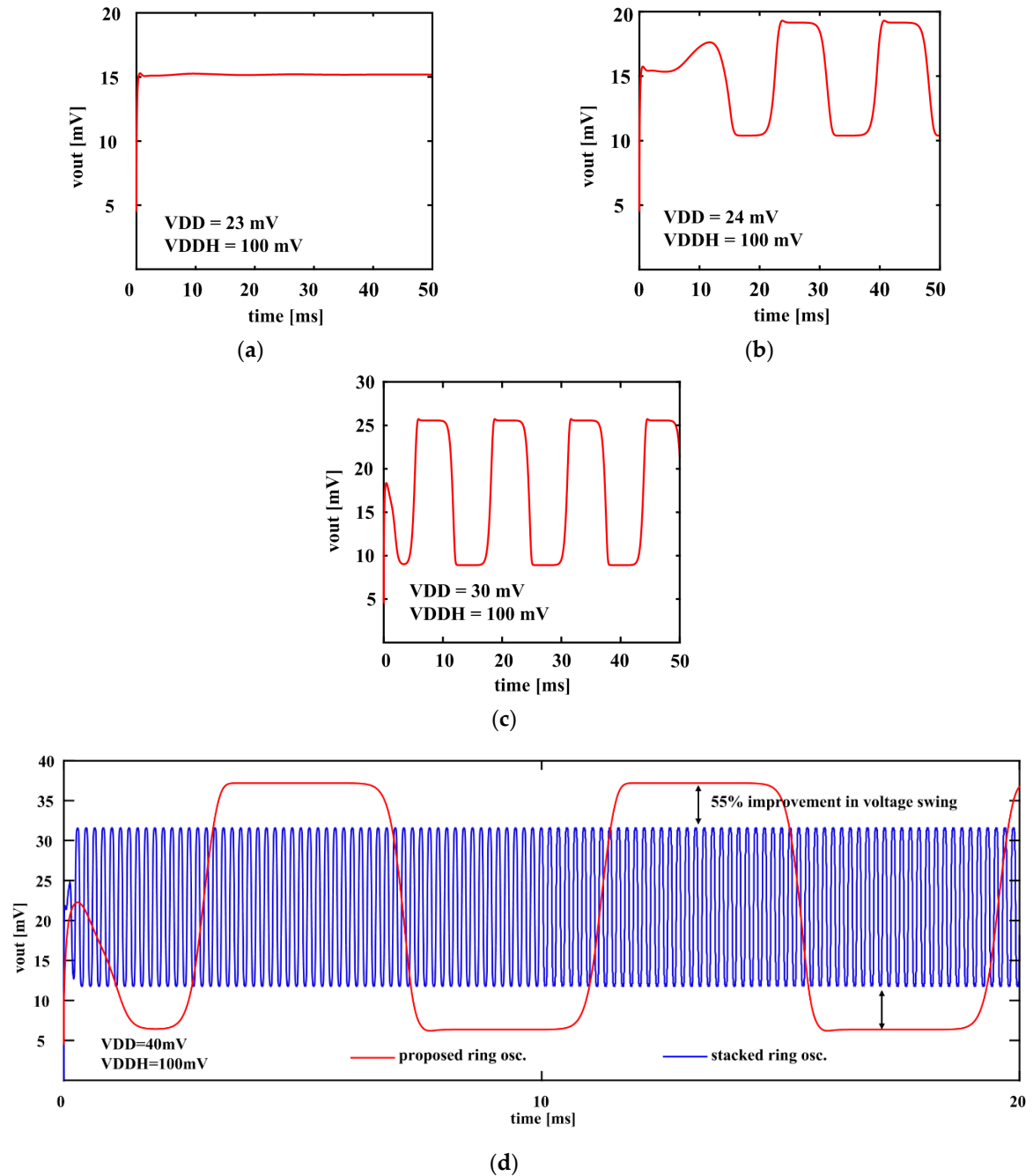


Figure 7. Experimental results of the proposed cold start-up ring oscillator and the stacked cold start-up ring oscillator: (a) post-layout transient simulation with $V_{DD} = 23$ mV and $V_{DDH} = 100$ mV at a typical corner under room temperature; (b) post-layout transient simulation with $V_{DD} = 24$ mV and $V_{DDH} = 100$ mV at a typical corner under room temperature; (c) post-layout transient simulation with $V_{DD} = 30$ mV and $V_{DDH} = 100$ mV at a typical corner under room temperature; (d) post-layout transient simulation with $V_{DD} = 40$ mV and $V_{DDH} = 100$ mV at a typical corner under room temperature.

Figure 8 presents the output swing histogram of MC simulation for the cold start-up ring oscillator based on the proposed low voltage delay element under different VDD from 100 samples. As indicated in Figure 8a, the MC simulation result indicates that the oscillation may fail with the consideration of the process variation. However, with the increase of VDD, the failed cases decline and the normalized standard deviation (σ/μ) becomes smaller, as shown in Figure 8b,c. In particular for VDD = 40 mV (Figure 8c), the failed cases almost disappear.

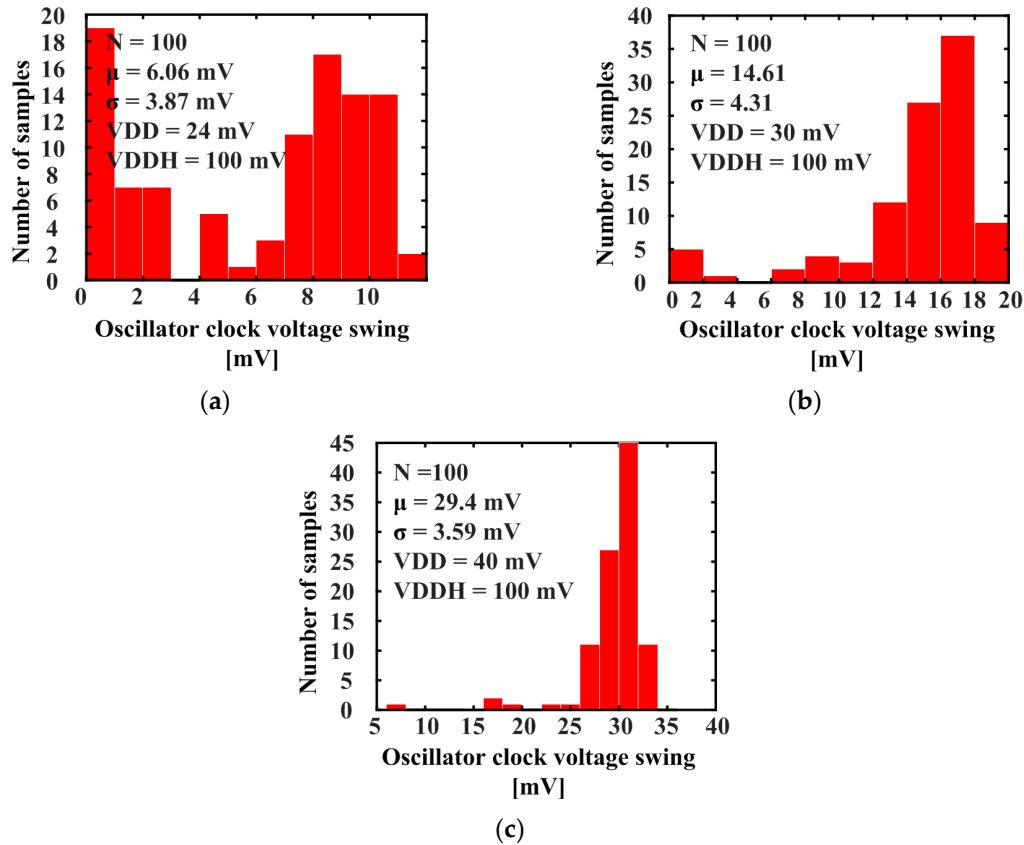


Figure 8. Oscillator output swing histogram based on MC simulations with proposed low voltage delay element: (a) MC simulation results under VDD = 24 mV and VDDH = 100 mV at room temperature; (b) MC simulation results under VDD = 30 mV and VDDH = 100 mV at room temperature; (c) MC simulation results under VDD = 40 mV and VDDH = 100 mV at room temperature.

Table 3 shows a performance comparison of the cold start-up ring oscillator based on the proposed delay element with previous works. Compared with other non-fully integrated schemes [2–4], the cold start-up voltage of the proposed solution is close to the cold start-up voltage of the LC-based oscillator previously reported [4]. Among the ring oscillators from the aspect of simulation results [9,10], the proposed solution obtains the minimal cold start-up voltage. Compared to a previous study [15] using body dynamical control to achieve a low voltage ring oscillator in a cold start-up minimal system, a VLS is inserted in each delay element to assist the body control in this paper. As the VLS can transfer the oscillation waveform in the low voltage domain into the oscillation waveform in the high voltage domain, a wider body dynamical control range is thus obtained to bias the body of the corresponding delay element in the low voltage ring oscillator. Although the proposed solution in this paper requires an extra high power supply (VDDH) to realize a wider body dynamical control range, it can realize a fully integrated cold start-up ring oscillator with the minimal cold start-up voltage.

Table 3. Performance comparison with the prior works.

Ref.	Year	Process (nm)	Oscillator Type	Start-Up Technique	Start-Up Voltage (mV)	Off-Chip Components
[2]	2010	350	Mechanical switch	Mechanical motion	35 ²	1C + 1L + 1S
[3]	2012	130	Transformer based	White noise	40 ²	1T + 4C + 2D
[4]	2013	65	LC based	LS osc.	22 ¹	2L + 1C
[5]	2011	65	Ring	Body fixed control	95 ²	-
[6]	2016	180	Ring	Schmitt trigger ring osc.	70 ²	-
[8]	2018	180	Ring	Stacked inverter based	57 ²	-
[9]	2018	65	Ring	ring osc.	150 ¹	-
[10]	2018	180	Ring	ring osc.	37 ¹	-
[15]	2020	180	Ring	Stacked inverter based ring osc. with body dynamical control	36 ¹	-
This work	2020	180	Ring	VLS assistance ring osc.	24 ¹	-

¹ Simulation results; ² measurement results; “L”, “C”, “S”, “D” and “T” indicate inductor, capacitor, mechanical switch, diode, and transformer, respectively.

5. Conclusions

In this paper, we propose an improved delay element for cold start-up ring oscillators, which can be employed in battery-assistance DC energy harvesters: for example, a battery-assistance thermoelectric energy harvesting system in wearable devices; as the temperature difference between the skin and the ambient environment is only 1–2 °C, the generated input voltage for the energy harvester is only 25–50 mV in most cases. By inserting a VLS to achieve dynamic control of the transistors’ threshold voltage with a higher voltage swing, a cold start-up ring oscillator with this proposed delay element can oscillate under a lower supply voltage as i_{on} is aggressively enhanced. When considering the parasitic parameters of the physical layout, the post-layout experimental results show that the cold start-up ring oscillator with 21 stages of the proposed delay element can maintain oscillation under $V_{DD} = 24$ mV with a typical process corner at room temperature. Post-layout MC experimental results from 100 samples indicate that wider output voltage swing is obtained compared with other reported cold start-up ring oscillators. Thus, with the assistance of VLS, the cold start-up circuit constituted by the proposed delay element can enable that the whole energy harvesting system scavenges energy from sources even under a low input voltage. The proposed scheme features huge potential and is valuable for future battery-assistance IoT nodes and body-worn applications.

Author Contributions: Z.X., Z.W. and J.W. organized this work. The idea was proposed by Z.X. The pre-simulation was conducted by Z.X. The layout and post-simulation were achieved by Z.W. The manuscript was written and edited by Z.X. The funding was provided by J.W. J.W. also supervised and provided guidelines through the whole process of this work. All authors have read and agreed to the published version of the manuscript.

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