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Review

Review on Short-circuit Current Analysis and Suppression Techniques for MMC-HVDC Transmission Systems

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Abstract: The modular multilevel converter (MMC) has been widely adopted in high voltage direct current (HVDC) transmission systems due to its significant advantages. MMC-HVDC is developing towards multi-terminal direct current (MTDC) power grid for reliability enhancement. However, there exist a huge amplitude and a steep rise in fault current due to the low impedances of DC lines and MMCs, which threaten the security and reliability of the DC power grids. It is necessary to restrain the DC short circuit current in order to ensure the safe and stable operation of DC power grids. This paper gives a comprehensive review and evaluation of the proposed DC short-circuit current analysis and suppression techniques used in MMC-based MTDC power girds, in terms of MMC modeling, short circuit calculation, and suppression method. In addition, future trends of countermeasures to short circuit current in MMC-based MTDC power grids are also discussed.

Keywords: MMC-HVDC; DC power grid; DC short circuit current; MMC modelling techniques; short circuit current calculation method; short circuit current suppression method

1. Introduction

With the development of global power interconnection, the requirements of long-distance power transmission and asynchronous power grids' interconnection are increasing. In order to meet these requirements, high-voltage direct current (HVDC) technology is playing a significant role in future global power interconnection [1]. Among all of the converter topologies, the modular multilevel converter (MMC), which was first introduced in 2001, is considered to be the most promising converter topology for HVDC transmission systems [2] due to its advantages of no commutation failure, flexible active and reactive power control, low switching operational frequency, and high output waveform quality, etc. [3].

MMC-HVDC is widely applied in renewable energy integration [4], the construction of DC grids, connection to weak power systems, large city power supply, asynchronous power grids' interconnection [5], and so on [6]. Presently, there are more than thirty MMC-HVDC projects in operation or under construction throughout the world, some of which commissioned in recent years are listed in Table 1. With the ability of changing power flow direction without reversing the voltage polarity, MMC-HVDC is gradually developing towards a multi-terminal direct current (MTDC) power grid [7]. The increasing terminal number of MMC-HVDC systems in China has verified this trend. By providing the possibility of interconnections between asynchronous power systems and various renewable energy resources [8], MMC-based MTDC power grids can potentially enhance the reliability of the AC and DC systems and improve the flexibility and economy of power

dispatching [7]. It is playing an important role in future development of smart grids and the global power interconnection [9–14].

Table 1. Modular multilevel converter-high voltage direct current (MMC-HVDC) projects in operation or under construction world wide.

Commissioning Year	Name	Location	Terminals	Capacity, MW	DC Voltage, kV
2020	Zhangbei	China	4	3000	±500
2019	BorWin3	Germany	2	900	±320
2016	Chongqing-Hubei	China	2	2500	±420
2016	Luxi	China	2	1000	±350
2015	Helwin2	German	2	690	±320
2015	Xiamen	China	2	1000	±320
2014	Zhoushan	China	5	1000	±200
2013	Nan'ao	China	3	200	±160
2011	Nanhui	China	2	18	±30
2010	Trans Bay Cable	America	2	400	±200

However, the application of MMC-based MTDC power grids brings several technical challenges. One major challenge is the massive DC short-circuit fault currents. When compared with traditional AC systems, the impedances of DC lines and MMCs are much smaller. Once DC short-circuit faults occur, the capacitors in the submodules of MMCs discharge immediately and large short circuit currents are fed to the fault point through the DC transmission lines and the power electronic devices [13]. A typical DC pole-to-pole short circuit of an MMC-based MTDC power grid is shown in Figure 1. It can be seen from Figure 1 that the short-circuit current rapidly rises within a few milliseconds with a peak value of more than 10kA after the DC short circuit fault occurs. DC current breakers are not commonly available for interrupting short-circuit currents due to the absence of a natural current zero crossing in DC systems, and they have very limited ratings for HVDC applications [15]. It is necessary to analyze and suppress the short-circuit current in order to ensure that the DC current breakers can isolate the fault line.

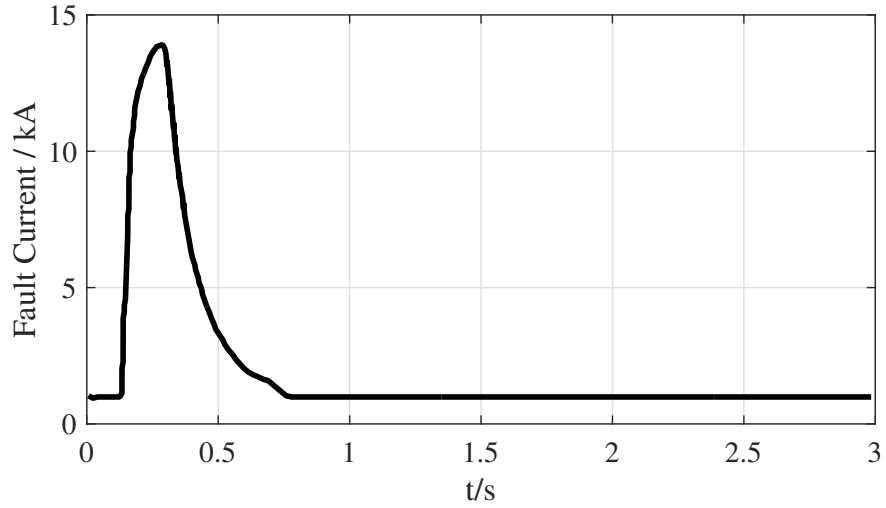

Figure 1. A typical DC pole-to-pole short circuit of MMC-based multi-terminal direct current (MTDC) power grid.

Modelling, short-circuit current calculation methods, and suppression methods are essential in the investigation of countermeasures to the DC short-circuit current in MMC-based MTDC power grids. This paper gives a comprehensive review and evaluation of short-circuit current analysis and countermeasures in MMC-based MTDC power grids. The main contributions of this paper are:

first, this paper offers an up-to-date review of the state of MMC-HVDC modelling; second, the existing MMC-based MTDC power grid short-circuit current calculation method is introduced; and third, this paper classifies the existing short-circuit current suppression methods, especially the latest achievements in this area. The analysis results and discussions show the shortcomings in the current research and provide future research directions that are based on this work.

This paper is organized, as follows: Section 2 makes a brief introduction of MMC-HVDC; Section 3 presents the classification of MMC-HVDC modeling methods; Section 4 introduces several short circuit current calculation methods, and classifies the existing short-circuit current suppression methods for MMC-based MTDC power grids; and, Section 5 concludes this paper and discusses future research trends that are based on this work.

2. A Brief Introduction of MMC

Figure 2a shows a general structure of a three-phase MMC. Each bridge arm of the MMC consists of an arm reactor L_{arm} and N series-connected sub-modules (SMs). R_{arm} is the equivalent resistance of the bridge arm. U_{dc} is the DC voltage of MMC. The multilevel output voltage is generated by controlling the number of inserted SMs in the bridge arm.

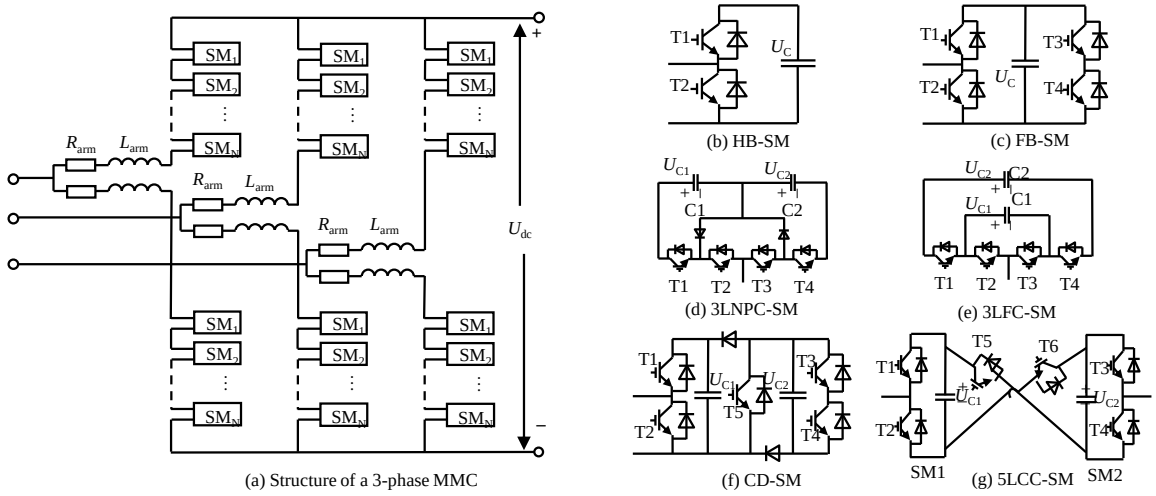

Figure 2. Structure of a three-phase MMC with various sub-modules (SMs).

Different topologies of SMs for MMCs have been proposed and investigated, including the half-bridge (HB), the full-bridge (FB), the clamp-double (CD). and the three-level/five-level cross-connected (3LCC/5LCC) SMs [16–18] as shown in Figure 2b–g. These SM topologies are available for the MMC structure that is shown in Figure 2a. The features of each topology are summarized, as follows:

- HB circuit: the HB-SM is inserted or bypassed by turning on T_1 or T_2, respectively. When the SM is switched-on or in inserted state, its output voltage equals to its capacitor voltage U_c. Otherwise, when the SM is switched-off or in bypassed state, the output voltage is 0 [18].
- FB circuit: the operation state of FB-SM is determined by the switching states of the four switches T_1 to T_4. When in switched-on/inserted state, the output voltage equals to the capacitor voltage u_c. Otherwise, it is 0. The costs of an MMC based on the FB-SMs are higher than that of an MMC based on the HB-SMs due to the increased number of switches in each SM [16].
- CD circuit: a CD-SM consists of two HB-SMs, two additional diodes, and one extra integrated gate bipolar transistor (IGBT) with its anti-parallel diode. During normal operation, the switch S_5 is always in conduction state and the dynamics of CD-SM are equivalent to two series connected HB-SMs [16].
- 3LCC circuit: there are two different types of 3LCC-SM, three level neutral-point-clamped (NPC), and three-level flying capacitor (FC). For a three-level FC-SM, its power losses are similar with a

HB-SM. The power losses of NPC-SM are higher than the HB-SM and lower than the FB-SM [3]. The 3LCC-SM based MMC is not very attractive from the perspective of manufacturing and control [17].

- 5LCC circuit: there are two HB-SMs connected back-to-back by two extra IGBTs with their anti-parallel diodes in a 5LCC-SM. Its power losses are the same as the CD-SM [17].

Table 2 provides a comparison of different SM topologies, in terms of output voltage levels, DC short circuit fault ride through capability, and power losses. Section 4 will discuss the DC short circuit fault ride through capability of each SM topology.

Table 2. Comparison of different SM topologies.

SM Topologies	Output Voltage Level	DC Short Circuit Fault Ride through Capability	Power Losses
HB-SM	$0, u_c$	No	Low
FB-SM	$0, +u_c$	Yes	High
CD-SM	$0, u_{c1}, u_{c2}, (u_{c1} + u_{c2})$	Yes	Moderate
Three-level FC	$0, u_{c1}, u_{c2}, (u_{c1} - u_{c2})$	No	Low
Three-level NPC	$0, u_{c2}, (u_{c1} + u_{c2})$	No	Moderate
5LCC-SM	$0, u_{c1}, u_{c2}, +(u_{c1} + u_{c2})$	Yes	Moderate

There are different dynamic characteristics and operational demands for various SM topologies. It is necessary to establish the MMC model that covers different SM topologies for further dynamic investigation and fault analysis.

3. MMC-Based MTDC Power Grid Modelling Overview

An MMC-based MTDC power grid consists of MMC main circuits, MMC control systems, AC systems, and a DC system. An overview of the model of each subsection is performed in this section.

3.1. MMC Main Circuit

Detailed switch model (DSM), average value model (AVM), simplified average value model (SAVM), detailed equivalent model (DEM), and equivalent discharging model (EDM) are the major types of accurate and efficient models to represent the dynamics of the MMC main circuit under different scenarios [19]. The principles and application scenarios of each MMC main circuit model are introduced, as follows.

- DSM: in a DSM, a detailed switch is applied to present the operational times of the switching devices and the on/off-state resistances/voltages in the SMs [20]. The detailed representation requires a small simulation time step to accurately track the switching voltage edges that are essential for the preservation of various frequency components in the AC and DC waveforms. Because a large number of electrical nodes is created in DSM, it leads to huge simulation time cost. With the increasing number of SMs in MMCs, the DSM is facing a significant challenge in computation [7]. DSM is not suitable for the dynamic analysis, control design, and fault analysis for large scale DC power systems, and simplifications shall be made.
- AVM: the AVMs of MMC has been proposed to approximate system dynamics, where the switching details are not explicitly modeled and the dynamics of MMC is equivalent through using controlled voltage and current sources [18]. The relationship of the arm currents (i_p for upper bridge arm and i_n for lower bridge arm) and the capacitor voltages (u_p for the upper bridge arm and u_n for lower bridge arm) can be expressed as

$$S_p \cdot i_p = C\frac{du_{cp}}{dt}, S_n \cdot i_n = C\frac{du_{cn}}{dt} \quad (1)$$

where C is the capacitance of each submodule capacitor; and, S_p and S_n are the average switching functions of the upper and lower arms.

The upper and lower bridge arm voltages u_{p} and u_{n} are

$$u_{\mathrm{p}} = NS_{\mathrm{p}}u_{\mathrm{cp}}, u_{\mathrm{n}} = NS_{\mathrm{n}}u_{\mathrm{cn}} \tag{2}$$

The average switching function model of the MMC is composed of (1) and (2).

Ignoring the differences between the circuit parameters of MMC six bridge arms and high order circulating current components, the arm current contains a DC component that equals $I_{\mathrm{dc}}/3$; a fundamental frequency AC component equaling to $I_{\mathrm{s}}/2$; and, even-order circulating current components with an amplitude of I_{cir}. The upper and lower arm currents are presented as

$$\begin{cases} i_p = \frac{1}{3}I_{\mathrm{dc}} - \frac{1}{2}I_s \sin(\omega t + \beta_1) + I_{\mathrm{cir}} \sin(2\omega t + \beta_2) \\ i_n = \frac{1}{3}I_{\mathrm{dc}} + \frac{1}{2}I_s \sin(\omega t + \beta_1) + I_{\mathrm{cir}} \sin(2\omega t + \beta_2) \end{cases} \tag{3}$$

The real switching function of the bridge arm is a stepped waveform that indicates when SMs are inserted or out of work [21]. However, with the increasing number of SMs, the average switching function S_{p} and S_{n} can be represented by continuous waveforms:

$$\begin{cases} S_p = \frac{1}{2} - \frac{1}{2}M\sin(\omega t + \alpha) + \frac{U_{\mathrm{cir}}}{U_{\mathrm{dc}}}\sin(2\omega t + \varphi) \\ S_n = \frac{1}{2} + \frac{1}{2}M\sin(\omega t + \alpha) + \frac{U_{\mathrm{cir}}}{U_{\mathrm{dc}}}\sin(2\omega t + \varphi) \end{cases} \tag{4}$$

where M is the modulation index and α is the phase angle of the fundamental frequency component of the switching function. U_{cir} and ϕ are the amplitude and phase of a control signal generated by the circulating current suppression controllers (CCSCs).

In the AVM, although the individual capacitor voltages are not calculated, the large-scale dynamic behavior can be accurately modeled [22]. Instead, a single DC voltage is calculated, so that the AVM can use larger simulation time steps and it requires less computational resources [23]. It provides faster simulation speed and is more efficient than models that consider the detailed MMC converter topology. It has been proposed for studying the dynamics behavior of both single MMC [24,25] and DC power grids [26–29].

- SAVM: the SAVM assumes that all of the internal variables in the MMC are perfectly controlled, all submodule capacitor voltages are perfectly balanced, and second harmonic circulating currents in each phase are suppressed [22,26]. It is a simplified model that is based on the AVM by ignoring the internal circulating current dynamic process. Therefore, the average switching function can be simplified to

$$\begin{cases} S_p = \frac{1}{2} - \frac{1}{2}M\sin(\omega t + \alpha) \\ S_n = \frac{1}{2} + \frac{1}{2}M\sin(\omega t + \alpha) \end{cases} \tag{5}$$

  It is suitable for the study of large-scale MMC-based MTDC power grids and system-level controller design, as discussed in [30].
- DEM: based on the equivalent branch model of a bridge arm, a DEM of MMC is proposed in [31,32]. In the DEM, the dynamics of each SM capacitor is represented by an equivalent controlled voltage source u_{c} in series with resistance R_{c} [31]. The values of u_{c} and R_{c} are

$$\begin{cases} R_{\mathrm{c}} = \frac{\Delta t}{2C} \\ u_{\mathrm{c}}(t) = u_{\mathrm{c}}(t - \Delta t) + 2R_{\mathrm{c}}i_{\mathrm{c}}(t - \Delta t) \end{cases} \tag{6}$$

  where C is the capacitance of each SM's capacitor, Δt is the time-step for simulation, and i_{c} is the SM capacitor current. The DEM has three major assumptions: an off-state switch is equivalent to an open circuit; and on-state that is equivalent to R_{on}; $i_{\mathrm{c}}(t)$ is equal to the corresponding bridge arm current when the SM is inserted. $i_{\mathrm{c}}(t)$ is equal to 0, when the SM is passed by [32].

As a result of the aforementioned assumptions, each MMC arm can be modeled as a series connection of arm inductor L_{arm}, equivalent voltage source U_{armEQ}, and equivalent resistance R_{armEQ}. Figure 3 shows the equivalent circuit of each submodule of the MMC in DEM.

The equivalent bridge voltage can be given by

$$U_{\text{armEQ}}(t) = \sum_{i=1}^{N} U_{\text{Th}_i}(t) \tag{7}$$

where i is the index of SM; N is the number of SM in each bridge arm; and, $U_{\text{Th}_i}(t)$ satisfies

$$U_{\text{Th}_i}(t) = \begin{cases} 0 & \text{if } \text{SM}_i \text{ is off} \\ U_{\text{cEQ}_i}(t) & \text{if } \text{SM}_i \text{ is on} \end{cases} \tag{8}$$

Meanwhile,

$$R_{\text{armEQ}}(t) = N_{\text{on}} \times R_c + N \times R_{\text{on}} \tag{9}$$

where N_{on} is the number of SMs in on-state.

The DEM provides a detailed representation of SMs switching events and individual capacitor ripples. It is feasible for arbitrary number of submodules. The DEM can be applied in order to design the balancing control of the capacitor voltages in the bridge arm. It can also represent the blocked mode, which is essential for accurately describing the MMC behaviors during startup and fault conditions [31,33].

- EDM: because the capacitor discharge currents of SMs are the dominant components of the DC short-circuit current in DC power girds, MMCs are equivalent to a series RLC circuit in a EDM [13,34–36]. Figure 4 shows the structure of EDM.

The equivalent circuit parameters can be obtained from the detailed average model parameters, as follows.

$$\begin{cases} R_{\text{c}} = \frac{2(R_{\text{arm}} + \sum R_{\text{ON}})}{3} \\ L_{\text{c}} = \frac{2L_{arm}}{3} \\ C_{\text{c}} = \frac{6C}{N} \end{cases} \tag{10}$$

where R_{arm} and L_{arm} are the resistance and inductance of the bridge arms, respectively, R_{ON} is the sum of the on-state resistances of all SMs. The model that is given by (10) ignores the dynamics of MMC control systems, such as the power and voltage control [13,34], and it is suitable for DC short circuit current calculation [13,34–36].

The above-discussed models of MMC main circuit are presented in Table 3 in order to make a comparison of their features. In the table, $\surd$ indicates that the chosen technique is strongly related to the corresponding item; $\times$ indicates that the chosen technique is not related to the corresponding item.

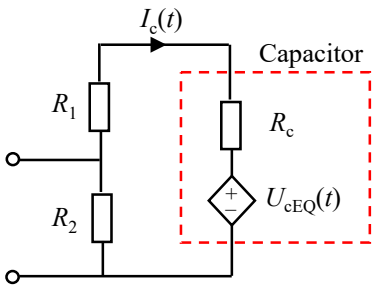

Figure 3. Detailed equivalent model (DEM) of each submodule of the MMC.

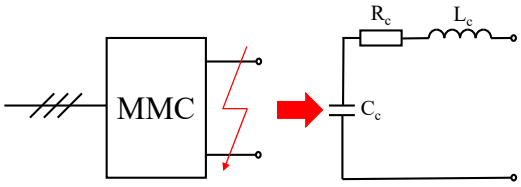

Figure 4. EDM of MMC under DC fault.

Table 3. Comparison of different MMC model.

Model	Single SM Dynamics	Control System Dynamics	Circuit Current Dynamics	System Level Analysis	Control Strategy Design	SM Level Analysis	DC Fault Analysis
DSM	√	√	√	×	×	√	√
AVM	×	√	√	√	√	×	√
SAVM	×	√	×	√	√	×	√
DEM	√	√	√	×	√	√	×
EDM	×	×	×	×	×	×	√

3.2. MMC Control Systems

Figure 5 shows a typical structure of MMC control systems. The control systems for a single MMC consist of vector current controls (VCCs), phase-lock-loops (PLLs) and CCSCs [18,24,25,37,38]. The VCCs consist of inner and outer control loops. The control modes of MMCs are determined by the outer loop control objectives that can be chosen among active/reactive power control mode, DC voltage/reactive power control mode, active power/AC voltage control mode, and DC/AC voltage control mode.

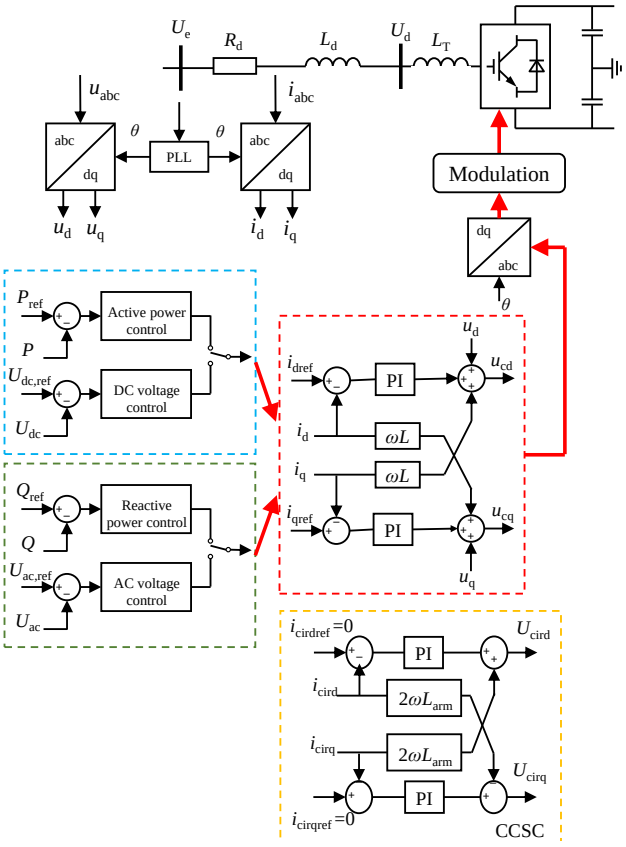

Figure 5. Structure diagram of an MMC control system.

The VCC typically adopts d–q decoupling control strategy for power or voltage, with proportion-integral (PI) controllers. as shown in Figure 5. In VCC, the d–q decoupling control strategy is realized through four PI controllers. The outputs of the VCC are the dynamic phasors of the fundamental frequency components. Therefore, a fourth-order model can be formulated in order to illustrate the dynamics of PI controllers.

$$\begin{cases} \dfrac{\mathrm{d}x_1}{\mathrm{d}t} = i_{\mathrm{dref}} - i_{\mathrm{sd}} \\ \dfrac{\mathrm{d}x_2}{\mathrm{d}t} = i_{\mathrm{qref}} - i_{\mathrm{sq}} \\ \dfrac{\mathrm{d}x_3}{\mathrm{d}t} = P_{\mathrm{ref}} - P \quad \text{or} \quad \dfrac{\mathrm{d}x_3}{\mathrm{d}t} = U_{\mathrm{dcref}} - U_{\mathrm{dc}} \\ \dfrac{\mathrm{d}x_4}{\mathrm{d}t} = Q_{\mathrm{ref}} - Q \quad \text{or} \quad \dfrac{\mathrm{d}x_4}{\mathrm{d}t} = U_{\mathrm{acref}} - U_{\mathrm{ac}} \end{cases} \tag{11}$$

where P_{ref}, Q_{ref} U_{dcref} and U_{acref} are the reference values of active power P, reactive power Q, DC voltage U_{dc}, and AC voltage U_{ac}, respectively. The reference currents i_{dref} and i_{qref} are given below.

$$\begin{cases} i_{\mathrm{dref}} = k_{\mathrm{pl}}\left(P_{\mathrm{ref}} - P\right) + k_{i1}x_3 \quad \text{or} \quad k_{\mathrm{pl}}\left(U_{\mathrm{dcref}} - U_{\mathrm{dc}}\right) + k_{i1}x_3 \\ i_{\mathrm{qref}} = k_{\mathrm{p2}}\left(Q_{\mathrm{ref}} - Q\right) + k_{i2}x_4 \quad \text{or} \quad k_{\mathrm{p2}}\left(U_{\mathrm{acref}} - U_{\mathrm{ac}}\right) + k_{i2}x_4 \end{cases} \tag{12}$$

where $k_{\mathrm{p}j}$ and $k_{\mathrm{i}j}$ are the proportional constant and integral constant of the jth PI controller, repectively.

The outputs of the MMC control system denoted by U_{cd} and U_{cq} are the dynamic phasors of the fundamental frequency components in the d–q frame, as follows

$$\begin{cases} u_{\mathrm{cd}} = u_{\mathrm{d}} - \omega L i_{\mathrm{q}} - k_{\mathrm{p3}}\left(i_{\mathrm{dref}} - i_{\mathrm{d}}\right) - k_{\mathrm{i3}}x_1 \\ u_{\mathrm{cq}} = u_{\mathrm{q}} + \omega L i_{\mathrm{d}} - k_{\mathrm{p4}}\left(i_{\mathrm{qref}} - i_{\mathrm{q}}\right) - k_{\mathrm{i4}}x_2 \end{cases} \tag{13}$$

PLL consists of two PI controllers. The dynamic of the PLL can be described as

$$\begin{cases} \dfrac{\mathrm{d}x_5}{\mathrm{d}t} = u_{\mathrm{sq}} \\ \dfrac{\mathrm{d}x_{\mathrm{pll}}}{\mathrm{d}t} = -k_{\mathrm{ppll}}U_{\mathrm{sq}} - k_{\mathrm{ipll}}x_5 \end{cases} \tag{14}$$

where k_{ppll} and k_{ipll} are the parameters of the PLL; x_5 and x_{pll} are the intermediate control variables, which denote the integral of the PI controller's error signals in PLL.

The output of the PLL is the phase signal park transforms, which can be expressed as

$$\begin{cases} \theta = \omega_0 t + x_{\mathrm{pll}} \\ \omega = \omega_0 - k_{\mathrm{ppll}}U_{\mathrm{sq}} - k_{\mathrm{ipll}}x_5 \end{cases} \tag{15}$$

where ω_0 is the angle frequency reference value of AC system and θ is the phase signal park transforms.

The CCSC contains two PI controllers, the dynamics of which can be expressed as

$$\begin{cases} \dfrac{\mathrm{d}f_1}{\mathrm{d}t} = I_{\mathrm{cirdref}} - I_{\mathrm{cird}} \\ \dfrac{\mathrm{d}f_2}{\mathrm{d}t} = I_{\mathrm{cirqref}} - I_{\mathrm{cirq}} \end{cases} \tag{16}$$

with I_{cirdref} and I_{cirqref} being the reference value of the circulating current. f_1 and f_2 indicate the intermediate control variables, which denote the integral of the PI controller's error signals.

The output of the CCSC is the circulating current suppression voltage, which is denoted by U_{cird} and U_{cirq} .

$$\begin{cases} U_{\text{cird}} = k_{\text{pcir}} \left(I_{\text{cirdref}} - I_{\text{cird}} \right) + k_{\text{icir}} f_1 + 2\omega L_{\text{arm}} I_{\text{cirq}} \\ U_{\text{cirq}} = k_{\text{pcir}} \left(I_{\text{cirqref}} - I_{\text{cirq}} \right) + k_{\text{icir}} f_2 - 2\omega L_{\text{arm}} I_{\text{cird}} \end{cases} \tag{17}$$

in which k_{pcir} and k_{icir} are the proportional and integral gain of the PI controller in the CCSC.

3.3. AC System

Figure 6 depicts the equivalent circuit of an AC system, where the AC system is modelled by a resistance-inductance series circuit with an AC voltage source [39], and R_{ac} and L_{ac} are the equivalent AC resistance and inductance, respectively. L_{T} are the transformer equivalent inductance. The internal dynamic characteristics of AC system are coupled with the DC power grid through the AC voltage source.

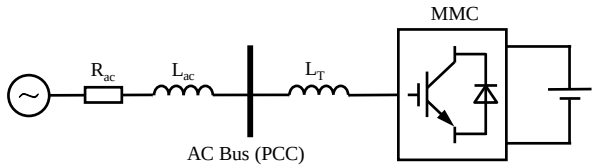

Figure 6. Equivalent circuit of AC System.

3.4. DC System

The DC system of an MMC-based MTDC transmission system consists of DC transmission lines and the smoothing reactors at the converter ends [39]. With the smoothing reactors included in the equivalent series inductance of the transmission line, a lumped resistance-inductance series circuit is applied in order to establish the equivalent model of a DC transmission line, as shown in Figure 7.

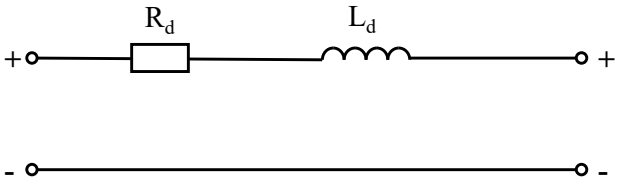

Figure 7. Equivalent circuit of DC Line.

The state space model of a DC transmission line can be given by

$$\frac{\mathrm{d}I_{\text{dc}}}{\mathrm{d}t} = \frac{U_{\text{dc1}}}{L_{\text{d}}} - \frac{U_{\text{dc2}}}{L_{\text{d}}} - \frac{R_{\text{d}} I_{\text{dc}}}{L_{\text{d}}} \tag{18}$$

where U_{dc1} and U_{dc2} are the DC voltages at each end of the DC line; and, R_{d} and L_{d} are the equivalent resistance and inductance.

4. Analysis and Suppression Method of Short Circuit Current in MMC-Based MTDC Power Gird

The massive short circuit current caused by DC short circuit fault seriously threatens the security and reliability of DC power grids due to the small impedances of MMCs and DC transmission lines. It is necessary to analyze and suppress the DC short circuit currents in MMC-based MTDC power grid to ensure the safe and stable operation of DC power grid. A review of short current calculation and suppression methods is presented in this section.

4.1. Short Circuit Current Calculation Method

Various types of DC short circuit faults may occur in an MMC-based MTDC power grid, such as pole-to-pole short circuit fault and single-pole-to ground short-circuit fault. Existing research on DC short circuit current calculation mainly focuses on the pole-to-pole short circuit fault, because the pole-to-pole fault current of which is the most serious fault currents of all types of DC fault [13,34–36,40–42]. Therefore, the calculation of pole-to-pole short circuit current can provide guidance for parameter design and protection schemes of DC power grids.

4.1.1. Pole-to-Pole Short Circuit Current Calculation Method

Once a pole-to-pole DC short circuit fault occurs in MMC-based MTDC power grids, the capacitors discharge rapidly, which leads to massive short circuit current in both transmission lines and each MMC bridge arm. These phenomena usually happen within 5∼10 ms after the fault occurs [17,34]. For an MMC-based MTDC power grid, the dominant component of the short-circuit currents is the discharge currents of SM capacitors. The AC infeed contributions are exclusively present after 10 ms, which can be faithfully ignored [34,43]. It should be noted that the dynamics of MMCs that are based on various SM topologies under DC faults are developed in the same way before blocking, including HB-SM and other SM topologies with DC fault ride through capability [3,7,13].

An equivalent circuit method for calculating the pole-to-pole short circuit fault current in MMC-based MTDC power grids is presented in [13]. In the proposed calculation method, each MMC is represented by (10) and the DC line is equivalent to a series RLC circuit, as shown in Figure 8. The nodes that are connected to a real converter are defended as "real nodes" and the intersection nodes of the transmission lines without connection to a real converter are defined as "virtual node".

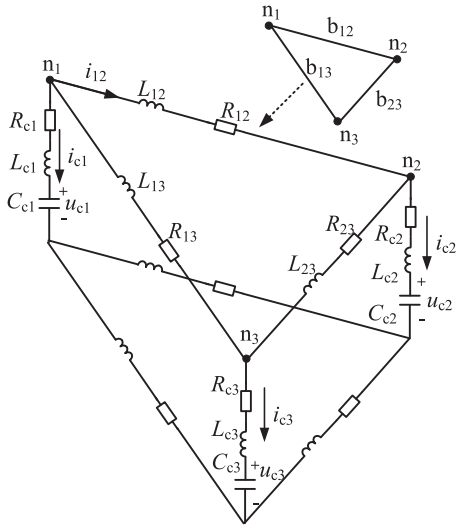

Figure 8. Equivalent circuit of a three-terminal MMC-based DC power grid.

When considering a DC power grid with b branches, N real nodes, and M virtual nodes on the positive pole layer, the total number of the nodes is n. The branch currents matrix $\boldsymbol{i_0}$, node capacitor voltages matrix $\boldsymbol{u_0}$, and node injection current matrix $\boldsymbol{i_{c0}}$ can be expressed by

$$\begin{aligned} \boldsymbol{i}_0 &= \left[\; i_{12}, \ldots i_{ij}, \ldots \; \right]_b^{\mathrm{T}} \\ \boldsymbol{u}_0 &= \left[\; u_{\mathrm{c}1}, u_{\mathrm{c}2}, \ldots u_{\mathrm{c}N}, u_{\mathrm{c}N+1}, \ldots u_{\mathrm{c}N+M} \; \right]_n^{\mathrm{T}} \\ \boldsymbol{i}_{\mathrm{c}0} &= \left[\; i_{\mathrm{c}1}, i_{\mathrm{c}2}, \ldots i_{\mathrm{cn}}, \; \right]_n^{\mathrm{T}} \end{aligned} \tag{19}$$

Branch current equations in matrix form can be expressed as

$$\mathbf{A}_0 \cdot \boldsymbol{u}_0 = \boldsymbol{R}_0 \cdot \boldsymbol{i}_0 + \mathbf{L}_0 \cdot \dot{\boldsymbol{i}}_0 \tag{20}$$

where $\mathbf{A}_0$ is the incidence matrix with n nodes and b branches before fault. $\boldsymbol{R}_0$ and $\boldsymbol{L}_0$ is the resistance matrix and inductance matrix before fault, respectively. Assume the fault point that is indicated by 0 is set between node i and node j and R_f is the fault resistance. By applying fault branch, the R_{ij} and L_{ij} are replaced by R_{i0}, R_{j0} and L_{i0}, L_{j0}. i_{i0} and i_{j0} denote the currents of branch $i0$ and $j0$, respectively. The modified matrices are defined as $\boldsymbol{R}_t$ and $\boldsymbol{L}_t$, respectively. $\mathbf{A}_0$ is modified to $\mathbf{A}_t$ with the branch ij that is replaced by branch $i0$ and $j0$. Therefore, (20) can be rewritten as

$$\boldsymbol{A}_t \cdot \boldsymbol{u}_0 = \boldsymbol{R}_t \cdot \boldsymbol{i} + \boldsymbol{L}_t \cdot \dot{\boldsymbol{i}} \tag{21}$$

The relationship between the post-fault branch currents $\boldsymbol{i}_\mathbf{c}$ and post-fault node injection currents $\boldsymbol{i}$ can be represented by

$$\boldsymbol{i}_\mathbf{c} = \boldsymbol{A}_{t1}^\mathrm{T} \cdot \boldsymbol{i} \tag{22}$$

where $\boldsymbol{A}_{t1}$ is the first to Nth columns in $\boldsymbol{A}_t$

The relationship between the capacitor voltages and currents can be presented by

$$\dot{\boldsymbol{u}} = \boldsymbol{P} \cdot \boldsymbol{i} \tag{23}$$

where $\boldsymbol{P}$ is given by

$$\boldsymbol{P} = -\mathrm{diag}\left[\ 1/C_{\mathrm{c}1}, 1/C_{\mathrm{c}2} \ldots 1/C_{\mathrm{c}N}\ \right] \boldsymbol{A}_t^\mathrm{T} \tag{24}$$

The virtual node voltages are not required and they can be eliminated through replacing the virtual node voltages with voltage drop through the DC line route from a node n to the short circuit fault point 0.

After eliminating the voltage of vertical nodes and update the matrices, the simultaneous differential equations for short circuit calculation are expressed as

$$\begin{cases} \boldsymbol{A} \cdot \boldsymbol{u} = \boldsymbol{R} \cdot \boldsymbol{i} + \boldsymbol{L} \cdot \boldsymbol{i} \\ \dot{\boldsymbol{u}} = \boldsymbol{P} \cdot \boldsymbol{i} \end{cases} \tag{25}$$

where $\boldsymbol{A}$, $\boldsymbol{R}$, and $\mathbf{L}$ are the updated matrices of $\boldsymbol{A}_\mathbf{t}$, $\boldsymbol{R}_\mathbf{t}$, and $\boldsymbol{L}_\mathbf{t}$, respectively. The currents through the DC lines under the DC short circuit fault can be calculated through (25).

The proposed pole-to-pole short circuit current calculation method is available for both MMC and other VSCs. It is also available for calculating pole-to-pole short circuit current of different DC grid topologies, such as radial, ring, and mesh DC power grids. By dividing the DC power grid into fault zone and residual zone, this method is suitable for DC power grids with several DC voltage levels that are connected by DC/DC transformers. Only the internal fault zone current is needed to be calculated [13].

4.1.2. Short-Circuit Current Calculation Considering MMC Control

A short-circuit current calculation method that considers MMC control for MMC-based MTDC power grids is proposed in [40]. When compared with the previous calculation method in [13,35], the MMC is modeled as an RLC series circuit in parallel with a time-dependent controlled current source I_x based on the AVM, as shown in Figure 9.

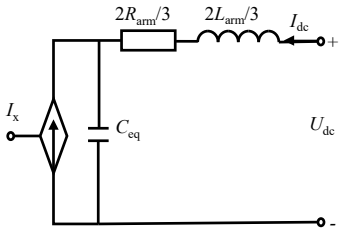

Figure 9. DC side modified AVM of the MMC.

The equivalent model for an MMC-based MTDC power grid is established by combing the equivalent MMC model with the equivalent resistance-inductance series circuits of the DC lines. The post-fault branch currents and node voltages are obtained by solving the equivalent model of the DC grid through a companion circuit method. The proposed short circuit current calculation method that considers MMC control can be flexibly accommodated for all kinds of DC faults by updating the conductance matrix, history current vector, and DC current source vector [40].

The calculation of DC short circuit current calculation considering MMC control in [42] is performed in the frequency domain. The MMC is represented by an AVM and the effect of fault-generated traveling waves (FTWs) is fully considered. Therefore, the proposed method avoids the shortcoming that the *RL* line model-based methods cannot solve the nodal voltage, and the effective time window is much longer than the EDM-based method. The proposed method satisfies the accuracy requirement with a small computational burden. Therefore, it can be applied to a large number of fault calculations requirement scenes, such as parameter design and the protection of DC power grids.

When compared with the equivalent circuit method in [13,34] ignoring the MMC control, the short calculation proposed in [40–42] consider the dynamics of the control system in the short circuit current calculation, which can provide guidance for fault current suppression through MMC control.

4.2. DC Short Circuit Current Suppression Method in MMC-Based MTDC Power Grid

The existing short-circuit current suppression methods dealing with the DC short-circuit current can be divided into three types [13]:

- Using the MMC topology with DC fault ride through capability such as FB-SMs, CD-SMs, and 5LCC-SMs, etc.
- Installing current limiting device and cooperating with DC circuit breakers to isolate the DC fault line.
- Design MMC control strategies in order to suppress the short circuit current.

4.2.1. MMC Topologies with DC Fault Ride Through Capability

The HB-SM is the most widely applied topologies of MMC for DC power girds due to the simple structure and low cost. However, MMC rhat is based on HB-SM cannot block the fault currents fed from the AC grid [44], as shown in Figure 10a. Without DC CBs, it can only clear DC fault line by tripping the AC circuit breakers [45]. Various SMs have been proposed and investigated in order to improve fault-blocking performance of the MMC-based MTDC power grids [7]. Figure 10b–e show the short circuit current discharge circuit (in red line) for various SM topologies.

- FB circuit: after a DC short circuit current occurs, all of the IGBTs in the SMs are blocked and the capacitor voltages can generate reverse voltages to block the AC currents, as shown in Figure 10b. Thus, the FB-SMs can provide the DC fault ride through capability [17].
- CD circuit: in the CD based MMC-HVDC system, although the SMs can block the DC fault current [2], they can only generate a reverse voltage U_{dc} per bridge arm, which is, half of the reverse voltage produced by the FB-SMs per arm, as shown in Figure 10c. Thus, it takes more time for the CD-MMC to suppress the fault current to zero [16].

- 5LCC circuit: during a DC short circuit fault, the short-circuit current can be blocked by the two capacitors of the 5LCC-SM, as shown in Figure 10d. The reverse voltage generated by 5LCC-SM per arm is the same as the voltage produced by the FB-SM [17].
- 3LCC circuit: similar to the HB-SM, the three-level NPC and FC SMs cannot handle any DC fault, as shown in Figure 10e,f. Furthermore, from a manufacturing perspective, this solution is not very attractive [46].

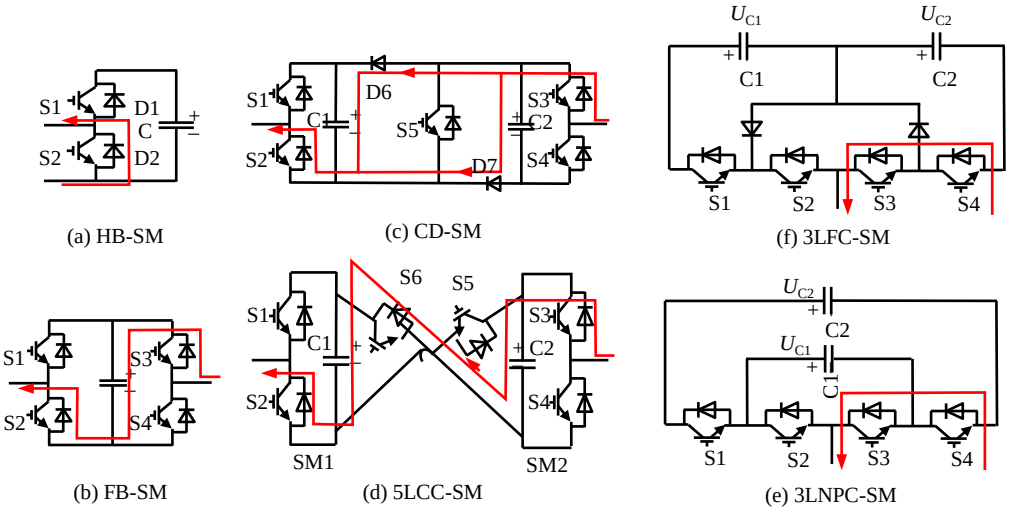

Figure 10. Fault current discharge path of various SM topologies.

The power transmission will be interrupted and the entire DC power grid will be shut down because SMs with DC fault ride through capability cut off the fault line through blocking all of the converters. Meanwhile, changing SM topologies will also create extra investment cost and additional loss of the project [2].

4.2.2. Fault Current Limiting Devices

Installing current limiting devices in DC systems and cutting off the fault line with DC CBs is another preferable suppression method for short circuit current. DC inductors and DC fault current limiters (FCLs) are two widely applied fault current limiting devices in MMC-based MTDC grids [47].

The current-limiting DC inductors are usually installed at both ends of the transmission lines in series in order to achieve better fault current suppression performance [48,49]. Figure 11 shows the short circuit current with different inductive fault current limiters in a four-terminal MMC-based power gird. The detailed structure and parameters of the four-terminal MMC-based power gird can be found in [50]. The inductive fault current limiters have a good performance in limiting the rising rate of the short circuit current.However, the series inductors can decrease the robustness and response speed of the DC system [51].

Another widely applied current limiting device is the DC FCL. FCL has many different topologies, such as resistive FCL, superconducting FCL (SFCL), solid state FCL, and magnetic FCL.

- Solid FCLs: solid FCLs are the most popular topologies due to its advantages of minimum power loss under normal condition, quick response, fast recovery capacity, good reliability, and low cost [52]. A resistive based solid-state FCL is proposed in [53]. The resistive based solid-state FCL consists of a current-limiting resistor module R and a control module in parallel, as shown in Figure 12.

  The resistive based solid-state FCL has two operational states. In the normal operating state, reverse parallel gate turns off thyristors (GTOS) in a conducting state, which ensures that the current-limiting resistor R is bypassed and the operational current can flow through the GTOs.

Under DC fault conditions, T_1 and T_2 are turned off according to the operation signal issued by the fault detection system, and R is rapidly put into use, which increases the system damping and inhibits the fault current's rising.

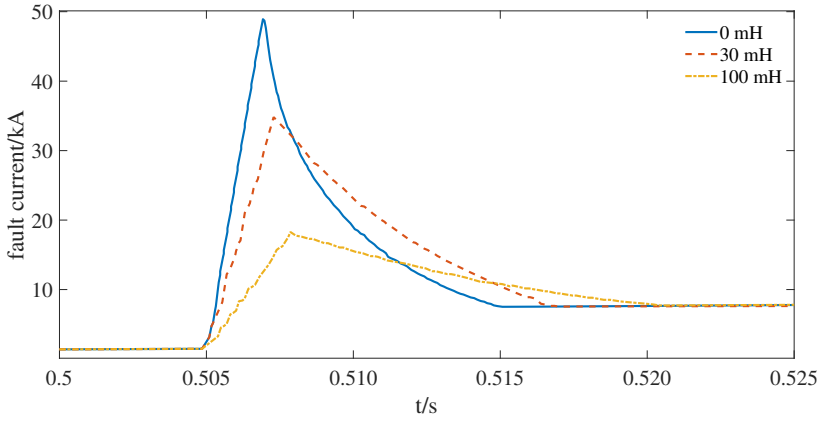

Figure 11. Short circuit current with different inductive fault current limiters.

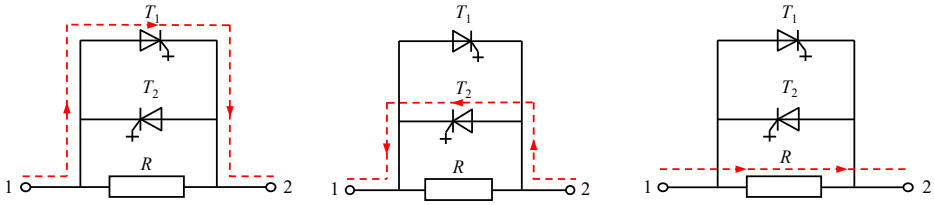

Figure 12. Operating states of resistive based solid-state fault current limiter (FCL).

- SFCL: the SFCL operates under a superconducting state in normal operation state, which offers no resistance to the load current. Meanwhile, it can achieve high resistance under fault conditions [50,54–56]. Figure 13 shows the short circuit current with resistive FCLs in a four-terminal MMC-based power grid, whose structure and parameters can be found in [50]. It can be found that, although the amplitude of the DC short circuit current can be effectively decreased, the resistive SFCL cannot limit the rising rate. To remedy this defect, reference [50] proposes an improved structure for inductive SFCL, as shown in Figure 14.

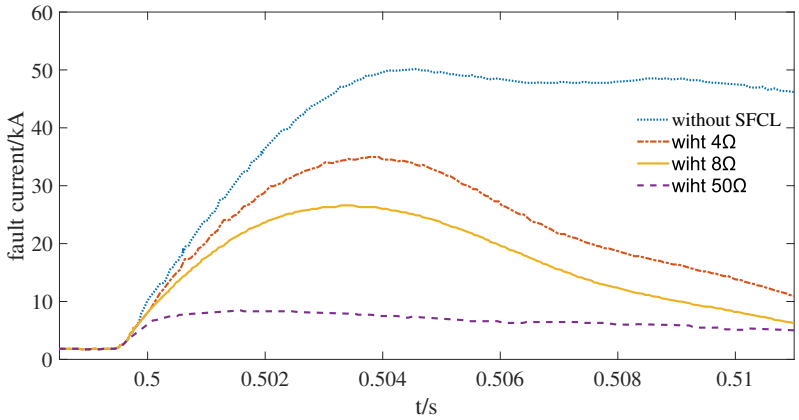

Figure 13. Short circuit current with the resistive FCLs.

The inductive SFCL consists of several diodes and a saturated iron core SFCL. The saturated iron core SFCL is placed between the bridges composed with four diodes ($D_1 \sim D_4$). The proposed SFCL is connected in series in DC transmission lines via connectors A and B. Under normal

conditions, the DC operational current can flow through the diodes groups D_1 and D_4, or D_2 and D_3. Wherever the short circuit fault occurs, the bi-directional SFCL allows for the fault current flow through. The copper made primary coils of the iron core SFCL are connected with the DC system. The secondary coils are made of superconductive materials and powered by a DC source. The external feature of the proposed inductive SFCL is equivalent to a small inductance and it has little impact on the system normal operational dynamics.

The improved inductive SFCLs are applied to the four-terminal power grid that is shown in [50]. Under DC short circuit fault conditions, the inductance of the SFCL increases rapidly in order to restrain the rising rate of the short circuit current as shown in Figure 15. However, the permeability and the coil turns limit the size of the proposed inductive SFCL [50]. Moreover, superconductive FCL needs a high technological level and huge capital cost [47], which makes it unable to be widely applied in MMC-based MTDC power grids.

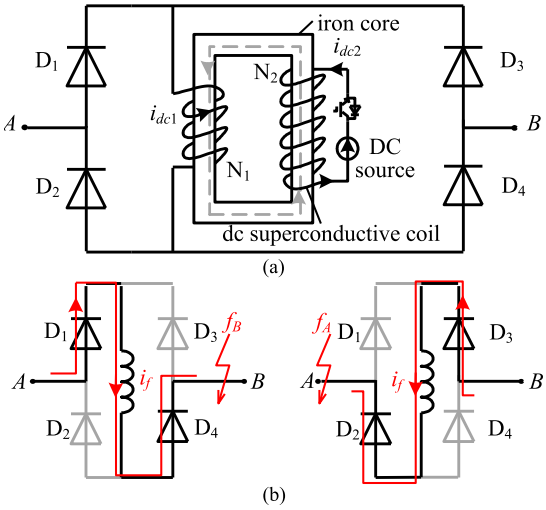

Figure 14. The working principle of the inductive SFCL: (**a**) Topology; (**b**) Short circuit current path.

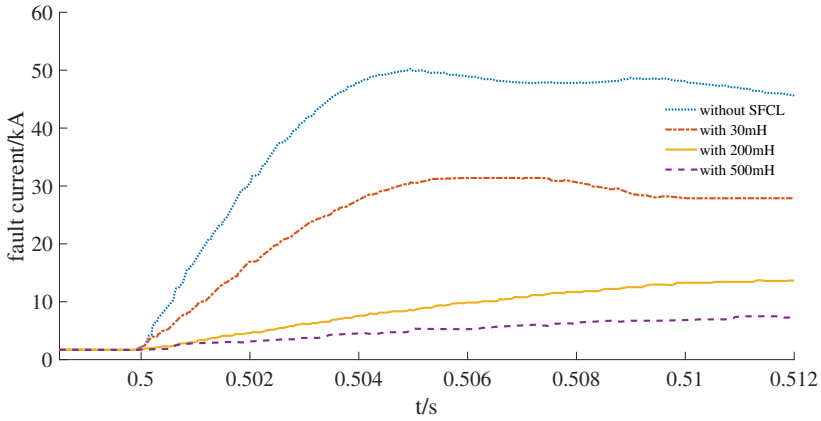

Figure 15. Short circuit current with the improved inductive SFCL.

- NSFCL: a kind of structure of NSFCL, called capacitor-based FCL (CBFCL), is proposed in [57] and the power circuit structure of the CBFCL is shown Figure 16.

  The CBFCL consists of three main sections:

  - isolation transformer and rectifier;
  - a bypass switch; and,
  - capacitor bank section with DC bus and corresponding switches.

Switch S_1 is applied to flow the normal operation current, while S_2 is applied to flow the fault current. Energy is transfered between the capacitor bank section and the DC bus through S_C and S_d. The operation modes that are under normal conditions are shown in Figure 16a,b and operation modes under fault conditions are shown in Figure 16c,d. Under normal conditions, S_C is turened off and the capacitor bank section is charged while taking into account resistor r_C in series with capacitor bank after a time constant. Because the capacitor bank section receives electrical energy from the DC bus, which leads to a voltage rise. S_C is conducted after the voltage of capacitor bank section reached a determined level. The proposed CBFCL circuit has little impact on the normal operation of the MMC-HVDC system. When a DC short circuit fault occurs, S_1 is conducted. By turning on S_2 in short circuit current limitation, it makes the capacitor bank section and inductor participate insert in current path.

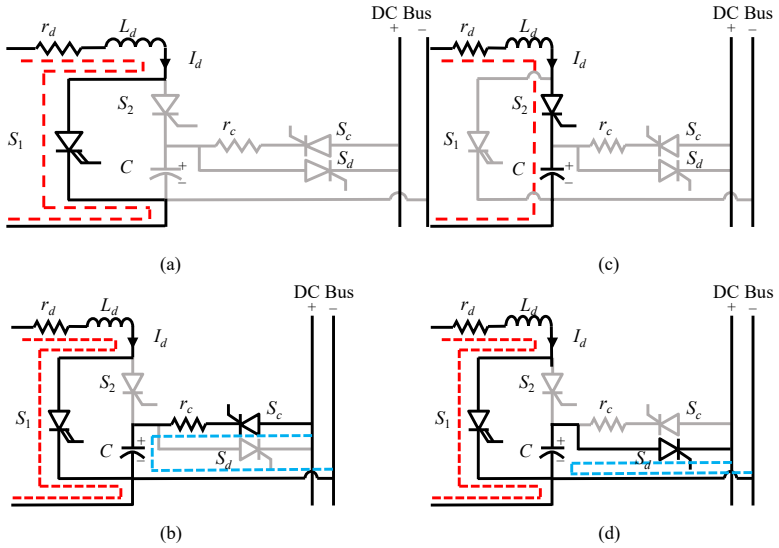

Figure 16. Performance of the proposed CBFCL: (**a**) under normal condition, (**b**) under normal condition considering charge of the capacitor bank, (**c**) under fault condition, and (**d**) after fault clearance.

When comparing with previous studies, there are no switching strategies, such as pulse width modulation in the CBFCL for limiting the fault current and all of the switches behave like contactors in which they are closed or opened. This feature makes it possible to use cheaper switches and a better lifetime of switching instruments. Moreover, the CBFCL not only cuts off the short circuit current, but also saves energy in the capacitor that can be utilized after fault clearance [57].

4.2.3. MMC Fault Current Suppression Control Strategy

Although many researches have investigated the topologies and application of current limiting devices, it is still not a perfect method for suppressing the DC short-circuit current. Due to the difficulty in manufacturing and high cost, there is no suitable DC fault current limiting devices for widely application [58]. The full use of converters' own capability through properly designed control strategies has become a prioritized choice, and it has been widely adopted in scenarios, such as DFIGs [59]. Therefore, making full use of the MMCs' self-controlling ability will be an ideal and feasible method of short circuit current suppression for MMC-based MTDC power girds. Several researches have investigated the fault suppression method by designing new MMC control strategies [43,60].

Reference [60] proposed a comprehensive DC short-circuit fault ride through a strategy for a hybrid MMC with HB-SMs and FB-SMs. Under normal conditions, since the output voltage of the FB-SM is not required, the switches of the FB-SMs of both upper and lower arms are turned on. The circuit of the hybrid MMC is topologically equivalent to a traditional HB-MMC. Under a

pole-to-pole fault condition, a bipolar output voltage of the FBSM is required in the upper and lower arm. The HB-SMs are bypassed and the circuit of the hybrid MMC is topologically equivalent to the double star-connected cascade H-bridge (CHB) converter that reduces the number of SM in operation and restrains the rise of short circuit current. The voltage injection method is applied to balance bridge arm capacitor energies, which ensures that the AC grid is not affected during the fault.

A source-side DC fault current clearance scheme for hybrid MMC-based power grids is proposed in [43]. The hybrid MMC consists of the HB-SMs and FB-SMs and it adopts converter DC current control and DC fault line current control during the fault. Figure 17 shows the flowchart of the protection scheme. After the DC short circuit fault is detected, the nearest MMC switches into fault line current control mode and the fault is isolated by a mechanical circuit breaker. In the proposed scheme, there are no DC CBs required, which significantly benefits the construction of MMC-based DC power grids. However, the above two methods need hybrid MMC and it is still not available for the most widely applied HB-MMC.

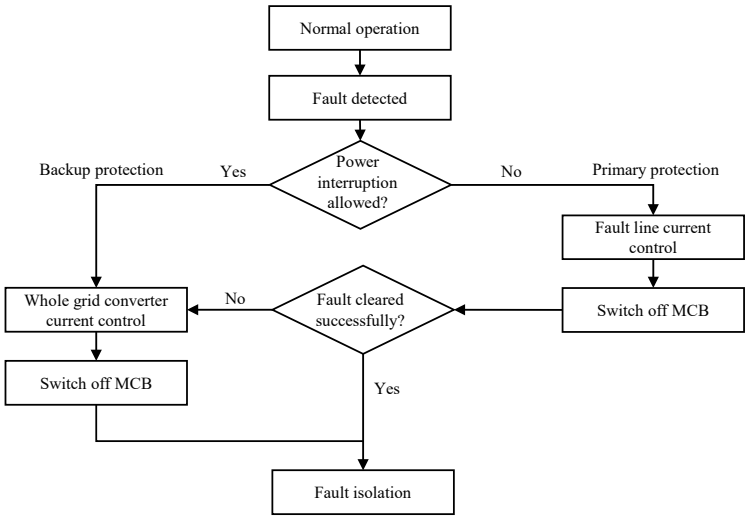

Figure 17. Flowchart of the proposed protection schemes.

A DC short circuit current suppression method that is based on bridge arm voltage control is designed in [58]. It is found that the rising rate of the short circuit current is proportional to the number of sub-modules participating in the discharge that can be reduced through reducing the DC component in the reference voltage in the bridge arm after fault.

Figure 18 shows the fault current limiting control strategy structure. Under normal operation conditions, the output voltage of the system is larger than the voltage. The DC component compensation of the bridge arm voltage is 0, and the AC component in the bridge arm is not adjusted. Therefore, it has litle impact on the normal operation control characteristics of the system. Under DC fault conditions, the system output voltage rapidly drops once the short circuit fault occurs, which will be smaller than the voltage threshold. The control system switches the operation mode to compensate the DC component of the bridge arm voltage. With the DC and AC component of the compensated bridge arm reduced simultaneously, the output DC voltage is further reduced and the fault current is suppressed. The proposed current limiting measure is applied to a double-terminal MMC-HVDC system in [58]. Figure 19 shows the comparison of DC short circuit current with/without a current limiting measure. The increasing rate of the DC short-circuit current with a current limiting measure significantly decreases.

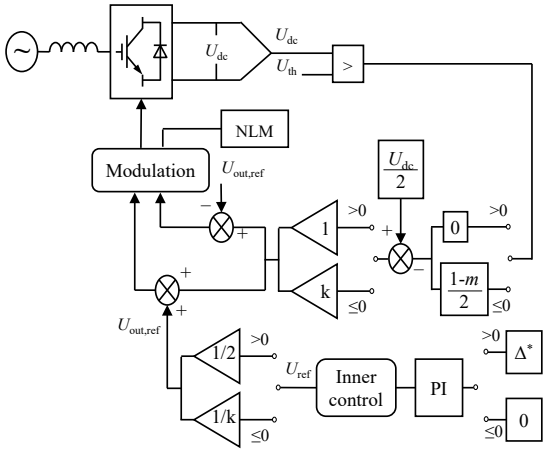

Figure 18. Block diagram of MMC based on partial bypass of SMs.

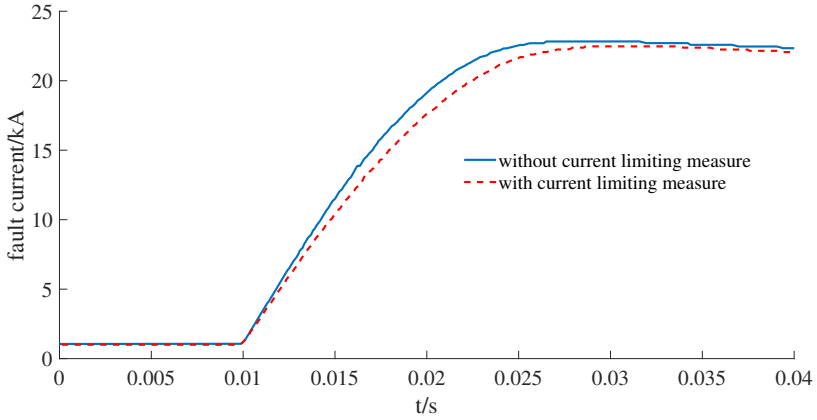

Figure 19. Comparison of DC fault current with/without current limiting measure.

When compared with redesigning the MMC topologies and installing new current limiting devices, designing MMC control strategies for short-circuit current suppression can make full use of the control capability of MMCs and save capital cost.

5. Conclusions and Future Trend Exploration

This paper gave a comprehensive review of the existing DC short-circuit current analysis and suppression methods that were used in MMC-based MTDC power grids, including the latest theoretical achievements and techniques applied in engineering practice. The existing MMC modeling, DC short circuit current calculation methods, and suppression methods were classified and the advantages and disadvantages were summarized in this paper.

The models of MMC-based MTDC power grids have been studied and investigated for different scenarios. The DSM is feasible for SM-level dynamic analysis and control design. The AVM and SAVM are the preferred models for system-level analysis and control design. The DEM can be applied to design the balancing control of the capacitor voltages and represent the blocked mode. The EDM is the most suitable model for DC fault analysis and protection design.

The mainstream of DC short-circuit current calculation in MMC-based MTDC power grids is the equivalent circuit method, where MMCs are formulated as capacitor-inductor series circuits. However, the equivalent circuit method ignores the internal dynamics of MMCs and cannot display the inherent characteristics of the MMC-based MTDC power grids. It is necessary to establish the fault current analysis MMC model when considering the internal dynamics, and propose the short circuit calculation method considering the dynamic characteristics of MMC-based MTDC power grids.

The existing fault current suppression methods in MMC-based MTDC power grids usually include changing SM topologies, adding current limiting devices, and controlling the MMC. Table 4 presents the above-discussed DC short circuit current suppression methods to make a comparison of their features. In the table, $\surd$ indicates that the chosen technique is strongly related to the corresponding item; $\times$ indicates that the chosen technique is not related to the corresponding item; 'B' indicates 'Big'; 'M' indicates 'Moderate'; and, 'S' indicates 'Small'. Most of the existing MMC-HVDC projects adopt HB-SMs and they cannot cut off the fault current by themselves. The cost of replacing the SM topologies with fault ride through capability is very large, and this disadvantage limits its practical application. Although installing fault current limiting devices can achieve good fault current suppression performance, it also has the disadvantages of high cost and impact on normal operational conditions. The future research direction of the fault current limiting devices is to reduce the cost and impact on the normal operational conditions. Suppressing the DC fault current through controlling MMC has the advantages of low cost, small impact on normal operational conditions, and flexibility in modification. Thus, it is an ideal DC fault current suppression method for MMC-based MTDC power grid and it has broad prospects for future development.

Table 4. Comparison of different short circuit current suppression method.

Method	SM Change	Add Devices	Increase Impedance	Iron Core	Superconducting Materials	Extra Cost	Impact on Normal Condition
FB-SM	√	×	×	×	×	B	S
DB-SM	√	×	×	×	×	B	S
5LCC-SM	√	×	×	×	×	B	S
DC inductor	×	√	√	√	×	S	B
Solid FCL	×	√	√	×	×	M	S
SFCL	×	√	√	√	√	B	S
CBFCL	×	√	√	×	×	B	S
Hvbird MMC	√	×	×	×	×	B	S
MMC control	×	×	×	×	×	×	S

Author Contributions: Conceptualization, B.Q.; methodology, B.Q., W.L., and R.Z.; software, W.L. and B.Q.; validation, W.L., J.L. and H.L.; investigation, W.L. and J.L.; writing—original draft preparation, B.Q., W.L. and R.Z.; writing—review and editing, W.L., R.Z., and J.L.; supervision, B.Q. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest.

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