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Investigation on Tunneling-based Ternary CMOS with Ferroelectric-Gate Field Effect Transistor Using TCAD Simulation

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Received: 6 June 2020; Accepted: 17 July 2020; Published: 20 July 2020

Abstract: Ternary complementary metal-oxide-semiconductor technology has been spotlighted as a promising system to replace conventional binary complementary metal-oxide-semiconductor (CMOS) with supply voltage (V_{DD}) and power scaling limitations. Recently, wafer-level integrated tunneling-based ternary CMOS (TCMOS) has been successfully reported. However, the TCMOS requires large V_{DD} (> 1 V), because a wide leakage region before on-current should be necessary to make the stable third voltage state. In this study, TCMOS consisting of ferroelectric-gate field effect transistors (FE-TCMOS) is proposed and its performance evaluated through 2-D technology computer-aided design (TCAD) simulations. As a result, it is revealed that the larger subthreshold swing and the steeper subthreshold swing are achievable by polarization switching in the ferroelectric layer, compared to conventional MOSFETs with high-k gate oxide, and thus the FE-TCMOS can have the more stable (larger static noise margin) ternary inverter operations at the lower V_{DD} .

Keywords: ferroelectric; band-to-band tunneling; ternary CMOS; low power devices; semiconductor devices

1. Introduction

Tunneling-based ternary complementary metal-oxide-semiconductor (TCMOS) technology has been reported recently [1–3]. Instead of the binary systems of the existing complementary metal-oxide-semiconductor (CMOS) technology, the third output voltage (V_{out}) state is formed in the ternary systems, and it has been spotlighted in terms of scaling and energy-efficiency [4,5]. In the TCMOS, the off-current (I_{OFF}) levels of NMOS (n-type MOS) and PMOS (p-type MOS), which are generated by band-to-band tunneling (BTBT), should be matched to form the third V_{out} state during inverter operations. In contrast to conventional ternary devices that utilize multithreshold voltage (Multi- V_t) transistors [6–12], the TCMOS can perform ternary operations using a pair of NMOS/PMOS with a single voltage (V_t); the fabrication process is also comparable to the conventional CMOS process, because it can be fabricated only by introducing one additional doping process. However, the TCMOS has the disadvantage of slow switching speed caused by low on-state current (I_{ON}). In general CMOS, the time required for V_{out} state transition is sub-nsec, while it takes $\sim \mu\text{sec}$ for the TCMOS to be switched [1].

In this study, TCMOS consisting of ferroelectric-gate field effect transistors (FE-TCMOS), consisting of ferroelectric-gate field effect transistor (FeFET), is proposed to improve switching speed and supply voltage (V_{DD}) scaling since it is well-known that the FeFET boosts I_{ON} and steepens

subthreshold swing (SS), compared to conventional MOSFETs [13–17]. To verify the operations of the FE-TCMOS, technology computer-aided design (TCAD) simulations with the calibrated ferroelectric material parameters are used and the ternary operations are rigorously compared between TCMOS and FE-TCMOS.

2. Experiments and Simulation Methods

To embody the ferroelectricity in FE-TCMOS (Figure 1a,b), a metal-ferroelectric-metal (MFM) capacitor was first fabricated using hafnium zirconium oxide (HZO) as ferroelectric material, and polarization-electric field (P-E) characteristics were obtained. Then, the simulation parameters of the ferroelectric material were achieved by fitting the simulation data to the measurement P-E data (Figure 1c) using the Sentaurus 2-D TCAD simulations where Preisach model was used for the calibration [18]. The equation for the model is as follows:

$$P_{aux} = c \cdot P_s \cdot \tanh(w \cdot (E \pm E_c)) + P_{off} \quad (1)$$

where E is electric field, P_{aux} is auxiliary polarization, and

$$w = \frac{1}{2F_c} \ln \frac{P_s + P_r}{P_s - P_r} \quad (2)$$

$$\frac{d}{dt}P(t) = \frac{P_{aux}[E(t)] - P(t)}{\tau_p} \quad (3)$$

where P_s is saturation polarization, P_r is remanent polarization, E_c is coercive field, and τ_p is relaxation time for polarization in ferroelectric material. Figure 1c indicates that the measured and the calibrated P-E curves are well-matched [15]. Here, the relaxation time τ_p is set to 250 ns. These ferroelectric material parameters are reflected to the gate dielectric of FE-TCMOS for the simulations, whereas high-k dielectric ($\epsilon_b = 25$) is applied instead of the ferroelectric material for TCMOS simulations. Figure 1a shows the schematic diagram of the FE-TCMOS implemented in the simulations. A P-N junction is formed by introducing an additional doped layer between the source and the drain under the channel. When a drain voltage (V_D) is applied, the band-to-band tunneling (BTBT) is generated at the drain-side P-N junction of the layer, and thus the P-N junctions formed by adding the doped layer can be modeled as a drain-side tunnel junction diode. Figure 1b is the circuit schematic diagram of the FE-TCMOS, which shows that the tunnel junction diode is connected to the V_{out} node as contrast to a conventional CMOS. Specific simulation parameters are listed in Table 1.

Figure 1. (a) The schematic diagram of TCMOS consisting of ferroelectric-gate field effect transistors (FE-TCMOS). The ferroelectric layer is inserted between gate and oxide interfacial layer. (b) The circuit schematic diagram of FE-TCMOS. Tunnel junction diode is located under the drain-side channel. (c) Experimental polarization-electric field (P-E) curve and calibrated P-E curve by technology computer-aided design (TCAD) simulation.

Table 1. Simulation Parameters.

Parameter	Description	Value
L_G	Gate Length	1 μm
N_S	Source Doping Concentration	10^{20} cm^{-3} (Arsenic)
N_D	Drain Doping Concentration	10^{20} cm^{-3} (Arsenic)
N_B	Body Doping Concentration	10^{17} cm^{-3} (Boron)
N_T	Tunneling Layer Doping Concentration	$5 \times 10^{19} \text{ cm}^{-3}$ (Arsenic)
T_{TNL}	Tunneling Layer Thickness	20 nm
T_{OX}	Interfacial layer Thickness	1 nm
T_{FE}	Ferroelectric Thickness	10 nm
P_s	Saturation Polarization	18 $\mu\text{C}/\text{cm}^2$
P_r	Remanent Polarization	30 $\mu\text{C}/\text{cm}^2$
E_c	Coercive Field	0.75 MV/cm
τ_p	Relaxation Time for Polarization	250 ns
ϵ_b	Permittivity Constant of Ferroelectric Material	25

3. Results and Discussion

3.1. Tunneling-Based Ternary CMOS with Ferroelectric-Gate Field Effect Transistor

Before identifying the operations of TCMOS, the electrical characteristics of TNMOS (tunneling-based ternary NMOS) and TPMOS (tunneling-based ternary PMOS) were first verified (Figure 2). Compared to conventional N/PMOS for CMOS, TNMOS/TPMOS have the larger V_t (close to V_{DD}) and the constant I_{OFF} regardless of gate voltage (V_G). As aforementioned, the I_{OFF} is generated by the BTBT at the drain-side tunnel junction and hence the I_{OFF} increases with the larger V_D (Figure 3). For the stable TCMOS operations, the I_{OFF} of TNMOS/TPMOS needs to be almost the same at $V_D = \sim \text{half } V_{DD}$ because the third V_{out} state between $V_{out} = 0 \text{ V}$ and $V_{out} = V_{DD}$ is formed using V_{DD} divided by the resistance difference (namely, the I_{OFF} difference) between them [2], if the TNMOS/TPMOS are simplified as variable resistors with respect to V_D . Thus, the doping concentration modulation for the tunneling layer is essential to adjust the I_{OFF} in the TCMOS fabrication process.

Figure 2. The transfer characteristics of conventional NMOS/PMOS and TNMOS/TPMOS. Due to the I_{OFF} generated from the tunnel junction, the I_{OFF} increases with the larger drain voltage. Compared with conventional NMOS/PMOS, TNMOS/TPMOS are designed to have larger voltage (V_t).

The ferroelectric material (e.g., doped HfO_2) can have the larger permittivity by a polarization switching than the general high- k dielectric material (e.g., HfO_2). The slope of the P-E curve refers to the permittivity of the dielectric, and the slope of the P-E curve in the ferroelectric material is larger than that of the high- k dielectric. Therefore, when the high- k dielectric is replaced with the ferroelectric layer in the gate stack of a MOSFET, the larger I_{ON} and the steeper SS are achievable. Figure 4a shows the comparison of the transfer characteristics between conventional TNMOS/TPMOS and FE-TNMOS (ferroelectric-gate field effect transistors-TNMOS)/TPMOS. As expected, the larger

I_{ON} and the improved SS are observed in the FE-TNMOS/FE-TPMOS (ferroelectric-gate field effect transistors-TPMOS) (Figure 4a). Considering that the high V_t is inevitable for TCMOS operations, it is expected that FE-TCMOS can be operated at the more scaled V_{DD} . In other words, at a specific V_{DD} , FE-TCMOS might have a faster operation speed and a larger static noise margin than conventional TCMOS.

Figure 3. (a) The schematic diagram of tunneling layer and doping concentration in case of TNMOS. The band-to-band tunneling generation rate at tunnel junction with respect to drain voltage. The drain voltages are (b) 0.05, (c) 0.5, and (d) 1.0 V, respectively. The band-to-band tunneling generation rate becomes larger with the higher drain voltage.

Figure 4. (a) The transfer characteristics of conventional TNMOS/TPMOS and FE-TNMOS/TPMOS. The higher I_{ON} and the steeper SS are shown in FE-TNMOS/TPMOS. (b) The SS of conventional TNMOS/TPMOS and FE-TNMOS/TPMOS with respect to drain current. In the entire drain current range, FE-TNMOS/TPMOS have a lower SS.

3.2. Operation Characteristics of FE-TCMOS

Prior to the evaluation of FE-TCMOS, the voltage transfer characteristics (VTC) of conventional TCMOS and CMOS were first verified. Figure 5a shows the VTC of TCMOS and CMOS where it can be confirmed that TCMOS is stably operated with $V_{DD} = 1$ V as a ternary CMOS with the third V_{out} state. Then, FE-TCMOS and FE-CMOS were embodied by reflecting the calibrated ferroelectric material parameters to the gate stack. To evaluate the electrical characteristics of FE-TCMOS and FE-CMOS, a 7-stage inverter chain was configured in mixed-mode device and circuit simulations as shown in Figure 5b. The input pulse, which has the transition from 0 V to V_{DD} (1 V) with 1 ms rising time, was applied, and the average propagation delay of V_{out} was extracted as the switching time from each inverter stage. Figure 5c demonstrates the switching time as a function of the number of inverter stages. It is found that the FE-TCMOS has the slower switching speed than the FE-CMOS. It has been reported that the tunneling-based TCMOS has the slower (μ sec order) switching speed compared to that (psec order) of the CMOS [1], because the switching delay of an inverter is proportional to the driving current of n/p-type transistors. That is, TNMOS/TPMOS not only have the low I_{ON}

due to the high V_t , but 0 V to half V_{DD} and V_{DD} to half V_{DD} transitions are formed by the I_{OFF} . Considering the 250 ns ferroelectric relaxation time (namely, polarization switching time) obtained in the previous study [15], if the ferroelectric layer is introduced to the CMOS, the boosted I_{ON} and the steeper SS cannot be achieved since the switching speed of the CMOS inverter is much faster than the polarization switching. This means that a ferroelectric material having a faster switching speed (sub-psec polarization switching) than the CMOS switching is required to apply the ferroelectric layer to conventional CMOS. In contrast, the operating speed of the tunneling-based TCMOS is slower than the polarization switching of the ferroelectric material. Therefore, the ferroelectric layer can effectively play a role as a current booster in the TCMOS.

Figure 5. (a) The voltage transfer curves of conventional complementary metal-oxide-semiconductor (CMOS) and ternary complementary metal-oxide-semiconductor (TCMOS). The third V_{out} state is formed in TCMOS by voltage dividing depending on I_{OFF} difference between TPMOS and TNMOS. (b) The circuit schematic diagram of 7-stage inverter chain. (c) The switching time of FE-CMOS and FE-TCMOS with respect to the number of inverter stages. The switching time of FE-CMOS is pico-sec order, whereas FE-TCMOS is micro-sec order. The dashed line represents ferroelectric switching delay, which is larger than the switching time of FE-CMOS.

Subsequently, the switching speed is compared between FE-TCMOS and TCMOS with respect to the number of inverter stages. Figure 6a shows that the switching delay difference between them is negligible, because the switching speed is determined by the I_{OFF} and both devices have almost the same I_{OFF} . The static noise margin (SNM) of FE-TCMOS was investigated from the butterfly curves with various V_{DD} s (0.5 V, 0.7 V, and 1.0 V), and the SNMs were compared with those of TCMOS. Figure 6b indicates that the FE-TCMOS has the sufficient SNM even at low V_{DD} . Additionally, Figure 6c shows the SNM comparison between FE-TCMOS and TCMOS. The improvement of the SNM is extracted as the increase of the SNM in percentage with respect to V_{DD} . It is observed that the FE-TCMOS has the larger SNM and the SNM becomes improved further at the lower V_{DD} , implying that the FE-TCMOS is more advantageous as V_{DD} decreases. These results can be understood better by the steeper SS and the larger I_{ON} of FE-TNMOS/TPMOS than by conventional TNMOS/TPMOS.

Figure 6. (a) The switching time comparison between TCMOS and FE-TCMOS. The switching speed difference between them is negligible. (b) The butterfly curves of FE-TCMOS with respect to V_{DD} . (c) The comparison of static noise margin between FE-TCMOS and TCMOS. The improvement of SNM in FE-TCMOS is extracted as the increase in percentage, compared to TCMOS.

4. Conclusions

In this study, we investigated the ternary CMOS with the ferroelectric layer as a gate oxide. By utilizing the higher capacitance of the ferroelectric layer instead of the conventional high-k dielectric, the larger I_{ON} and the steeper SS were obtained, compared to conventional MOSFETs with high-k gate oxide, which leads to the more stable (larger SNM) ternary inverter operations at the lower V_{DD} . It has the advantage of being completely compatible with existing processes [19]; moreover, through the switching speed comparison between TCMOS and CMOS, it is confirmed that the ferroelectric polarization switching is faster than the tunneling-based ternary inverter switching and thus the ferroelectric layer can play a role as a current booster in TCMOS.

Author Contributions: Conceptualization, K.L.; methodology, K.L.; validation, K.L.; formal analysis, K.L.; investigation, K.L.; resources, K.L. and D.K.; writing—original draft preparation, K.L.; writing—review and editing, K.L., S.K., D.K. and B.-G.P.; visualization, K.L.; supervision, D.K. and B.-G.P. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: This work was supported in part by The Brain Korea 21 Plus Project in 2020, in part by the Future Semiconductor Device Technology Development Program (10067739) funded by Ministry of Trade, Industry and Energy (MOTIE) and Korea Semiconductor Research Consortium (KSRC), and in part by Synopsys Inc.

Conflicts of Interest: The authors declare no conflict of interest.

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