Controlling the Doping Depth in Silicon Micropillars

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Featured Application: The proposed method can be utilized to fabricate micropillar solar cells.

Abstract: Micropillar arrays with radial p–n junctions are attractive for photovoltaic applications, because the light absorption and carrier collection become decoupled. The main challenge in manufacturing radial p–n junctions is achieving shallow (dopant depth <200 nm) and heavy doping ($>10^{20}$ cm $^{-3}$) that will allow the formation of a quasi-neutral region (QNR) and space charge region (SCR) in its tiny geometry. This experimental study investigates an approach that allows shallow and heavy doping in silicon micropillars. It aims to demonstrate that silicon dioxide (SiO $_2$) can be used to control the dopant penetration depth in silicon micropillars.

Keywords: micropillars; silicon; shallow doping

1. Introduction

Micropillar arrays have been of interest for photovoltaic applications because structured patterning of a planar silicon surface leads to enhanced light trapping efficiency [1–7]. This enhancement leads to an increase in efficiency between 1.5–11% [8] and in turn enables solar cells based on thin layers (<100 μ m), thereby greatly reducing start-up materials cost [9–11]. Among the various surface structures possible, micropillar arrays with radial p–n junctions are particularly attractive, because the light absorption and carrier collection become decoupled [12]. In other words, incident light is absorbed along the long wire axis, while generated charge carriers can be collected along the relatively short radial direction [13]. The main challenge in forming radial p–n junctions is achieving shallow doping that will allow the formation of a quasi-neutral region (QNR) and space charge region (SCR) in its tiny geometry [14,15]. Figure 1a is a representation of the desired radial p–n junction [15]. Figure 1b is a representation of the radial p–n junction obtained when the pillars are doped using the same procedure that is used to dope planar silicon wafers [16,17]. Another challenge is reducing the surface defects generated by the direct etching of the semiconductor, which may cause a lower carrier collection efficiency and degradation of the cell performance [18–21]. Current etching and doping techniques result in rough surfaces with major defects that act as favorable sites for surface recombination. This paper aims to demonstrate that silicon dioxide (SiO $_2$) can be used as a layer to achieve shallow (dopant depth <200 nm) and heavy ($>10^{20}$ cm $^{-3}$) doping in micropillars. The reason the above metrics were used (<200 nm and $>10^{20}$ cm $^{-3}$) is because a study has shown that junctions with depth larger than 200 nm resulted in 20% reduced efficiency [22]. Another study [23–25] also revealed that junctions with low dopant concentration ($<2 \times 10^{19}$ cm $^{-3}$) did not give properly functioning diodes.

Figure 1. Image (a) represents the desired radial p–n junction [15], image (b) represents the radial p–n junction obtained when the micropillars were doped with the same method used to dope planar silicon wafers, and image (c) is the potential radial p–n junction with the proposed doping method.

2. Materials and Methods

A p-type Cz (100) wafer with a resistivity of 5–10 Ω -cm was used for the experiments. All wafers were chemically cleaned. The cleaning steps involve preparing a solution of a mixture of H_2SO_4 and H_2O_2 with a 5:1 ratio (Piranha solution). Piranha is mainly used to remove heavy organic materials, like resist and other organic contamination. It works as an oxidant and attacks the hydrocarbons [25]. Vertical silicon micropillars were fabricated using dry etching. The microdisk arrays were patterned in LOR3A and Shipley S1805 photoresist using photolithography. After the pattern was developed, titanium was deposited to a thickness of 50 nm, and nickel was evaporated to a thickness of 200 nm. The lift off process was performed to leave 4 μm circles of the evaporated metals. The samples were etched for 60 min.

Plasma Enhanced Chemical Vapor Deposition (PECVD) was used to deposit 50 nm of SiO_2 at a rate of 10.5 nm/min. The samples were annealed at 950 $^\circ\text{C}$ for 20 s using Rapid Thermal Annealing (RTA). In sample A, the phosphorus was spun-on doped and driven into the sample by rapid thermal annealing. In sample B, SiO_2 was used between the dopant and the substrate in order to reduce the diffusion of phosphorus into the substrate.

In order to perform I–V measurements, aluminum metal contacts were deposited on the top and back of the silicon substrates. The procedure is as follows: (1) spin dope boron on the back of the intrinsic silicon substrate; (2) anneal boron dopant at 950 $^\circ\text{C}$ for five minutes using rapid thermal annealing process; and (3) deposit the aluminum metal contacts on top of the wafer using electron e-beam. The thickness of the metal was 250 nm. A 1 cm $\times$ 1 cm mask was used to deposit the top contacts, with the dimensions of the contact being 2 mm $\times$ 2 mm (5) deposit aluminum contacts on the bottom of the intrinsic silicon.

3. Results

Figure 2 is a Scanning Electron Microscope (SEM) image of the silicon micropillars with no SiO_2 deposition. It was seen that the diameter of the pillars was 3.952 μm . Figure 3 shows a SEM image of the silicon micropillar with silicon oxide deposited on the pillars. It was seen that the diameter of the pillars was 4.170 μm .

X-ray Photoelectron Spectroscopy (XPS) measurements were performed in order to study the depth profile of phosphorus in all the samples. XPS is a tool used for surface analysis. The X-ray depth penetration is about 10 μm , but only the top 10 nm can emit photoelectrons. Figure 4 shows the dopants depth and atomic percentage of Phosphorus in sample A (no oxide layer) and sample B (oxide layer). Sample A showed that with no SiO_2 layer, the phosphorus concentration at 5 nm depth was 8% ($4 \times 10^{21} \text{ cm}^{-3}$) and the atomic percentage dropped to $\approx 2\%$ at 15 nm. Sample B showed that with SiO_2 used as a blocking layer, the phosphorus concentration was 4% at the surface and dropped to

2% at 15 nm. These results show that the concentration of phosphorus and the slope of concentration vs. depth can be controlled by using SiO_2 .

Figure 5 depicts the I-V profile of sample B (oxide layer). The voltage was swept from -5 V to 5 V , and the current was measured. It was observed that a Schottky contact was obtained, where at 5 V the dark current was 0.2 mA/cm^2 and the light current was 0.3 mA/cm^2 . The addition of the silicon oxide insulating layer could play a role in enhancing the solar cell's current output by reducing the cell's saturation current.

Figure 2. Micropillars without oxide layer. The diameter of the pillar is $3.952\text{ }\mu\text{m}$.

Figure 3. Micropillars with oxide layer. The diameter of the pillar is $4.17\text{ }\mu\text{m}$.

Figure 4. Atomic percentage of phosphorous in sample A (no oxide layer/legend with red circles) and sample B (oxide layer/legend with blue squares).

Figure 5. I-V profile of sample B (the sample with an oxide layer).

A p–n junction is characterized by its saturation current, I_0 , which is the sum of the minority saturation current and majority carrier saturation current. It is known that high saturation current hurts the performance of solar cells. Adding an insulating layer between the semiconductor and the metal can reduce the saturation current due to the majority carriers without impacting significantly the short-circuit current which is a result of minority carriers tunneling through the insulator, as shown in Figure 6. The main cause of this phenomena is because the electric field drives the minority carriers towards the barrier, where they can accumulate to tunnel through. The majority carriers on the other hand are pushed away from the interface electric field. This means slowing their passage can significantly reduce their current flow. Thus, creating a Metal–Insulator–Semiconductor (MIS)

contact instead of a Metal–Semiconductor (MS) contact can have the added advantage of reducing the saturation current of the solar cell.

Figure 6. Energy band schematic of a metal–oxide–semiconductor interface [26].

4. Conclusions

The above results demonstrate that silicon oxide, which can be used as a passivating layer [27], can also be used to achieve a shallow doping depth in silicon wafers. It was demonstrated that the doping profile can be varied by doping through a silicon oxide layer. Two main points need to be studied further: (1) the doping level required in micropillar solar cells applications $>10^{20} \text{ cm}^{-3}$ which is $\approx 5\%$ concentration of phosphorus. The above experiments show a doping level greater than 9%. Detecting a doping level of 5% and below might be challenging with the XPS. Another tool, such as the Atomic Probe Topography or Secondary Ion Mass Spectroscopy, is recommended; (2) the second point is whether activation of phosphorus is achieved by the rapid thermal annealing. In order for a p–n junction to form, the phosphorus has to be part of the silicon lattice in order to form a covalent bond. One possible solution is to increase the thickness of the SiO_2 layer so that the lower concentration of phosphorus penetrates silicon. Experimenting with changing the SiO_2 layer thickness and measuring the I–V curve to obtain information about the nature of the junction and type of contact is recommended as the next step.

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