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Two-Phase Interleaved Boost Converter with ZVT Turn-On for Main Switches and ZCS Turn-Off for Auxiliary Switches Based on One Resonant Loop

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Received: 12 May 2020; Accepted: 1 June 2020; Published: 3 June 2020

Abstract: A two-phase interleaved boost converter with soft switching is proposed herein. By means of only one auxiliary circuit with two auxiliary switches having zero-current switching (ZCS) turn-on, two main switches are switched on with zero-voltage transition (ZVT) to enhance the overall efficiency. Moreover, a current-balancing circuit with a no current-balancing bus is utilized to render the load current extracted from the two phases as even as possible, so that the system stability is upgraded. In such a study, this converter, having the input of $24V \pm 10\%$ and the rated output of 36V/6A, was employed to demonstrate the effectiveness of such a converter by experiment.

Keywords: boost converter; current balancing; two-phase; interleaved control; ZVT; ZCS

1. Introduction

As well known, the switching power supply is widely used today. This is because of its small volume, high efficiency, etc. However, it has some disadvantages due to its hard switching, such as high switching loss, large voltage/current stress and strong electromagnetic interference.

To overcome the demerits mentioned above, the quasi-resonant converter (QRC) [1–6] has been investigated since 1980, mainly on the condition that the voltage/current waveform is sinusoidal. This converter contains the resonant inductor in a series with the switch or the diode, and hence resonates with the switch parasitic capacitor or the diode parasitic capacitor so that the zero-voltage switching (ZVS) during the turn-on period or the zero-current switching (ZCS) during the turn-off period can be realized. However, this inductor locates on the path of the main power stage such that the high voltage/current on/in the switch or diode will occur and hence the circulation current is unavoidable, thereby creating a large conduction loss. Moreover, the resonant energy comes from the input and the load such that the soft switching can be achieved only for some input voltage range as well as some load range.

To overcome the demerits of QRCs, a resonant network paralleled with the main power stage path was developed. Some derived structures were presented, such as active clamp [7–21], zero-voltage transition (ZVT) and zero-current transition (ZCT) [22–33]. The last two structures use resonant networks, which will make the main switch have ZVS and ZCS according to the auxiliary switch. Furthermore, the voltage on the switch and the current in the switch are of sinusoidal form. By doing so, the voltage stress and current stress for the switch are effectively alleviated, causing the circulation

current to be small and hence the unavoidable conduction loss to be reduced. Moreover, the required resonant energy is not all determined by the input voltage and output load. Accordingly, in design of the resonant parameters for soft switching all over the range of input voltage and output load, only the minimum input voltage and the maximum output load were considered.

On the other hand, to increase the output current as well as to upgrade the corresponding overall efficiency, the multiphase converter along with interleaved control are commonly utilized. Since the AC components of the inductor currents for multiple phases are cancelled with each other to some extent, not only is the output current ripple thereby decreased but also the frequency of the output current ripple is increased. Accordingly, not only will the design of the required filter be easier, but the corresponding size will also be smaller. Generally, the total loss generated from multiple phases will be smaller than that generated from one phase. Furthermore, the soft switching multiphase converter is proposed so that the overall efficiency is further upgraded. The literature [34–37] takes multiple phases with the accompanying number of auxiliary resonance circuits, thereby resulting in increasing the number of components and hence increasing not only the conduction loss but also the cost. In the literature [36], the two-phase converter utilizes the same auxiliary resonant circuit. However, only the ZVS is employed so that the improvement in efficiency is restricted. In the literature [37], a two-phase converter adopts one snubber circuit to force the main switches to realize soft switching. Nevertheless, the resonant inductor is put on the power path, thus increasing the conduction loss. In addition, since there are differences in component features and line impedance between the two phases, the current-balancing control will be required. Regarding current balance, there are two types of current-balancing control strategies. One method is passive; the other method is active. The former adopts differential-mode transformers or capacitors or both to do current balance [38–41], while the latter consists of current regulators and sensors to do current balance [42–46].

Accordingly, only one resonant circuit, which is comprised of relatively few elements as compared with [47] is presented and imposed on a two-phase interleaved boost converter to force two main switches to have ZVT turn-on and two auxiliary switches to have ZCS turn-off. Moreover, as the switches operate under soft switching, the output current ripple is not affected such that the life of the capacitor can be prolonged. As for the current balance, a simple method, based on digital control with no current-balancing bus, is proposed to render the load current evenly distributed between the two phases.

2. Proposed Converter

Figure 1 shows the proposed converter containing a traditional two-phase boost converter with the parasitic diodes D_{S1} and D_{S2} and parasitic capacitors C_{S1} and C_{S2} for the main switches S_1 and S_2 , respectively, the output diodes D_1 and D_2 , and one output capacitor C_o , along with a resonant circuit, which is composed of only one resonant inductor L_r , only one resonant capacitor C_r , one resonant diode D_r , and two auxiliary switches S_a and S_b with parasitic diodes D_{Sa} and D_{Sb} and parasitic capacitors C_{Sa} and C_{Sb} , respectively. Moreover, the output resistor is indicated by R .

Figure 1. Proposed circuit.

3. Operation Behavior

Before tackling this section, there are some assumptions and symbols to be given as below: (i) all the elements are viewed as ideal except the parasitic diodes and capacitors for the main switches and auxiliary switches; (ii) the input inductors can be regarded as current sources represented by I_{L1} and I_{L2} ; (iii) the output capacitor can be viewed as a voltage source V_o ; (iv) this converter operates in the continuous current mode (CCM); (v) the gate-driving signals for the switches S_1 , S_2 , S_a and S_b are denoted by v_{g1} , v_{g2} , v_{ga} and v_{gb} , respectively; (vi) the voltages across the switches S_1 , S_2 , S_a and S_b are signified by v_{S1} , v_{S2} , v_{Sa} and v_{Sb} , respectively; (vii) the currents flowing through the switches S_1 , S_2 , S_a and S_b are represented by i_{S1} , i_{S2} , i_{Sa} and i_{Sb} , respectively; (viii) the currents flowing through D_1 , D_2 and D_r are indicated by i_{D1} , i_{D2} and i_{Dr} , respectively; (ix) the current flowing through L_r and the voltage across C_r are denoted by i_{Lr} and v_{Cr} , respectively.

According to the aforementioned assumptions and symbols, the converter in Figure 2 is an equivalent for that in Figure 1. In Figure 3, there are sixteen operation modes in this circuit. Since such a converter is controlled by interleave, namely, the gate-driving signal v_{g2} shifted by 180 degrees from the gate-driving signal v_{g1} , the behavior of the first eight operation modes is identical to that of the last eight operation modes. Hence, only the first eight operation modes are illustrated.

Figure 2. Equivalent circuit.

Figure 3. Illustrated waveforms.

Mode 1: $[t_0 \leq t \leq t_1]$. As in Figure 4, the auxiliary switch S_a is switched on at the instant t_0 . Since the output diodes D_1 and D_2 are also switched on, thereby making the parasitic capacitor of S_b , called C_{Sb} , abruptly discharged to zero. Meanwhile, the output voltage V_o was imposed on the resonant inductor L_r and the resonant capacitor C_r , thereby making L_r and C_r resonate. Moreover, the current i_{Sa} is equal to i_{Lr} and both are increasing, but the current i_{D1} begins to fall. As soon as i_{Lr} is equal to I_{L1} , namely $i_{Lr}(t_1) = I_{L1}$, this mode ends. During such a mode, the accompanying equations are described as below:

$$\begin{cases} i_{Lr}(t) = \frac{(V_o - v_{Cr}(t_0))}{Z_1} \sin(\omega_1(t - t_0)) + i_{Lr}(t_0) \cos(\omega_1(t - t_0)) \\ v_{Cr}(t) = V_o - (V_o - v_{Cr}(t_0)) \cos(\omega_1(t - t_0)) + i_{Lr}(t_0) Z_1 \sin(\omega_1(t - t_0)) \end{cases} \quad (1)$$

where

$$\omega_1 = \sqrt{\frac{1}{L_r C_r}} \text{ and } Z_1 = \sqrt{\frac{L_r}{C_r}} \quad (2)$$

At the instant t_0 , $i_{Lr}(t_0)$ is close to zero and $v_{Cr}(t_0)$ is much smaller than V_o , so the expression of the current i_{Lr} from Equation (1) can be approximately represented by

$$i_{Lr}(t) = \frac{V_o}{Z_1} \sin(\omega_1(t - t_0)) \quad (3)$$

From Equation (3), the elapsed time for this mode can be obtained to be

$$(t_1 - t_0) = \frac{1}{\omega_1} \sin^{-1} \left[\frac{I_{L1} Z_1}{V_o} \right] \quad (4)$$

Figure 4. Current path in mode 1.

Mode 2: $[t_1 \leq t \leq t_2]$. As in Figure 5, the output diode D_1 is switched off. Meanwhile, the current I_{L2} charges the parasitic capacitor of the auxiliary switch S_b , called C_{Sb} , to the output voltage V_o abruptly, while the resonant inductor L_r resonates with the resonant capacitor C_r in series with the parasitic capacitor of the main switch S_1 , called C_{S1} . Since the current i_{Sa} is equal to i_{Lr} , the current I_{L1} is the sum of the currents of i_{Lr} and i_{S1} . Therefore, I_{Lr} will force C_{S1} to discharge, thereby causing the voltage across S_1 , called v_{S1} , to be dropped. As soon as v_{S1} is zero, this mode ends. During such a mode, the accompanying equations are described as below:

$$\begin{cases} i_{Lr}(t) = \frac{V_1}{Z_2} \sin(\omega_2(t - t_1)) + I_1 \cos(\omega_2(t - t_1)) - I_1 + i_{Lr}(t_1) \\ v_{S1}(t) = \frac{C}{C_{S1}} (V_1 \cos(\omega_2(t - t_1)) - I_1 Z_2 \sin(\omega_2(t - t_1)) - V_1) + \\ \frac{I_{L1}}{C_r + C_{S1}} (t - t_1) + V_o \\ v_{Cr}(t) = -\frac{C}{C_r} (V_1 \cos(\omega_2(t - t_1)) - I_1 Z_2 \sin(\omega_2(t - t_1)) - V_1) + \\ \frac{I_{L1}}{C_r + C_{S1}} (t - t_1) + v_{Cr}(t_1) \end{cases} \quad (5)$$

where

$$C = \frac{C_r C_{S1}}{C_r + C_{S1}}, \quad \omega_2 = \sqrt{\frac{1}{L_r C}} = \sqrt{\frac{C_r + C_{S1}}{L_r C_r C_{S1}}}$$

$$Z_2 = \sqrt{\frac{L_r}{C}} = \sqrt{\frac{L_r (C_{S1} + C_r)}{C_r C_{S1}}} \quad (6)$$

$$V_1 = V_o - v_{Cr}(t_1), \quad I_1 = i_{Lr}(t_1) - \frac{C}{C_{S1}} I_{L1}$$

As the voltage v_{S1} is identical to the voltage v_{Cr} , the resonant current i_{Lr} , which flows through the auxiliary switch S_a , will be a maximum value, called $I_{Lr-peak}$, which can be expressed as

$$I_{Lr-peak} = \frac{\sqrt{V_1^2 + (I_1 Z_2)^2}}{Z_2} + \frac{C}{C_{S1}} I_{L1} \quad (7)$$

Figure 5. Current path in mode 2.

Mode 3: $[t_2 \leq t \leq t_3]$. As in Figure 6, the voltage across S_1 , called v_{S1} , is zero due to the parasitic diode of the switch S_1 , called D_{S1} , conducting the current. Therefore, as S_1 is switched on during this mode, S_1 has ZVT turn-on without conduction. Since L_r resonates with C_r , the voltage on L_r is identical to the minus voltage across C_r , thereby causing i_{Lr} to begin to drop. Moreover, the current I_{L1} is the sum of the currents of i_{Lr} , i_{S1} and i_{Dr} . As soon as i_{Lr} drops to I_{L1} , this mode ends. During such a mode, the accompanying equations are described as below:

$$\begin{cases} i_{Lr}(t) = i_{Lr}(t_2) \cos(\omega_1(t - t_2)) - \frac{v_{Cr}(t_2)}{Z_1} \sin(\omega_1(t - t_2)) \\ v_{Cr}(t) = v_{Cr}(t_2) \cos(\omega_1(t - t_2)) + i_{Lr}(t_2) Z_1 \sin(\omega_1(t - t_2)) \end{cases} \quad (8)$$

Figure 6. Current path in mode 3.

Mode 4: $[t_3 \leq t \leq t_4]$. As in Figure 7, the current i_{Lr} is equal to the current I_{L1} at the instant t_3 , and hence both the currents i_{S1} and i_{Dr} are zero, thereby causing the diodes D_{S1} and D_r to be switched off. During this mode, the main switch S_1 is switched on with conduction. Meanwhile, the resonant inductor L_r still resonates with the resonant capacitor C_r , and i_{Lr} is still reduced, but i_{S1} increases from zero gradually. Moreover, the current I_{L1} is the sum of the currents i_{S1} and i_{Sa} , and i_{Sa} is identical to i_{Lr} . As i_{Lr} drops to zero, the auxiliary switch S_a is switched off, thereby causing S_a to operate under ZCS turn-off. As soon as i_{Lr} is identical to zero, this mode ends.

Figure 7. Current path in mode 4.

Mode 5: $[t_4 \leq t \leq t_5]$. As in Figure 8, the main switch S_1 remains switched on. During this mode, the resonant inductor L_r still keeps resonating with the resonant capacitor C_r , and the current i_{Lr} increases in the negative direction and flows through S_1 , thereby making the parasitic diode of the auxiliary switch S_a , called D_{Sa} , switched on. Moreover, as soon as i_{Lr} goes from the minimum value to zero, this mode ends.

Figure 8. Current path in mode 5.

Mode 6: $[t_5 \leq t \leq t_6]$. As in Figure 9, the main switch S_1 still remains switched on. During this mode, the resonant inductor L_r , with its current in the positive direction, resonates with the resonant capacitor C_r , thereby making the resonant diode D_r switched on and hence a resonant loop is generated. Moreover, the current in the main switch S_1 , called i_{S1} , is identical to the current I_{L1} . As soon as S_1 is switched off, this mode ends.

Mode 7: $[t_6 \leq t \leq t_7]$. As in Figure 10, the main switch S_1 is switched off at the instant t_6 . During this mode, the current I_{L1} charges the parasitic capacitor of the main switch S_1 , called C_{S1} , and the parasitic capacitor of the auxiliary switch S_a , called C_{Sa} , causing the voltage across S_1 to be increased. Moreover, the resonant loop is the same as that displayed in mode 6. As soon as the voltage v_{S1} is identical to the output voltage V_o , this mode ends.

Figure 9. Current path in mode 6.

Figure 10. Current path in mode 7.

Mode 8: $[t_7 \leq t \leq t_8]$. As in Figure 11, during this mode, all the switches are switched off, but only the output diode D_1 conducts with the current i_{D1} identical to the current I_{L1} . Moreover, the resonant loop is the same as that displayed in mode 7. As soon as the main switch S_b is switched on, this mode ends, and hence the other phase begins to work, coming back to state 1 until this cycle is finished. After this, the next period will be repeated.

Figure 11. Current path in mode 8.

4. Current Control Strategy

Figure 12 displays the proposed current-balancing control strategy. The duty cycle of the gate-driving signal v_{g1} for the first phase after the first pulse-width modulation (PWM) generator is tuned to get the wanted output voltage V_o , based on the voltage loop with the controller $G_{c1}(z)$ having the voltage command reference V_{ref} and the digital sensed voltage V_o' , which is obtained from the

sensed voltage v'_o by the voltage divider with a gain k and the first analog-to-digital converter (ADC1). Meanwhile, the sensed current of the first phase, named i'_{L1} , is sent to ADC2, to get the digital sensed current I'_{L1} , which will be used as the current command reference for the current-balancing loop with the controller $G_{c2}(z)$ having the digital sensed current I'_{L2} from the sensed current of the second phase, named i'_{L2} , after ADC3, so that the duty cycle of the gate-driving signal v_{g2} for the second phase after the second PWM generator is automatically tuned to force the input current to be evenly distributed between the two phases and hence the load current balancing between the two phases can be realized.

Afterwards, the current-balancing behavior is described below. First, by assuming that the output power (P_o) is identical to the input power (P_i), the output current (I_o) is identical to the product of the DC inductor current (I_L) and one minus duty cycle ($1-D$). Therefore, if $I_L = I_{L1} + I_{L2}$ and $I_o = I_{o1} + I_{o2}$, then under $I_{L1} = I_{L2} = 0.5I_L$, $I_o = 0.5I_{L1}(1-D_a) + 0.5I_{L2}(1-D_b)$, where D_a is the duty cycle of v_{g1} generated from the controller $G_{c1}(z)$ and D_b is the duty cycle of v_{g2} generated from the controller $G_{c2}(z)$. For example, if I_{o1} is larger than I_{o2} , then D_a will be increased and D_b will be decreased, thereby causing I_{o1} to go down and I_{o2} to go up. Eventually, both I_{o1} and I_{o2} are equal to $0.5 I_o$, making the current balancing realized.

Figure 12. Proposed current-balancing control strategy (ADC: analog-to-digital converter; PWM: pulse-width modulation).

5. Design Considerations

Prior to designing the key parameters of this converter, the associated specifications of the system are shown in Table 1.

Table 1. System Specifications (CCM: continuous current mode)

System Parameters	Specifications
Operating Mode	CCM
Input Voltage	24 V
Switching Frequency	50 kHz
Output Voltage	36 V
Rated Output Power/Current	216W/6A
Min. Output Power/Current	21.6W/0.6A

5.1. Design of L_1 and L_2

Since this converter is a two-phase structure, the values of the input inductors can be approximately decided by a single phase with the rated output power/current reduced by a factor of 2. Moreover, the converter operates in the CCM, so the minimum value of L_1 , called $L_{1, min}$, can be represented by

$$L_1 \geq \frac{RD_a(1-D_a)^2T_s}{2} \quad (9)$$

where R is the output resistor, whose value is located between 12Ω and 120Ω .

Based on (9), the maximum duty cycle is obtained to be 0.33, which corresponds to the input voltage of 24 V and the output voltage of 36 V. Therefore, $L_{1, \min} = 178 \mu\text{H}$ after some calculations, and eventually the value of L_1 is chosen to be $200 \mu\text{H}$, which is also for the value of L_2 .

5.2. Design of C_o

Regarding the output capacitor design, Equation (11) is used on condition that the maximum output voltage ripple is equal to 20% of the output voltage V_o , the value of R is 12Ω , T_s is $20 \mu\text{s}$, $D = 0.33$, and $V_o = 36 \text{ V}$. After some calculations, the value of C_o is larger than $275 \mu\text{F}$. Eventually, a $470 \mu\text{F}$ capacitor is chosen, and this is because the value of the electrolytic capacitor will be decreased if the frequency is increased:

$$\Delta v_o = \Delta v_{C_o} = \frac{1}{C_o} \int_0^{DT_s} i_{C_o} dt = \frac{I_o DT_s}{C_o} = \frac{V_o DT_s}{RC_o} \quad (10)$$

5.3. Design of L_r and C_r

The proposed soft switching structure is based on the turn-on of the auxiliary switch S_a prior to the turn-on of the main switch S_1 , so that the resonant inductor L_r resonates with the resonant capacitor C_r and the parasitic capacitor of S_1 , called C_{S1} . As the current i_{L_r} is larger than the current I_{L1} , the voltage across S_1 , called v_{S1} , drops to zero abruptly, the parasitic diode of S_1 , called D_{S1} , is switched on, and afterwards S_1 is switched on with ZVT. To avoid the converter operating abnormally, the time interval, used to execute resonance, is not too long. Therefore, the turn-on time interval of the auxiliary switch S_a is chosen to be one tenth of the switching period T_s , about $2 \mu\text{s}$. Meanwhile, to reduce the effect of i_{L_r} on S_1 , the turn-on instant of S_a is prior to the turn-on instant of S_1 by one fifth of the turn-on time interval of S_a , namely $0.4 \mu\text{s}$. Hence, to obtain the soft switching of S_1 , the time interval for v_{S1} to drop to zero is chosen to be $0.5 \mu\text{s}$ or less as shown in (11):

$$(t_1 - t_0) + (t_2 - t_1) \leq 0.5 \mu\text{s} \quad (11)$$

where during the time interval between t_1 and t_0 , the resonant current i_{L_r} rises from zero to the current I_{L1} , whereas during the time interval between t_2 and t_1 , the voltage across S_1 drops from the output voltage V_o to zero.

In Equation (11), the former time interval was quite significantly larger than the latter time interval, so the former time interval at a rated load is set at half of the time interval between the turn-on instant of S_a and the turn-on instant of S_1 , namely $0.2 \mu\text{s}$, so as to make sure that S_1 can operate under ZVT turn-on within the time interval of $0.5 \mu\text{s}$. Therefore, the following equation can be obtained to be:

$$(t_1 - t_0) = \frac{1}{\omega_1} \sin^{-1} \left[\frac{I_{L1} Z_1}{V_o} \right] = 0.2 \mu\text{s} \quad (12)$$

To make sure that the resonant period of the auxiliary circuit, called T_1 , can make the ZVS turn-on of the main switches S_1 and S_2 happen within the switching period T_s , T_1 is set at $0.75 T_s$, equal to $7.5 \mu\text{s}$, and afterwards, based on (12), the values of L_r and C_r can be determined to be $1.25 \mu\text{H}$ and $1.14 \mu\text{F}$.

6. Experimental Results

To verify the performance of the proposed soft switching control strategy, the waveforms of the converter operating at minimum and rated loads are given. Figures 13–23 are for the converter

operating at a minimum load, whereas Figures 24–34 are for the converter operating at a rated load. Figure 13 displays v_{g1} and v_{g2} for S_1 and S_2 , respectively. Figure 14 displays v_{g1} and v_{ga} for S_1 and S_a , respectively, whereas Figure 15 shows v_{g2} and v_{gb} for S_2 and S_b , respectively. Figure 16 displays i_{Lr} and v_{Cr} . Figure 17 shows v_{S1} , i_{L1} and i_{Lr} . Figure 18 displays v_{S2} , i_{L2} and i_{Lr} . Figure 19 shows v_{g1} , v_{S1} and i_{S1} . Figure 20 displays v_{g2} , v_{S2} and i_{S2} . Figure 21 displays v_{ga} , v_{Sa} and i_{Sa} . Figure 22 displays v_{gb} , v_{Sb} and i_{Sb} . Figure 23 shows the current balancing between the two phases. As for Figures 24–34, the measured items are the same as those for Figures 13–23.

Figure 13. Waveforms pertaining to S_1 and S_a at the minimum load: (1) v_{g1} ; and (2) v_{g2} .

Figure 14. Waveforms pertaining to S_1 and S_a at the minimum load: (1) v_{g1} ; and (2) v_{ga} .

Figure 15. Waveforms pertaining to S_2 and S_b evenly at the minimum load: (1) v_{g2} ; and (2) v_{gb} .

Figure 16. Waveforms pertaining to L_r and C_r at the minimum load: (1) i_{Lr} ; and (2) v_{Cr} .

Figure 17. Waveforms pertaining to S_1 , L_1 and L_r at the minimum load: (1) v_{S1} ; (2) i_{L1} ; and (3) i_{Lr} .

Figure 18. Waveforms pertaining to S_2 , L_2 and L_r at the minimum load: (1) v_{S2} ; (2) i_{L2} ; and (3) i_{Lr} .

Figure 19. Waveforms pertaining to S_1 at the minimum load: (1) v_{G1} ; (2) v_{S1} ; and (3) i_{S1} .

Figure 20. Waveforms pertaining to S_2 at the minimum load: (1) v_{G2} ; (2) v_{S2} ; and (3) i_{S2} .

From Figures 13–24, we can see that v_{G2} is shifted from v_{G1} by 180 degrees. From Figures 14 and 25, S_a is switched on before S_1 is switched on, whereas from Figures 15 and 26, we can see that S_b is switched on before S_2 is switched on. In Figures 16 and 27, we can see that L_r resonates with C_r . From Figures 17 and 28, we can see that as S_a is switched on prior to S_1 , i_{Lr} is rising abruptly and then is larger than i_{L1} , causing the voltage across C_{S1} to be dropped to zero and then S_1 to be switched on with ZVT, whereas from Figures 18 and 29, we can see that as S_b is switched on prior to S_2 , i_{Lr} is rising

abruptly and then is larger than i_{L2} , causing the voltage across C_{S2} to be dropped to zero and then S_2 to be switched on with ZVT. From Figures 19 and 30, we can see that S_1 has ZVT turn-on, whereas from Figures 20 and 31, we can see that S_2 has ZVT turn-on. From Figures 21 and 32, we can see that due to resonance, i_{Sa} is dropped to zero and then clamped at zero, thereby making S_a switched off with ZCS, whereas from Figures 22 and 33, we can see that due to resonance, i_{Sb} is dropped to zero and then clamped at zero, thereby making S_b switched off with ZCS. From Figures 23 and 34, we can see that the current balancing between the two phases performs well for any load.

Figure 21. Waveforms pertaining to S_a at the minimum load: (1) v_{ga} ; (2) v_{Sa} ; and (3) i_{Sa} .

Figure 22. Waveforms pertaining to S_b at the minimum load: (1) v_{gb} ; (2) v_{Sb} ; and (3) i_{Sb} .

Figure 23. Waveforms pertaining to current balancing at the minimum load: (1) v_{S1} ; (2) v_{S2} ; (3) i_{L1} ; and (4) i_{L2} .

From Figures 13–35, we can know that all over the load range, both the main switches have ZVT turn-on and both the auxiliary switches have ZCS turn-off.

Figure 24. Waveforms pertaining to S_1 and S_a at the rated load: (1) v_{g1} ; and (2) v_{g2} .

Figure 25. Waveforms pertaining to S_1 and S_a at the rated load: (1) v_{g1} ; and (2) v_{ga} .

Figure 26. Waveforms pertaining to S_2 and S_b at the rated load: (1) v_{g2} ; and (2) v_{gb} .

Figure 27. Waveforms pertaining to L_r and C_r at the rated load: (1) i_{Lr} ; and (2) v_{Cr} .

Figure 28. Waveforms pertaining to S_1 , L_1 and L_r at the rated load: (1) v_{S1} ; (2) i_{L1} ; and (3) i_{Lr} .

Figure 29. Waveforms pertaining to S_2 , L_2 and L_r at the rated load: (1) v_{S2} ; (2) i_{L2} ; and (3) i_{Lr} .

Figure 30. Waveforms pertaining to S_1 at the rated load: (1) v_{G1} ; (2) v_{S1} ; and (3) i_{S1} .

Figure 31. Waveforms pertaining to S_2 at the rated load: (1) v_{G2} ; (2) v_{S2} ; the (3) i_{S2} .

Figure 32. Waveforms pertaining to S_a at the rated load: (1) v_{ga} ; (2) v_{sa} ; and (3) i_{sa} .

Figure 33. Waveforms pertaining to S_b at the rated load: (1) v_{gb} ; (2) v_{sb} ; and (3) i_{sb} .

Figure 34. Waveforms pertaining to current balancing at the rated load: (1) v_{s1} ; (2) v_{s2} ; (3) i_{L1} ; and (4) i_{L2} .

Figure 35. Efficiency vs. load current.

7. Comparisons

In Table 2, the numbers of resonant components are five, seven and five for the circuits from [37] and [47], and the proposed circuits, respectively. The circuit shown in [37] has ZCT turn-on and ZVT turn-off. The circuit displayed in [47] has ZVT turn-on and ZCT turn-off. The proposed circuit has ZVT turn-on. The minimum values of the overall efficiency are 84%, 91% and 94% for the circuits [37]

and [47], and the proposed, respectively. The circuit [47] has ZVT turn-on and ZCT turn-off but the number of resonant components is seven, whereas the proposed circuit only has ZVT turn-on, but the number of resonant components is five. In general, the ZVS turn-on or ZVT turn-on is quite important for reducing the switching loss of the metal-oxide-semiconductor field-effect transistor (MOSFET) [48]. Accordingly, the proposed circuit has the best performance among the three.

Table 2. Comparisons between the circuits from [37], [47] and the proposed circuits (ZVS: zero-voltage switching; ZVT: zero-voltage transition; ZCS: zero-current switching; ZCT: zero-current transition).

Comparisons	Resonant Count No.	Soft Switching Type for Main Switches								Overall Efficiency	
		ZVS	ZVT	ZCS	ZCT	ZVS	ZVT	ZCS	ZCT	Min.	Max.
[37]	5				*		*			84%	90%
[47]	7		*						*	91%	93%
Proposed	5		*							94%	96%

The sign * means that the converter possesses this soft switching type.

8. Conclusions

In this paper, to reduce the switching loss as well as to upgrade the overall efficiency, the proposed converter with the main switches S_1 and S_2 had ZVT turn-on as well as the auxiliary switches S_a and S_b having ZCS turn-off. All the soft switching operations are achieved based on only one resonant loop. The ZVT behavior is realized by switching on the auxiliary switch S_a (or S_b) before the main switch S_1 (or S_2) is switched on, so that the voltage across S_1 (or S_2) is dropped to zero and hence S_1 (or S_2) has an ZVT turn-on. On the other hand, the ZCS behavior was achieved based on the characteristics of the auxiliary circuit, so that S_a and S_b have a ZCS turn-off. From the experimental results, we can know that soft switching can be realized all over the load range. In addition, the current balancing between the two phases is performed well for any load.

Author Contributions: Conceptualization, Y.-T.Y.; methodology, K.-I.H.; software, W.-Z.J.; validation, W.-Z.J.; formal analysis, W.-Z.J.; investigation, Y.-T.Y.; resources, K.-I.H.; data curation, Y.-T.Y.; writing—original draft preparation, K.-I.H.; writing—review and editing, K.-I.H.; visualization, Y.-T.Y.; supervision, K.-I.H.; project administration, K.-I.H.; funding acquisition, K.-I.H. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Ministry of Science and Technology, Taiwan, under the Grant Number: MOST 108-2221-E-027-051.

Acknowledgments: The authors gratefully acknowledge the support of the Ministry of Science and Technology, Taiwan, under the Grant Number MOST 108-2221-E-027-051.

Conflicts of Interest: The authors declare no conflict of interest with commerce.

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