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Improvement of Electrical Performance in Heterostructure Junctionless TFET Based on Dual Material Gate

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Abstract: In this paper, a dual metallic material gate heterostructure junctionless tunnel field-effect transistor (DMMG-HJLTFET) is proposed and investigated. We use the Si/SiGe heterostructure at the source/channel interface to improve the band to band tunneling (BTBT) rate, and introduce a sandwich stack (GaAs/Si/GaAs) at the drain region to suppress the OFF-state current and ambiplolar current. Simultaneously, to further decrease ambipolar current, the gate electrode is divided into three parts namely auxiliary gate (M1), control gate (M2), and tunnel gate (M3) with workfunctions Φ_{M1}, Φ_{M2} and Φ_{M3}, respectively, where $\Phi_{M1} = \Phi_{M3} < \Phi_{M2}$. Simulation results indicate that DMMG-HJLTFET provides superior performance in terms of logic and analog/RF as compared with other possible combinations, the ON-state current of the DMMG-HJLTFET increases up to 9.04×10^{-6} A/μm, and the maximum g_m (which determine the analog performance of devices) of DMMG-HJLTFET is 1.11×10^{-5} S/μm at 1.0V drain-to-source voltage (Vds). Meanwhile, RF performance of devices depends on the cut-off frequency (f_T) and gain bandwidth (GBW), and DMMG-HJLTFET could achieve a maximum f_T of 5.84 GHz, and a maximum GBW of 0.39 GHz, respectively.

Keywords: gate material engineering; band-to-band tunneling (BTBT); a sandwich stack structure (GaAs/Si/GaAs); dual material gate heterostructure junctionless TFET (DMMG-HJLTFET)

1. Introduction

The mechanism of conventional metal oxide semiconductor field effect transistors (MOSFETs) is thermal electron emission, so the continuous scaling of conventional MOS device is extremely difficult in nanoscale circuit because of a great many reasons, such as, VDD scaling of MOSFETs is no longer viable, OFF-state current dramatically increases and short channel effects (SCE) is severely aggravated, and a limitation of 60 mV/Dec subthreshold swing (SS) can't be broken [1,2]. In order to overcome these issues, different types of structure have been investigated in recent years, among them, tunnel field effect transistor (TFET) [3,4] is a selective candidate for future low power applications due to its complementary MOS (CMOS) process compatibility and scalability, which employs band-to-band tunneling (BTBT) mechanism and is not influenced by the short channel effect, moreover, it can break the SS limit of 60 mV/Dec, and the leakage current is small under the OFF-state condition [5–7]. However, there are also inherent disadvantages in TFETs, the most serious problems are small ON-state current and large miller capacitance. To address these issues, a lot of novel structures of TFETs are proposed [8–19]. As a whole, most of TFETs reported in recent years adopt different doping concentration in channel and active regions to form heavily doped abrupt junction at tunneling interface, which leads to a complex fabrication processes and a high thermal budget, what's more,

introduction of high-density layer at source/channel junction and Gaussian doping in drain region also find difficultly during fabrication process and it's easy to be influenced by random dopant fluctuations (RDFs) [20–23].

To avoid the above issues in TFETs, the junctionless tunneling field effect transistor (JLTFET) [24–30] is proposed, which uses a uniformly high-doping concentration in source, channel, and drain region, wherein the doping concentration and type of channel are consistent with source and drain. Therefore, junctionless tunnel field-effect transistor (JLTFET) is immune to random dopant fluctuations (RDFs) [31], while complex fabrication processes and high thermal budgets in JLTFET manufacturing can be effectively avoided by the charge plasma concept. Still, low ON-state current remains the problem in junctionless TFETs due to the presence of a barrier between source and channel. As we know, TFETs use a heavily doped source and a lightly doped channel to make the distance between the source valance band and the channel conduction band as short as possible, so that band to band tunneling from source valance band to channel conduction band will occur at source/channel interface, that is to say, a heavily doped degenerate source is required in TFETs to make the working mechanism of this structure change from hot electron emission to band to band tunneling. In this paper, different doping regions in the uniform doping device are achieved via the charge plasma concept. In this paper, a dual material gate heterostructure junctionless TFET (DMMG-HJLTFET) is proposed and investigated, in which we adopt a uniform doping concentration and a corresponding P^+-N^+-I-N^+ structure can be realized via the charge plasma concept with appropriate work function for polar gate (PG) and control gate (CG). The PG is located at the source region and has a larger work function than CG for inducing a P^+ source while CG is located at the middle for inducing intrinsic channel. We use Si/SiGe heterostructure at the source/channel interface to improve band to band tunneling (BTBT) rate. Meanwhile, a sandwich stack structure (GaAs/Si/GaAs) at the drain region is introduced to suppress the OFF-state current and ambiplolar current. Moreover, based on the gate-engineered concept, the gate electrode is divided into three parts in DMMG-HJLTFET so that the ON-state current and the OFF-state current can be further improved. Si-based integrated circuits are most extensive in nowadays, so DMMG-HJLTFET using Si and SiGe as heterojunction in source/channel interface is proposed. And in order to match the current and performance with the DMGE-HJLTFET in [22], a sandwich stack structure (GaAs/Si/GaAs) in drain region is used in our new design. Through a comprehensive analysis, the DC and AC characteristics of this structure are comparable to DMGE-HJLTFET, and better than similar devices without gate engineering and sandwich structure, whose comparison will be shown in Table 2.

The details will be discussed in following sections: Section 2 describes the device structure and parameters. Section 3 includes the properties of the structure and the optimization process. Section 4 summarizes the article and makes some relevant statements.

2. Methods

Figure 1a shows the device structure of conventional JLTFET, in which the PG is located at the source region and has a larger work function than CG for inducing a P+ source while CG is located at the middle for inducing intrinsic channel, and a heavily doping is considered in silicon body with concentration of 1×10^{19} cm^{-3}, resulting in a junctionless P^+-N^+-I-N^+ structure with appropriate workfunctions for PG and CG by charge plasma concept. Compared with conventional JLTFET, the difference of heterostructure junctionless tunnel field-effect transistor (HJLTFET) is that ON-state current can be improved by heterojunction at source/channel interface, as shown in Figure 1b. Based on conventional HJLTFET, DMMG-HJLTFET still uses Si/SiGe heterostructure at the source/channel interface and introduces a sandwich stack structure (GaAs/Si/GaAs) at drain region to suppress OFF-state current and ambiplolar current, moreover, the gate electrode is divided into three parts namely auxiliary gate (M1), control gate (M2), and tunnel gate (M3) with workfunctions Φ_{M1}, Φ_{M2} and Φ_{M3}, respectively, where $\Phi_{M1} = \Phi_{M3} < \Phi_{M2}$, as shown in Figure 1c. As a result, the DMMG-HJLTFET has a larger ON-state current and lower OFF-state current than JLTFET and HJLTFET, so it is possible

to be applied to low power integrated circuit. Table 1 shows the fundamental geometrical parameters of the different devices.

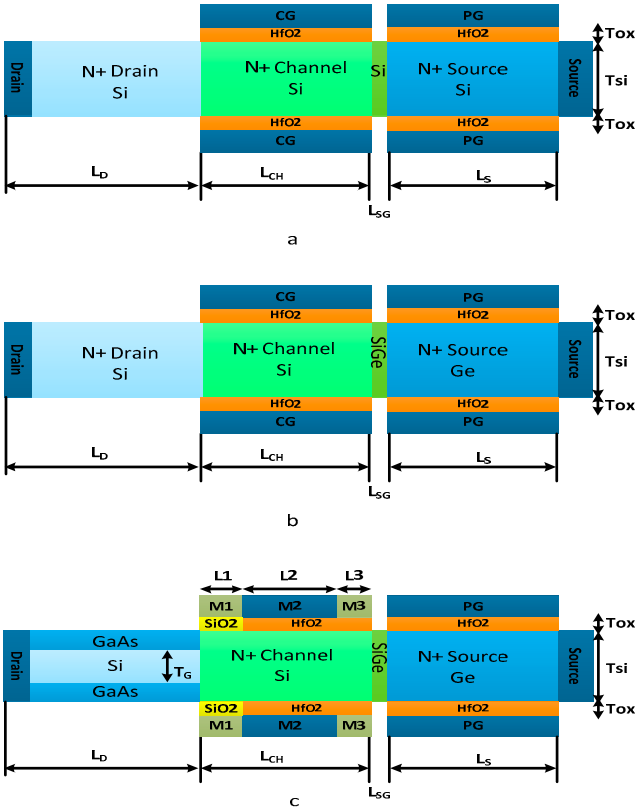


Figure 1. Cross-sectional view of (**a**) JLTFET; (**b**) HJLTFET; (**c**) DMMG-HJLTFET.

Table 1. The fundamental geometrical parameters of the different devices.

Parameter Name	JLTFET	HJLTFET	DMMG-HJLTFET
Length of source (L_S/nm)	20	20	20
Length of channel (L_{CH}/nm)	20	20	20
Length of drain (L_D/nm)	20	20	20
Length of gap (L_{SG}/nm)	5	5	5
Thickness of SiO2 and HfO2(T_{OX}/nm)	2	2	2
Thickness of the silicon body (Tsi/nm)	5	5	5
Thickness of the Si (T_S/nm) in sandwich stack	3	3	3
Length of auxiliary gate(L1/nm)			7
Length of control gate(L2/nm)			10
Length of tunnel gate(L3/nm)			3
Work function of polarity gate(Φ_{PG}/eV)	5.9	5.9	5.9
Work function of control gate(Φ_{CG}/eV)	4.6	4.6	4.6
Work function of auxiliary gate(Φ_{M1}/eV)			4.1
Work function of tunnel gate(Φ_{M3}/eV)			4.1
N-type doping concentration (N_C/cm^{-3})	1×10^{19}	1×10^{19}	1×10^{19}

All the simulations are carried out in Silvaco Atlas 5.20.2.R [32–35]. The nonlocal BTBT model (BBT.NONLOCAL) is used to take into account the spatial variation of the energy bands and the nonlocal generation of electrons and holes. Because of the presence of highly doped channel, Shockley-Read-Hall related to concentration (CONSRH) is used for accounting the minority carrier recombination effects, at the same time, Fermi Statistics (FERMI) and band gap narrowing (BGN) model are also activated to reduce the carrier concentration in the simulation. Moreover, quantum confinement effects due to the increased doping levels and thinner gate oxide in the channel distinctly influence the device

characteristics, so quantum confinement model given by Hansch (HANSCHQM) is also considered in our simulation. Furthermore, tunneling of electrons from the valence band to the conduction band through trap or defect states and phonon assisted tunneling effects of indirect band gap semiconductors can have an important effect on the current, in order to involve these effects, the Schenk model for trap Assisted tunneling (SCHENK.TUNN) and band to band tunneling model given by Schenk (SCHENK.BBT) are also included.

3. Results and Discussion

3.1. The Operating Mechanism of DMMG-HJLTFET

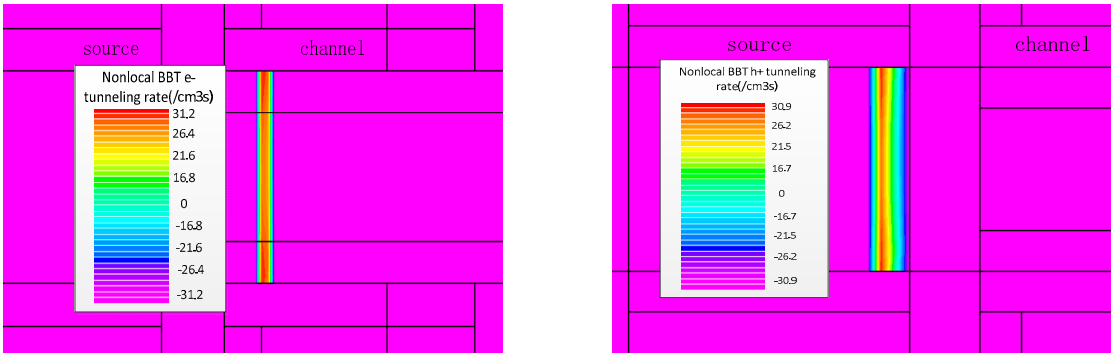
A basic analytical formulation for band to band tunneling probability T (E) is shown in Equation (1):

$$T(E) \propto (-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3|e|h(E_g+\Delta\Phi)}\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{si}t_{ox}})\Delta\Phi \quad (1)$$

where m* is the effective carrier mass, E_g is the bandgap, $\Delta\Phi$ is the energy range over which tunneling can take place, and t_{ox}, t_{si}, ε_{ox}, and ε_{si} are the oxide and silicon film thickness and dielectric constants, respectively. As can be seen from the above formulation that small m*and small E_g in source region is required in the source region, and appropriate materials need to be selected in source/channel interface to ensure the appropriate $\Delta\Phi$.

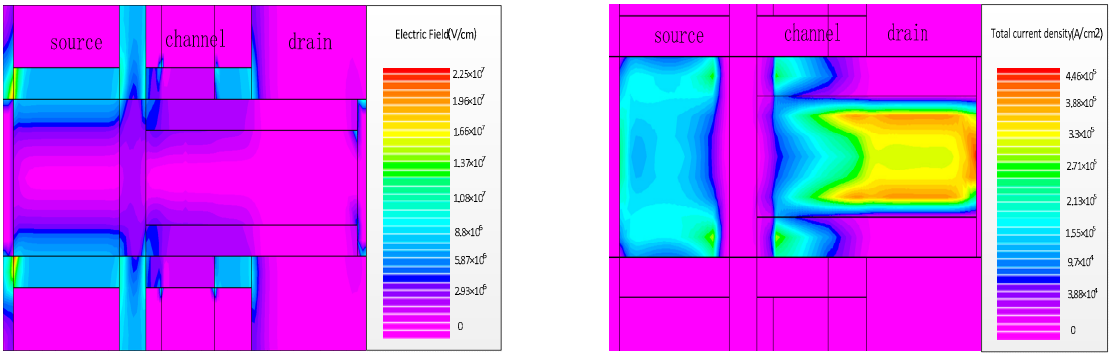
Based on theoretical analysis, we propose a dual material gate heterostructure junctionless TFET (DMMG-HJLTFET) in this paper.

The physical mechanism of DMMG-HJLTFET is explained in Figures 2a–d and 3a,b. Figure 2a,b shows the BTBT rate of electron and hole of DMMG-HJLTFET when Vds = 1 V. It is obvious that BTBT occurs at source and channel interface, and the rate of BTBT increases significantly due to heterojunction between source and channel. Figure 2c shows the electric field distribution when Vgs = 2.0 V and Vds = 1.0 V, it is not difficult to find that the value of electric field is markedly improved near hetero junction and hetero dielectric, resulting in a higher ON-state current and a lower OFF-state current in DMMG-HJLTFET. Figure 2d shows the total current density of DMMG-HJLTFET when Vgs = 2.0 V and Vds = 1.0 V, as can be seen from the Figure 2d, the current mainly flows in the middle region of this device, introducing the sandwich stack structure (GaAs/Si/GaAs) for DMMG-HJLTFET not only guarantees the large ON-state current, but also guarantees the small OFF-state current, which benefits from combining the advantages of silicon and GaAs.



(**a**) (**b**)

Figure 2. *Cont.*



(**c**) (**d**)

Figure 2. (**a**) Nonlocal band to band tunneling (BTBT) rate of electron; (**b**) nonlocal band to band tunneling (BTBT) rate of hole; (**c**) electric field distribution in DMMG-HJLTFET; (**d**) total current density of DMMG-HJLTFET.

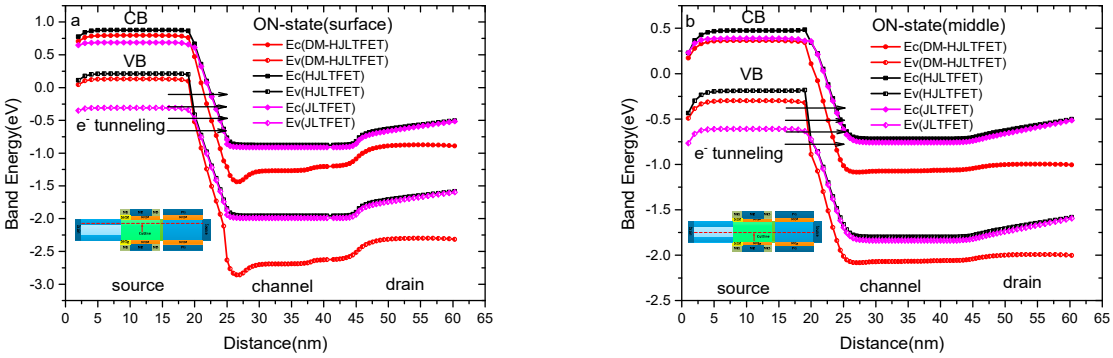


Figure 3. (**a**) The energy band diagram of JLTFET, HJLTFET and DMMG-HJLTFET at the device surface region; (**b**) The energy band diagram of DMMG-HJLTFET at the device middle region.

The comparative analysis among devices JLTFET, HJLTFET and DMMG-HJLTFET for the energy band diagram at the device surface is shown in Figure 3a. From observing this figure, it is not difficult to find that the conduction band and valance band of HJLTFET and DMMG-HJLTFET in the tunneling region are very close to each other, resulting in the tunneling distance of both devices being much smaller than that of JLTFET, this is because both devices employ germanium as their source and a heterojunction is introduced at the channel/source interface, which leads to the tunneling possibilities and ON-state current of HJLTFET and DMMG-HJLTFET being much larger than that of JLTFET. Moreover, the difference in DMMG-HJLTFET is that the gate electrode is divided into three parts namely auxiliary gate (M1), control gate (M2), and tunnel gate (M3), with workfunctions Φ_{M1}, Φ_{M2} and Φ_{M3}, which further improves the tunneling possibilities at channel/source interface and produces an extra barrier height at channel/drain interface in DMMG-HJLTFET. Together with sandwich stack structure (GaAs/Si/GaAs), divided gate electrode obviously increases the ON-state current and decreases the OFF-state current of DMMG-HJLTFET. Figure 3b shows the energy band diagram of JLTFET, HJLTFET and DMMG-HJLTFET at the middle region of the device, as can be seen from this figure, the variation of energy band of source region at the middle is similar to Figure 3a, however, variation of energy band of channel and drain region is very different to Figure 3a. The reason for this is that the extra barrier introduced by divided gate electrode only exists in the surface region of DMMG-HJLTFET.

3.2. The Input Characteristics

The log scale and linear scale transfer characteristics of JLTFET, HJLTFET and DMMG-HJLTFET are illustrated in Figure 4a. It is very clear that DMMG-HJLTFET can generate a higher current

than HJLTFET and JLTFET, the ON-state current of DMMG-HJLTFET is 1.01×10^{-5} A/μm when Vgs = 2.0 V and Vds = 1.0 V, however, the corresponding ON-state currents of HJLTFET and JLTFET are only 3.82×10^{-6} A/μm and 7.21×10^{-7} A/μm, respectively. Moreover, the OFF-state current of DMMG-HJLTFET is much smaller than that of JLTFET and HJLTFET due to a sandwich stack structure (GaAs/Si/GaAs) is introduced at the drain region, which ensures a small OFF-state current in DMMG-HJLTFET on account of large forbidden band width of GaAs.

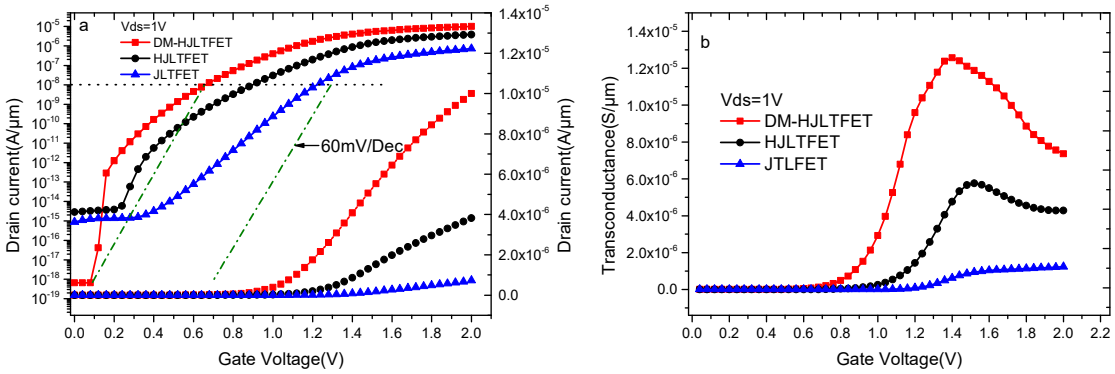


Figure 4. (**a**) The log scale and linear scale transfer characteristics of JLTFET, HJLTFET, and DMMG-HJLTFET; (**b**) transconductance of JLTFET, HJLTFET and DMMG-HJLTFET.

The transconductance (g_m) is an important parameter to evaluate the analog performance of devices. It can be calculated by first derivative of drain current (Ids) with respect to V_{GS}, Equation (2) is the formula of g_m:

$$g_m = \frac{dI_{ds}}{dV_{GS}} \tag{2}$$

Figure 4b shows the transconductance characteristics of JLTFET, HJLTFET and DMMG-HJLTFET. Transconductance of DMMG-HJLTFET increases observably compared with JLTFET and HJLTFET. The maximum transconductance of DMMG-HJLTFET is 1.26×10^{-5} S/μm, while the maximum transconductance of JLTFET and HJLTFET are 1.22×10^{-6} S/μm and 5.76×10^{-6} S/μm.

Including Figure 4a,b, a comparison of the three devices is presented in Table 2. According to Table 2, the value of Ion/Ioff ratio of DMMG-HJLTFET can be reached at 1.56×10^{13}, while the Ion/Ioff ratio of JLTFET and HJLTFET are only 5.3×10^{8} and 1.34×10^{9}, respectively. Moreover, average subthreshold swing(SS) of DMMG-HJLTFET is 52 mV/Dec extracted from Vmin to Vt (Vmin is the gate voltage at which drain current equals to Ioff, the gate voltage at which the drain current becomes 1×10^{8} A/μm is taken as the threshold voltage Vt) under Vds = 1.0 V.

Table 2. Comparison of parameters of JLTFET, HJLTFET and DMMG-HJLTFET.

	Ion (A/μm)	Ioff (A/μm)	Ion/Ioff	g_m (S/μm)	SS (mV/Dec)
JLTFET	7.21×10^{-7}	1.36×10^{-15}	5.3×10^{8}	1.22×10^{-6}	122
HJLTFET	3.82×10^{-6}	2.84×10^{-15}	1.34×10^{9}	5.76×10^{-6}	88.2
DMMG-HJLTFET	1.01×10^{-5}	6.5×10^{-19}	1.56×10^{13}	1.26×10^{-5}	52

3.3. The Output Characteristics

Figure 5a indicates the output characteristics of JLTFET, HJLTFET and DMMG-HJLTFET at Vgs = 1 V, it can be seen clearly that JLTFET shows worse saturation performance under this simulation condition, meanwhile, the maximum ON-state current of JLTFET is only 2.35×10^{-10} A/μm. While HJLTFET and DMMG-HJLTFET have better saturation performance, and the maximum ON-state currents of HJLTFET and DMMG-HJLTFET are 3.01×10^{-8} A/μm and 8.32×10^{-7} A/μm, respectively.

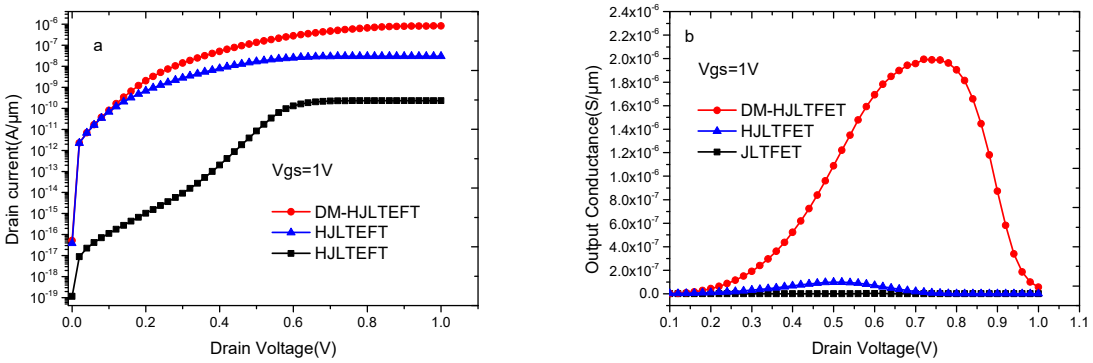


Figure 5. (**a**) Simulated output characteristics and (**b**) Simulated output transconductance of JLTFET, HJLTFET and DMMG-HJLTFET at Vgs = 1 V.

The output transconductance(g_{ds}) is also an important parameter to evaluate the analog performance of devices, and it can be calculated by Equation (3):

$$g_{ds} = \frac{dI_{ds}}{dV_{DS}} \tag{3}$$

Figure 5b shows the output conductance (g_{ds}) characteristics of JLTFET, HJLTFET and DMMG-HJLTFET at Vgs = 1 V. As can be seen from the Figure 5b, output conductance of DMMG-HJLTFET is greater than that of JLTFET and HJLTFET from 0.2 V to 1.0V Vds, and maximum output conductance of DMMG-HJLTFET is 1.99×10^{-6} S/μm when Vds = 0.74 V. However, the maximum output conductance of JLTFET is 1.73×10^{-9} S/μm when Vds = 0.6 V, and the maximum output conductance of HJLTFET is 9.86×10^{-8} S/μm when Vds = 0.52 V.

3.4. Effect of Device Sizes on the Transfer Characteristics

Figure 6a shows the impact of channel doping concentration on transfer characteristics. As shown in this figure, the ON-state current of DMMG-HJLTFET stays at the order of 10^{-6} A/μm at Vds = 2 V when channel doping concentration increases from 1×10^{18} cm^{-3} to 1×10^{19} cm^{-3}. Moreover, the ON-state current of DMMG-HJLTFET increases while the OFF-state current of DMMG-HJLTFET always remains at the order of 10^{-18} A/μm, as a result, the ratio of Ion/Ioff keeps at level of 10^{13} with increase of channel doping concentration as shown in inserted small figure at Figure 6b.Therefore, channel doping concentration is selected as 1×10^{19} cm^{-3} in order to obtain a maximal ON-state current.

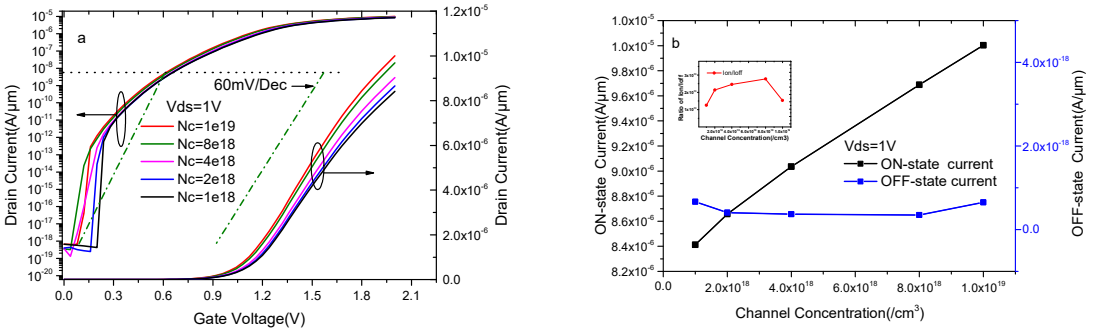


Figure 6. (**a**) Simulated log scale and linear scale transfer characteristics of DMMG-HJLTFET with different channel doping concentration; (**b**) ON-state current, OFF-state current and Ion/Ioff at different channel doping concentration.

Figure 7a shows the impact of polar gate work function(Φ_{PG}) on transfer characteristics with keeping $\Phi_{M1} = \Phi_{M3} = 4.1$ eV and keeping $\Phi_{M2} = 4.6$ eV. As can be seen clearly from the Figure 7a appropriate selection of polar gate work function is required to achieve higher ON-state current, the

ON-state current of DMMG-HJLTFET increases with the increase of polar gate work function while the OFF-state current of DMMG-HJLTFET stays at the order of 10^{-18} A/μm, the reason for this is that polar gate work function has a large influence on the polarization charge formation in source region, as a result, the ON-state current of DMMG-HJLTFET increases with the increase of polar gate work function. Figure 7b shows the variation of energy band with different polar gate work function, the position of conduction band and valance band in the source region increases as the polar gate work function goes up, as illustrated in Figure 7b, which leads to the enhancement of the effective tunneling area at channel/source interface, and further explains the conclusion of Figure 7a.

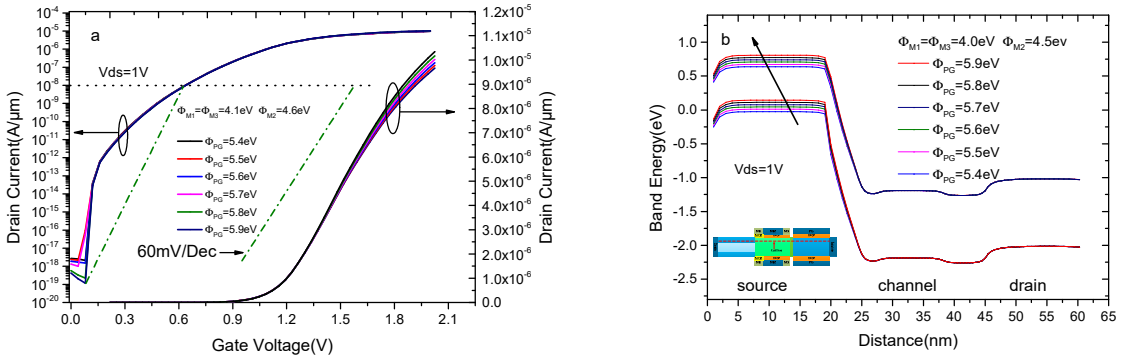
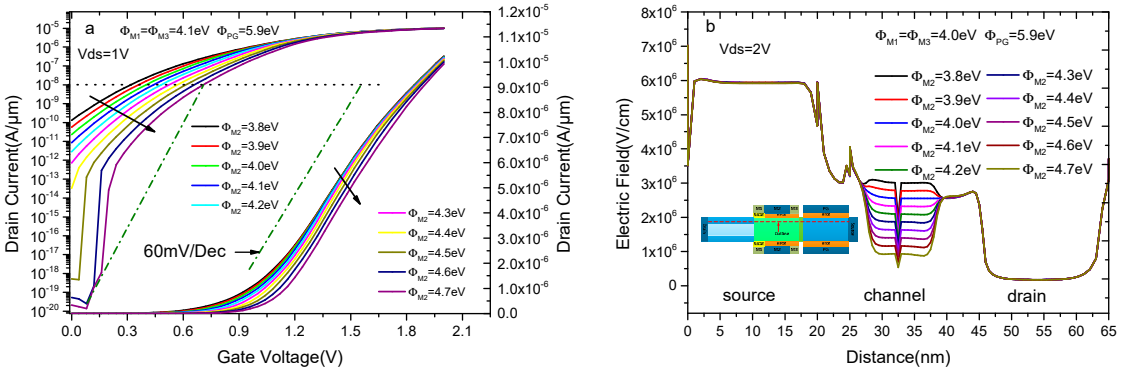


Figure 7. (**a**) Simulated log scale and linear scale transfer characteristics of DMMG-HJLTFET with different polar gate work function (Φ_{PG}); (**b**) the variation of energy band with different polar gate work function (Φ_{PG}).

We mentioned above that the gate electrode is divided into three parts namely auxiliary gate (M1), control gate (M2), and tunnel gate (M3) with work functions Φ_{M1}, Φ_{M2} and Φ_{M3}, respectively, where $\Phi_{M1} = \Phi_{M3} < \Phi_{M2}$.

Figure 8a–d shows the impact of control gate work function(Φ_{M2}) on transfer characteristics, electric field and band diagram with keeping $\Phi_{M1} = \Phi_{M3}$ = 4.1 eV and Φ_{PG} = 5.9 eV. As depicted in Figure 8a, the selection of control gate work function is very important to obtain higher ratio of Ion/Ioff, the ON-state current and the OFF-state current of DMMG-HJLTFET decrease with the increase of control gate work function. The variation of electric field is shown in Figure 8b, it is very clear that value of electric field in channel region increases with the decrease of control gate work function, which makes the surface potential under control gate increase and the energy band bend severely in this region, as shown in Figure 8c,d shows the energy band diagram in OFF-state, where it is observed that tunneling barrier height increases with the increase of control gate work function in the channel region. As a result, the overall performance of the DMMG-HJLTFET is significantly affected by the control gate work function, and the optimal value of the control gate work function is chosen as 4.6 eV.



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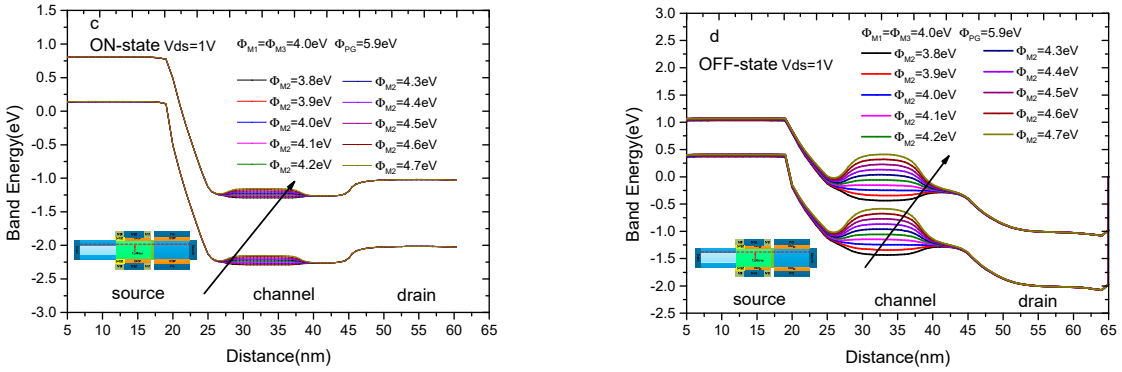

Figure 8. (**a**) Simulated log scale and linear scale transfer characteristics of DMMG-HJLTFET with different control gate work function (Φ_{M2}); (**b**) the distribution of electric field at the surface with different control gate work function (Φ_{M2}); (**c**) the variation of ON-state energy band with different control gate work function (Φ_{M2}); (**d**) the variation of OFF-state energy band with different control gate work function(Φ_{M2}).

Figure 9a–d shows the impact of auxiliary gate work function (Φ_{M1}) and tunnel gate work function (Φ_{M3}) on transfer characteristics, surface potential, electric field and band diagram with keeping Φ_{M2} = 4.6 eV and Φ_{PG} = 5.9 eV. It can be found through the observation of Figure 9a that the ON-state current of DMMG-HJLTFET decreases and the OFF-state current of DMMG-HJLTFET increases with the increase of auxiliary gate work function, i.e., appropriate selection for auxiliary gate work function should be small in terms of ON-state current. At the same time, the surface potential and electric field are also markedly influenced by auxiliary gate work function, as shown in Figure 9b,c, it can be notified that the DMMG-HJLTFET exhibits higher surface potential and electric field at the position of M1 and M3 with small auxiliary gate work function, which helps M1 suppress the ambipolar leakage current and reduce hot carrier effects (HCEs) by diminishing lateral electric field at drain/channel interface together with SiO2 near the drain and helps M3 improve the ON-state current by increasing the tunneling probability at source/ channel interface, as a result, a higher tunneling rate at the source/channel interface and higher barrier height at drain/channel interface are introduced simultaneously, as shown in Figure 9d. So, auxiliary gate work function should be small in terms of ON-state current and OFF-state current, and the auxiliary gate work function should be large in terms of barrier height at drain/channel interface. All things considered, the optimal value of auxiliary gate work function is chosen as 4.1 eV.

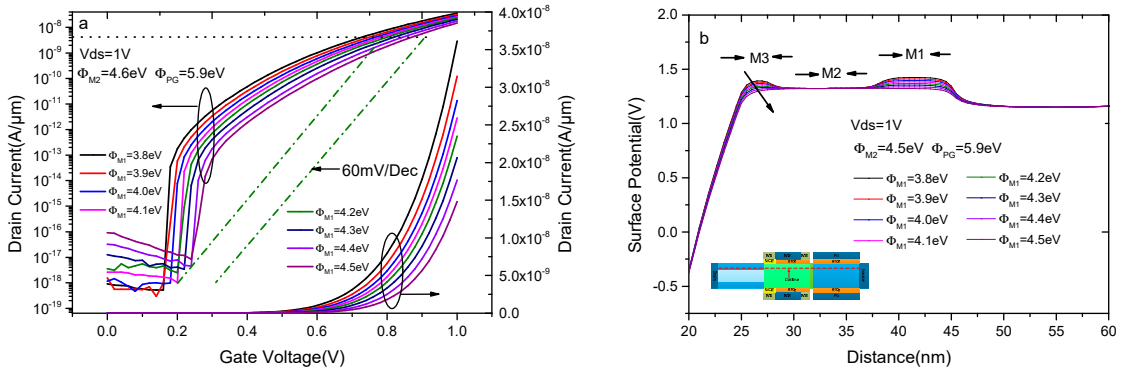

Figure 9. *Cont.*

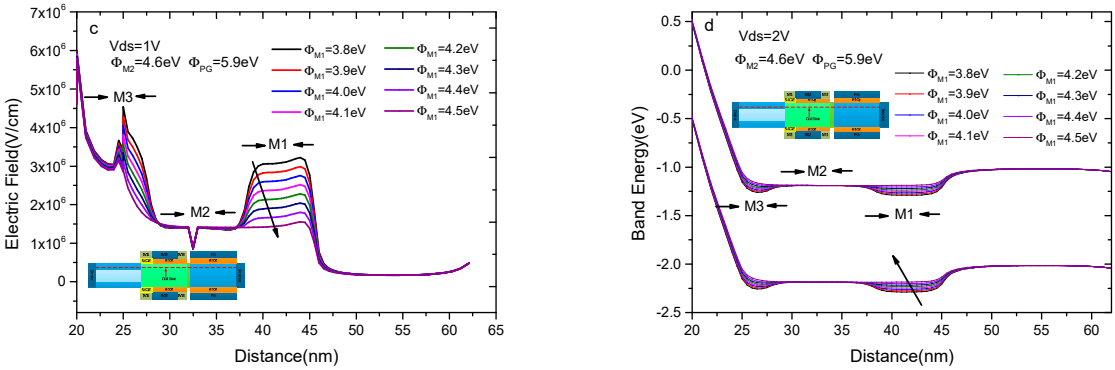

Figure 9. (**a**) Simulated log scale and linear scale transfer characteristics of DMMG-HJLTFET with different auxiliary gate work function (Φ_{M1}); (**b**) the potential distribution at the surface with different auxiliary gate work function (Φ_{M1}); (**c**) the distribution of electric field at the surface with different auxiliary gate work function (Φ_{M1}); (**d**) the variation of ON-state energy band with different auxiliary gate work function (Φ_{M1}).

Figure 10a shows the impact of the thickness of silicon (T_S) in a sandwich stack structure (GaAs/Si/GaAs) on transfer characteristics. It can be seen clearly from the Figure 10a, the ON-state current of DMMG-HJLTFET is minimal when T_S = 5 nm, this is because DMMG-HJLTFET is converted into HJLTFET when T_S = 5 nm, the current level of this condition is consistent with HJLTFET mentioned previous section. Meanwhile, the ON-state current of DMMG-HJLTFET increases visibly when T_S varies from 4 nm to 1 nm, the reason is that thickness of GaAs in sandwich stack structure (GaAs/Si/GaAs) increases from 0.5 nm to 3 nm when T_S decreases from 4 nm to 1 nm, which improves the electric field distribution at the surface of DMMG-HJLTFET, as shown in Figure 10b. It is not difficult to find that electric field of channel region increases and electric field of drain region decreases when T_S increases from 1 nm to 4 nm, which enhances the lateral electric field at drain/channel interface and improves the tunneling probability at source/channel interface. The reason for the improvement of the ON-state current and electric field distribution in Figure 10a,b is that GaAs is a direct bandgap semiconductor while Si is an indirect bandgap semiconductor, the bandgap width of GaAs is larger than that of Si, and the electron mobility of GaAs is much higher than that of Si.

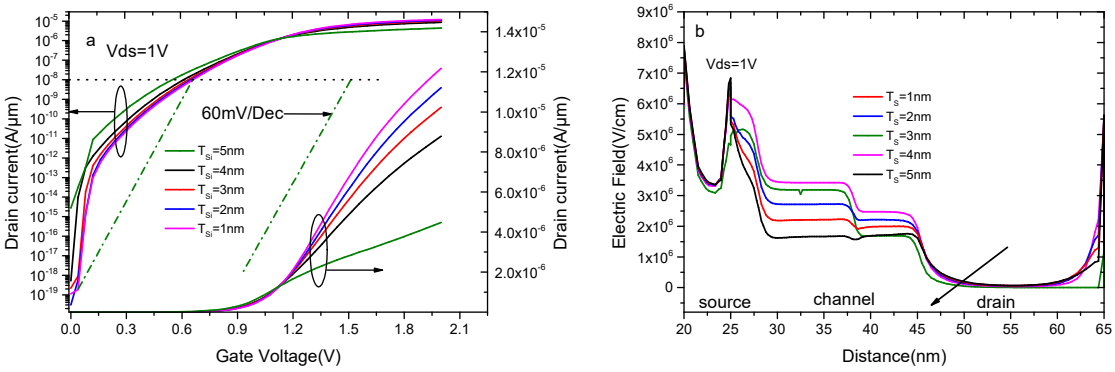

Figure 10. (**a**) Simulated log scale and linear scale transfer characteristics of DMMG-HJLTFET with different thickness of silicon (T_S) in sandwich stack structure (GaAs/Si/GaAs); (**b**) the distribution of electric field at the surface with different thickness of silicon (T_S) in sandwich stack structure (GaAs/Si/GaAs).

3.5. Performance Comparison in Terms of Analog/RF Figure of Merits

As we know, the frequency characteristics of the integrated circuits is profoundly affected by parasitic capacitances of devices, so it is very necessary to research the capacitance of DMMG-HJLTFET. Apparently, the characteristics of Cgg (gate capacitance), Cgs (capacitance of gate to source), and

Cgd (capacitance of gate to drain) are of great significance to evaluate the frequency characteristics and analog application ability of devices. Figure 11a–c show the capacitance of JLTFET, HJLTFET and DM-HJTFET versus Vgs under Vds = 1 V. In Figure 11a–c, the trend of the capacitance curve versus Vgs is similar, Cgs is very small in three devices due to the existence of polar gate which separates control gate electrode far from source electrode and, as a result, the coupling of control gate electrode and source electrode is relatively slight, so the curve of Cgg and Cgd is highly coincident, and Cgg is mainly determined by Cgd. Figure 11d shows the comparison of Cgg of JLTFET, HJLTFET and DMMG-HJLTFET, Cgg of JLTFET and HJLTFET remain at a small value when Vgs < Vds and increase rapidly with the increasing Vgs when Vgs > Vds, as shown in Figure 11d, while Cgg of DMMG-HJLTFET remains at a small value when Vgs < 0.5 Vds and increases rapidly with the increasing Vgs when Vgs > 0.5 Vds on account of divided gate electrode, moreover, Cgg of DMMG-HJLTFET is much less than that of JLTFET and HJLTFET due to the hetero dielectric adopted under the control gate.

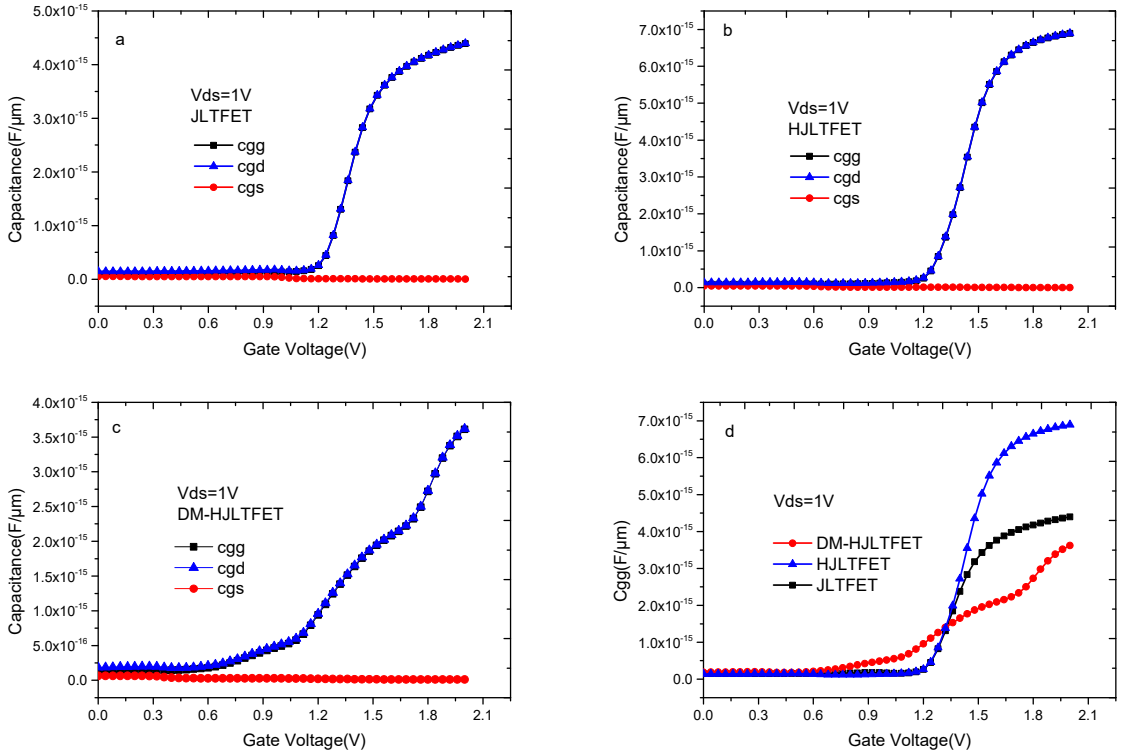

Figure 11. (**a**) Capacitance of JLTFET versus Vgs; (**b**) capacitance of HJLTFET versus Vgs; (**c**) capacitance of DMMG-HJLTFET versus Vgs; (**d**) comparison of Cgg (gate capacitance) of JLTFET, HJLTFET and DMMG-HJLTFET versus Vgs under Vds = 1.0 V.

Based on the above capacitance changes, we discuss the cut-off frequency(f_T) and gain bandwidth (GBW). Both of them are the important evaluation indicators for RF performance, and as shown in Equation (4), cut-off frequency(f_T) can be expressed as ratio of gm to Cgg [36]:

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1+2\frac{C_{gd}}{C_{gs}}}} \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} = \frac{g_m}{2\pi C_{gg}} \quad (4)$$

The GBW can be expressed as a ratio of g_m to C_{gd} for the DC gain value equal to 10, as shown in Equation (5) [37,38]:

$$GBW = \frac{g_m}{2\pi 10 C_{gd}} \quad (5)$$

Figure 12a,b shows the characteristic curves of the f_T and GBW of JLTFET, HJLTFET and DMMG-HJLTFET. Further, benefiting from large transconductance induced by structural innovation, the DMMG-HJLTFET could achieve a maximum f_T of 9.17 GHz at Vgs = 1.4 V, and a maximum GBW of 0.17 GHz at Vgs = 1.2 V, respectively. However, maximum f_T of JLTFET and HJLTFET are only 1.01 GHz at Vgs = 2.0 V and 3.74 GHz at Vgs = 1.6 V, and maximum GBW of JLTFET and HJLTFET are only 0.005 GHz and 0.09 GHz at Vgs = 1.1 V.

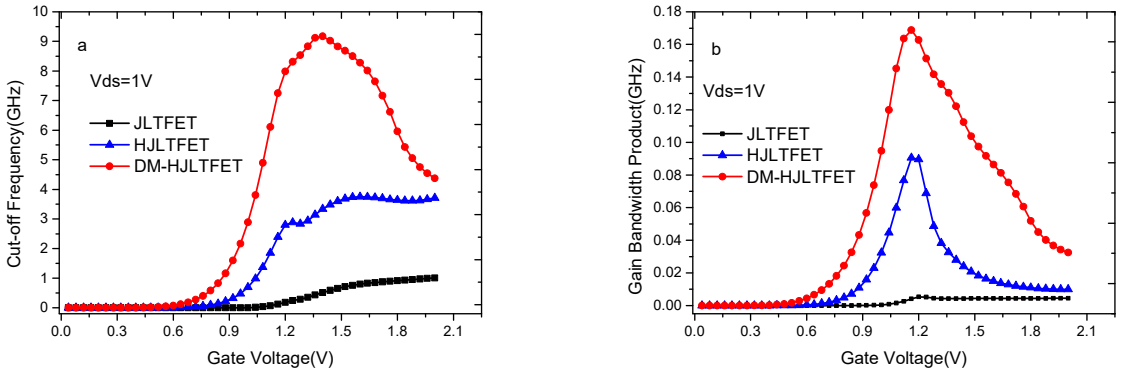

Figure 12. (**a**) The cut-off frequency(f_T) characteristic curves of JLTFET, HJLTFET and DMMG-HJLTFET; (**b**) the gain bandwidth (GBW) characteristic curves of JLTFET, HJLTFET and DMMG-HJLTFET.

4. Conclusions

In this paper, a dual material gate heterostructure junctionless TFET(DMMG-HJLTFET) is constructed and researched to improve the performance of JLTFET and HJLTFET. To enhance the on-state current and suppress the OFF-state current, Si/SiGe heterostructure at the source/channel interface and sandwich stack structure (GaAs/Si/GaAs) at drain region are introduced. Simultaneously, based on the gate engineered concept, the corresponding electrode is divided into three parts to further increase the tunneling barrier width at the drain/channel interface and the tunneling probabilities at source/channel interface. In our work, the effects of the device sizes, doping concentration and work function on the performance of the DMMG-HJLTFET are researched systematically to optimize the overall device performance. Simulation results indicate that DMMG-HJLTFET provides superior performance in terms of logic and analog/RF performance as compared with JLTFET and HJLTFET, the ON-state current of DMMG-HJLTFET increases up to 1.01×10^{-5} A/μm, and the maximum g_m of DMMG-HJLTFET is 1.26×10^{-5} S/μm at Vds = 1.0 V, meanwhile, DMMG-HJLTFET could achieve a maximum f_T of 9.17 GHz at Vgs = 1.4 V and a maximum GBW of 0.17 GHz at Vgs = 1.2 V, respectively. So, DMMG-HJLTFET may be one of the alternative devices for the next generation of low power applications.

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References

1. Choi, W.Y.; Park, B.-G.; Lee, J.D.; Liu, T.-J.K. Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. *IEEE Electron Device Lett.* **2007**, *28*, 743–745. [CrossRef]

2. Anghel, C.; Gupta, A.; Amara, A.; Vladimirescu, A. 30-nm Tunnel FET with Improved Performance and Reduced Ambipolar Current. *IEEE Trans. Electron Devices* **2011**, *58*, 1649–1654. [CrossRef]
3. Jang Hyun, K.; Sangwan, K.; Byung-Gook, P. Double-Gate TFET with Vertical Channel Sandwiched by Lightly Doped Si. *IEEE Trans. Electron Devices* **2019**, *66*, 1656–1661.
4. Mohd, R.U.S.; Sajad, A.L. Drain-Engineered TFET with Fully Suppressed Ambipolarity for High-Frequency Application. *IEEE Trans. Electron Devices* **2019**, *66*, 1628–1634.
5. Verhulst, A.S.; Vandenberghe, W.G.; Maex, K.; De Gendt, S.; Heyns, M.M.; Groeseneken, G. Complementary silicon-based heterostructure tunnel-FETs with high tunnel rates. *IEEE Electron Device Letter* **2008**, *29*, 1398–1401. [CrossRef]
6. Ahn, D.H.; Yoon, S.H.; Kato, K.; Fukui, T.; Takenaka, M.; Takagi, S. Effects of ZrO2/Al2O3 Gate-Stack on the Performance of Planar-Type InGaAs TFET. *IEEE Trans. Electron Devices* **2019**, *66*, 1862–1867. [CrossRef]
7. Avci, U.E.; Young, I.A. Heterojunction TFET scaling and resonant-TFET for steep subthreshold slope at sub-9nm gate-length. In Proceedings of the IEEE IEDM, Washington, DC, USA, 9–11 December 2013; pp. 4.3.1–4.3.4.
8. Zhaonian, Y. Tunnel Field-Effect Transistor with an L-Shaped Gate. *IEEE Trans. Electron Devices* **2016**, *37*, 839–842.
9. Kim, S.W.; Kim, J.H.; Liu, T.-J.K.; Choi, W.Y.; Park, B.G. Demonstration of L-Shaped Tunnel Field-Effect Transistors. *IEEE Trans. Electron Devices* **2016**, *63*, 1774–1778. [CrossRef]
10. Najam, F.; Yu, Y.S. Impact of Quantum Confinement on Band-to-Band Tunneling of Line-Tunneling Type L-Shaped Tunnel Field-Effect Transistor. *IEEE Trans. Electron Devices* **2019**, *66*, 2010–2016. [CrossRef]
11. Kim, J.H.; Kim, S.; Park, B.-G. Symmetric U-Shaped Gate Tunnel Field-Effect Transistor. *IEEE Trans. Electron Devices* **2017**, *64*, 1343–1349.
12. Wang, W.; Wang, P.F.; Zhang, C.M.; Lin, X.; Liu, X.Y.; Sun, Q.Q.; Zhou, P.; Zhang, D.W. Design of U-Shape Channel Tunnel FETs with SiGe Source Regions. *IEEE Trans. Electron Devices* **2014**, *61*, 193–197. [CrossRef]
13. Nam, H.; Cho, M.H.; Shin, C. Symmetric tunnel field-effect transistor (S-TFET). *Curr. Appl. Phys.* **2015**, *15*, 71–77. [CrossRef]
14. Lee, H.; Park, S.; Lee, Y.; Nam, H.; Shin, C. Random variation analysis and variation-aware design of symmetric tunnel field-effect transistor. *IEEE Trans. Electron Devices* **2015**, *62*, 1778–1783.
15. Jiang, Z.; Zhuang, Y.; Li, C.; Wang, P. Dual Sources U-shape Gate Tunnel FETs with High On-current and Steep SS. In Proceedings of the 2016 16th International Workshop on Junction Technology (IWJT), Shanghai, China, 9–10 May 2015; pp. 25–27.
16. Sola, W.; Sangsig, K. Covered Source–Channel Tunnel Field-Effect Transistors with Trench Gate Structures. *IEEE Trans. Nanotechnol.* **2018**, *18*, 114–118.
17. Li, W.; Liu, H.; Wang, S.; Chen, S.; Yang, Z. Design of High Performance Si/SiGe Heterojunction Tunneling FETs with a T-Shaped Gate. *Nanoscale Res. Lett.* **2017**, *12*, 198. [CrossRef] [PubMed]
18. Áron, S.; Steven, J.K.; Mathieu, L. Ab-Initio Simulation of van der Waals MoTe2–SnS2. Heterotunneling FETs for Low-Power Electronics. *IEEE Electron Device Lett.* **2015**, *36*, 514–516.
19. Cao, J.; Logoteta, D.; Özkaya, S.; Biel, B.; Cresti, A.; Pala, M.G.; Esseni, D. Operation and Design of van der Waals Tunnel Transistors: A 3-D Quantum Transport Study. *IEEE Trans. Electron Devices* **2016**, *63*, 4388–4394. [CrossRef]
20. Singh, D.; Pandey, S.; Nigam, K.; Sharma, D.; Yadav, D.S.; Kondekar, P. A Charge-Plasma-Based Dielectric-Modulated Junctionless TFET for Biosensor Label-Free Detection. *IEEE Trans. Electron Devices* **2018**, *64*, 271–278. [CrossRef]
21. Aslam, M.; Sharma, D.; Yadav, S.; Soni, D.; Sharma, N.; Gedam, A. A comparative investigation of low work-function metal implantation in the oxide region for improving electrostatic characteristics of charge plasma TFET. *Micro Nano Lett.* **2019**, *14*, 123–128. [CrossRef]
22. Haiwu, X.; Hongxia, L.; Shupeng, C.; Tao, H.; Shulong, W. Design and Investigation of a Dual Material Gate Arsenic Alloy Heterostructure Junctionless TFET with a Lightly Doped Source. *Appl. Sci.* **2019**, *9*, 4104.
23. Tao, H.; Hongxia, L.; Shupeng, C.; Shulong, W.; Wei, L. Design and Investigation of the High Performance Doping-Less TFET with Ge/Si0.6Ge0.4/Si Heterojunction. *Micromachines* **2019**, *10*, 424.
24. Aghandeh, H.; Ziabari, S.A.S. Gate engineered heterostructure junctionless TFET with Gaussian doping profile for ambipolar suppression and electrical performance improvement. *Superlattices Microstruct.* **2017**, *111*, 103–134. [CrossRef]

25. Rouzbeh, M.I.A.; Seyed, A.S.Z. Improved performance of nanoscale junctionless tunnel field-effect transistor based on gate engineering approach. *Appl. Phys. A Mater. Sci. Process.* **2016**, *122*, 988.
26. Rahimian, M.; Fathipour, M. Improvement of electrical performance in junctionless nanowire TFET using hetero-gate-dielectric. *Mater. Sci. Semicond. Process.* **2017**, *63*, 142–152. [CrossRef]
27. Anju; Tirkey, S.; Nigam, K.; Pandey, S.; Sharma, D.; Kondekar, P. Investigation of gate material engineering in junctionless TFET to overcome the trade-off between ambipolarity and RF/linearity metrics. *Superlattices Microstruct.* **2017**, *109*, 307–315. [CrossRef]
28. Basak, S.; Asthana, P.K.; Goswami, Y. Leakage current reduction in junctionless tunnel FET using a lightly. Doped source. *Appl. Phys.* **2015**, *118*, 1527–1533. [CrossRef]
29. Bal, P.; Akram, M.W.; Mondal, P.; Ghosh, B. Performance estimation of sub-30 nm junctionless tunnel FET (JLTFET). *J. Comput. Electron.* **2013**, *12*, 782–789. [CrossRef]
30. Lee, J.C.; Ahn, T.J.; Yu, Y.S. Si/Ge Hetero Tunnel Field-Effect Transistor with Junctionless Channel Based on Nanowire. *J. Nanosci. Nanotechnol.* **2019**, *19*, 6750–6754. [CrossRef]
31. Leung, G.; Chui, C.O. Variability impact of random dopant fluctuation on nanoscale junctionless FinFETs. *IEEE Electron Device Lett.* **2012**, *33*, 767–769. [CrossRef]
32. Wang, H.; Jiang, L.L.; Wang, N.; Yu, H.Y.; Lin, X.P. A Charge Storage Based Enhancement Mode AlGaN/GaN High Electron Mobility Transistor. *Mater. Sci. Forum* **2018**, *913*, 870–875. [CrossRef]
33. Pezzimenti, F. Modeling of the steady state and switching characteristics of a normally-off 4H-SiC trench bipolar-mode FET. *IEEE Trans. Electron Devices* **2013**, *60*, 1404–1411. [CrossRef]
34. Anvarifard, M.K.; Orouji, A.A. Proper Electrostatic Modulation of Electric Field in a Reliable Nano-SOI with a Developed Channel. *IEEE Trans. Electron Devices* **2018**, *65*, 1653–1657. [CrossRef]
35. Francesco, G.D.C.; Fortunato, P.; Salvatore, B.; Roberta, N. Numerical simulations of a 4H-SiC BMFET power transistor with normally-off characteristics. *Mater. Sci. Forum* **2011**, *679–680*, 621–624.
36. Sarkar, A.; Sarkar, C.K. RF and analogue performance investigation of DG tunnel FET. *Electron. Lett.* **2010**, *1*, 210–217. [CrossRef]
37. Seema, N.; Sudakar, S.C. Investigation of RF and linearity performance of electrode work-function engineered HDB vertical TFET. *Micro Nano Lett.* **2019**, *14*, 17–21.
38. Chen, S.; Liu, H.; Wang, S.; Li, W.; Wang, X.; Zhao, L. Analog/RF Performance of T-Shape Gate Dual-Source Tunnel Field-Effect Transistor. *Nanoscale Res. Lett.* **2018**, *13*, 321. [CrossRef]