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Broadband Simulation-Based EMC Modeling and EMI Assessment of a GaN-Based Phase-Shift Full-Bridge Converter for EV DC Powertrains

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Abstract

Nowadays, numerical simulation methods are advanced and widely used in industry, enabling the modeling of complex systems from printed circuit boards (PCBs) to full power converters. Among many isolated topologies, the phase-shift full-bridge (PSFB) topology is a well-established solution for isolated DC–DC conversion in electric vehicles. Therefore, this paper proposes a broadband electromagnetic compatibility (EMC) modeling methodology for a custom-designed 1 kW gallium nitride (GaN)-based PSFB converter intended for an electric vehicle (EV) DC powertrain. Moreover, the approach combines full-wave electromagnetic simulation with circuit-level simulation, including parasitic effects from PCB layout, power harnesses, and discrete components. Thus, the virtual prototype is assessed within a complete virtual test bench compliant with the standard Comité International Spécial des Perturbations Radioélectriques (CISPR) 25 over the 150 kHz–108 MHz range to capture common-mode (CM) and differential-mode (DM) conducted electromagnetic interference (EMI). Results show that the converter achieves efficiencies of 97.26% in standalone mode and 97.03% when integrated into the full DC powertrain. However, the conducted EMI assessment reveals that both CM and DM emissions exceed CISPR 25 Class 2 limits across the entire spectrum, with excess levels reaching up to 72 dBµV. Therefore, power harnesses significantly increase EMI levels at low frequencies due to the distributed inductance and stray capacitance. Finally, this study demonstrates the value of virtual prototyping for simulation-based EMI prediction in early-stage power converter design.

Keywords: broadband EMC modeling; EMI assessment; GaN-based phase-shift full-bridge converter; EV DC powertrains; virtual prototyping; conducted emissions; CISPR 25; common-mode; differential-mode

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1. Introduction

The increasing demand for commercial electric vehicles (EVs) has led to the introduction of new power ranges for automotive applications, enabling higher power capability and higher DC-link operating voltages (400 V to 800 V), with 400 V being the most prevalent EV battery architecture [1,2]. Several viable DC-DC converter topologies can be selected for EV powertrains. However, a small, reliable, parameterizable, lightweight, controllable, scalable, and efficient DC-DC converter is in high demand in the automotive industry [3–9]. In this context, energy efficiency has become one of the most important topics in power electronics. Wide-bandgap semiconductors, such as gallium nitride (GaN), can significantly

increase efficiency and enable smaller volumes in power-conversion systems, making them particularly attractive for EV applications [10]. The DC powertrain of an electric vehicle is the core system that transfers the high-voltage (HV) electrical energy stored in the HV battery to the low-voltage (LV) auxiliary power supply and loads.

This system function is usually ensured by an isolated HV phase-shift full-bridge (PSFB) DC-DC converter. The PSFB topology is commonly adopted for applications ranging up to 5 kW [11]. On the other hand, high-voltage systems in EVs, such as the DC powertrain, infotainment system, and other electronic components, create a complex environment where electromagnetic interference (EMI) can easily occur and affect other electronic systems in the vehicle or nearby [12–17]. Therefore, careful assessment of electromagnetic compatibility (EMC) is essential for the safe and reliable operation of EVs. Thus, to ensure EMC in automotive applications, international standards such as CISPR 12, CISPR 25, and CISPR 36 define limits and measurement methods for both radiated and conducted emissions [18,19]. Among these, CISPR 25 is the most relevant for onboard equipment, as it specifies the protection of onboard receivers against conducted disturbances in the frequency range of 150 kHz to 108 MHz [20]. As different markets have regulations that require different designs, it is necessary to cope with a large variety of similar converter variants. By using effective modeling and simulation strategies, the effort required to build these variants can be reduced, and costly redesigns can be avoided. In this context, EMC simulation has emerged as a powerful tool to predict EMI early in the design cycle, enabling the identification of failure mechanisms and the exploration of mitigation strategies before hardware prototyping [21]. Over the past decades, numerical simulation methods have matured significantly and are now widely embedded in industrial workflows [22]. These techniques enable modeling of complex structures ranging from PCBs and power modules to full power-conversion systems [17,23–35]. Previous works have addressed specific aspects of EMI modeling and mitigation for isolated DC–DC converters, including experimental validation of inductive component models [36], common mode noise cancellation through impedance balancing [37], and techniques to suppress noise caused by transformer parasitic capacitances [38,39]. These contributions have helped advance research in this field. The PSFB topology is widely recognized as a robust isolated DC-DC converter solution for electric vehicles. Thus, in this work, this topology is chosen as a design application and an EMC analysis subject.

A GaN-based PSFB converter delivering 1 kW of output power was custom-designed for this study. A full numerical model of the measurement setup, along with a model of the device under test (DUT), i.e., the PSFB converter, is developed to obtain reproducible and reliable simulation results. The modeled test setup replicates the CISPR 25 standardized EMC automotive testing rig used for EMI quantification, which stipulates a test frequency range from 150 kHz to 108 MHz [20]. A combined approach leveraging PathWave Advanced Design System (ADS) for circuit-level simulation and CST Studio Suite for full-wave three-dimensional (3D) electromagnetic modeling is adopted to perform a comprehensive EMI assessment of the PSFB converter within this virtual test setup.

The remainder of this article is organized as follows. Section 2 presents the electromagnetic (EM) modeling and characterization of the DC powertrain within the CISPR 25 test setup, including the description of EMI sources and propagation paths, the modeling of the HV battery and an HV line impedance stabilization network (LISN), the characterization of HV power harnesses, and the design and EM modeling of the PSFB converter. Section 3 presents and discusses the converter performance and conducted EMI noise analysis. Finally, Section 4 concludes the article and outlines perspectives for future work.

2. Electromagnetic Modeling and Characterization of the DC Powertrain Within the EMC Test Setup

The DC powertrain of an electric vehicle is the core system that transfers the HV electrical energy stored in the HV battery to the LV auxiliary power supply and loads. This function is typically ensured by an isolated HV PSFB DC-DC converter, which constitutes the main source of EMI within the system. As illustrated in Figures 1 and 2, the main functional units of the system include an HV battery, an HV LISN, the power harnesses of the conversion chain, a static load, and the PSFB power converter.

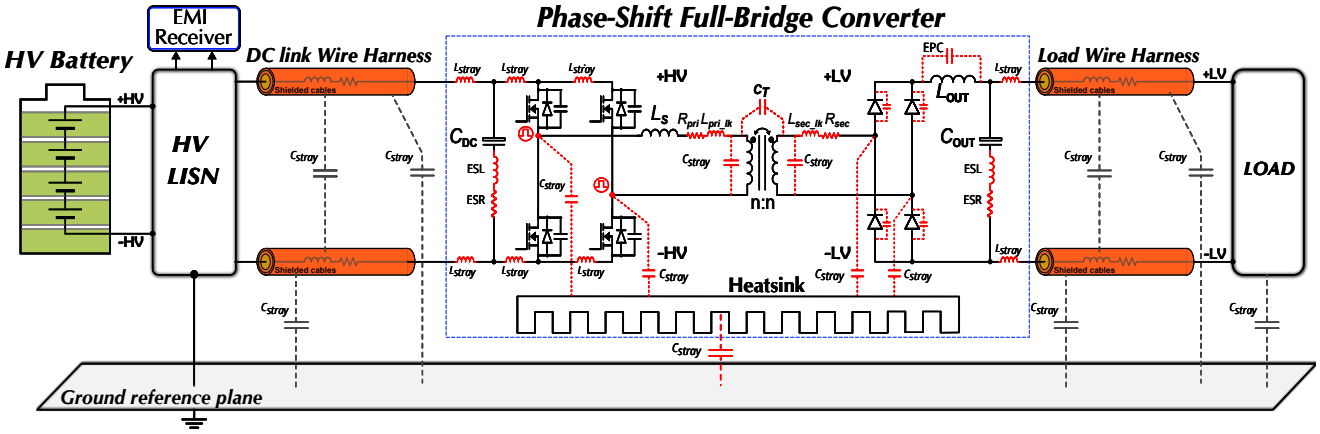
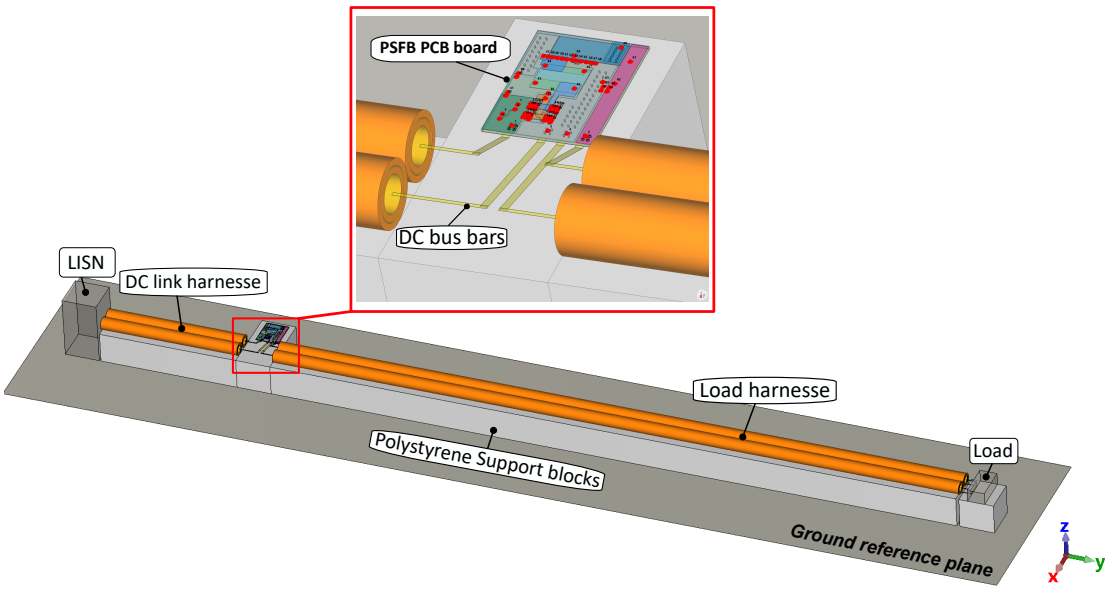


Figure 1. EMC—investigated power-conversion system.



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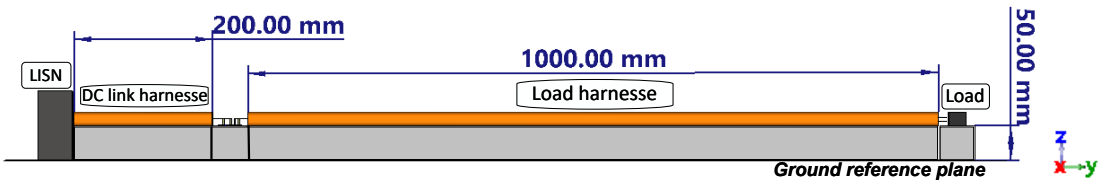


(**b**)

Figure 2. Full model of the DC powertrain within the CISPR 25 virtual test setup in CST Studio Suite. (**a**) 3D view of test setup. (**b**) Front view of the test setup.

The adopted modeling approach accounts for high-frequency effects along the common-mode (CM) and differential-mode (DM) noise propagation paths, which are predominantly governed by inductive and capacitive parasitic couplings (see Figure 1). Inductive couplings arise from stray interconnect inductances of the wiring harnesses, PCB tracks, stray elements of active and passive components (e.g., equivalent series inductance (ESL) of the DC-link capacitor), and the leakage inductances of the PSFB transformer. Capacitive couplings, on the other hand, occur between the conversion chain components, such as power cables, the PSFB heatsink, and the load and the reference ground. To enable reproducible and reliable simulation results, the fully modeled test setup in this work replicates the standardized CISPR 25 automotive EMC test rig for conducted EMI quantification (see Figure 2), which specifies a test frequency range spanning from 150 kHz to 108 MHz [20]. The breakdown of the modeling of this system's elements is given hereafter.

2.1. HV Battery and HV LISN Modeling

In this work, a high-frequency behavioral model of the HV Li-ion battery for automotive applications, developed in [40], is employed. It was developed for the construction of a battery emulator that mimics the real electrical behavior of an HV traction battery in test setups and was validated in the frequency range [30 kHz–200 MHz]. As illustrated in Figure 3, the battery simulation model comprises an ideal 400 V DC-voltage source and an impedance-emulating network used to characterize the HV traction battery. This model is adopted because it has proved extremely valuable for testing and designing filters, as well as analyzing the impact of power network impedance on conducted EMI levels. Additionally, as specified by CISPR 25 [20], an HV LISN is used to connect the HV battery to the input terminals of the DC powertrain.

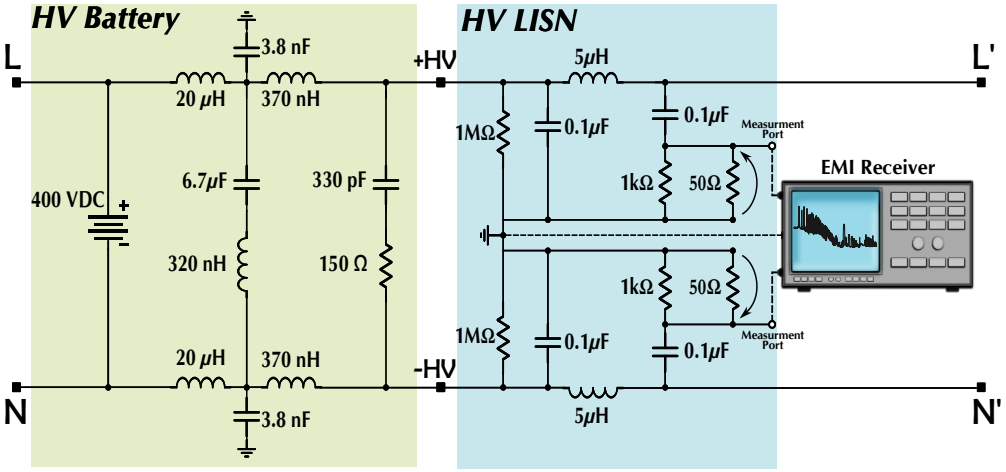


Figure 3. Model of the HV traction battery linked to the HV LISN cell according to CISPR25 [20].

2.2. Characterization of HV Power Harnesses

A trial-and-error approach in the design process of EMI filters can only be avoided if the impact of the network impedances within the HV power harness on conducted interferences is known. Thus, the proper assessment of the wiring harness is a crucial matter to address. According to the conducted EMI test rig arrangement specified by CISPR 25, the HV LISN is connected to the DUT (i.e., PSFB converter) through a 0.2-m HV shielded wiring harness, which is nearly one-fourteenth (i.e., $\lambda/14$) of the electrical wavelength at the test limit frequency of 108 MHz. The load, in this case, is connected to the PSFB converter through a 1-m-long shielded wiring harness (full wavelength). The structure of the shielded cables with their dimensions is represented in Figure 4.

This structure comprises a copper core (bare copper conductors), inner and outer cross-linked polyethylene insulation jackets (XLPE), and a shielding screen. The shielding of the power cables on the DC link and the load side is used to contribute to the reduction in both conducted and radiated emissions. The characterization of the shielded wiring harnesses' CM and DM impedances in open-circuit (OC) and short-circuit (SC) configurations is carried out to assess their high-frequency stray parameters. The shielded cables simulation in the CST Studio Suite is conducted according to their spatial disposition in the CISPR 25 measurement setup, as shown in Figure 5.

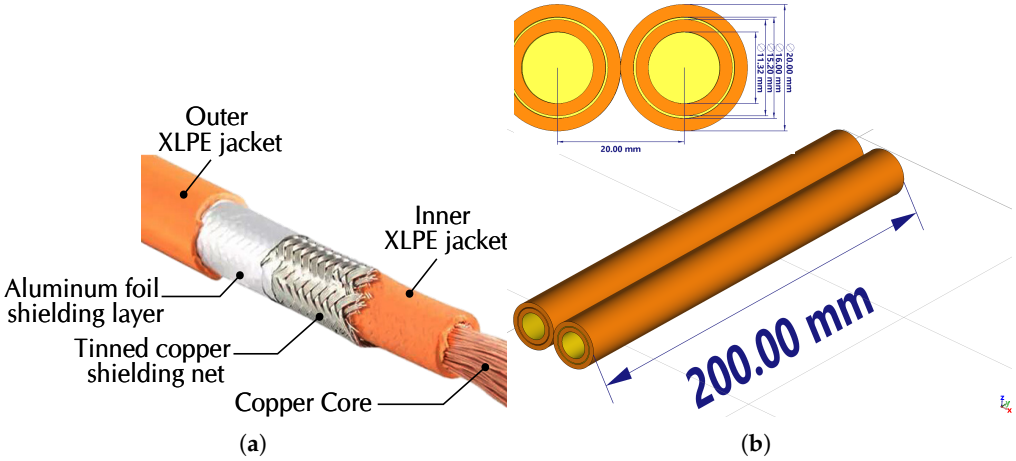


Figure 4. (**a**) Structure of an EV shielded cable. (**b**) Model of the DC link shielded wire harness in CST Studio Suite.

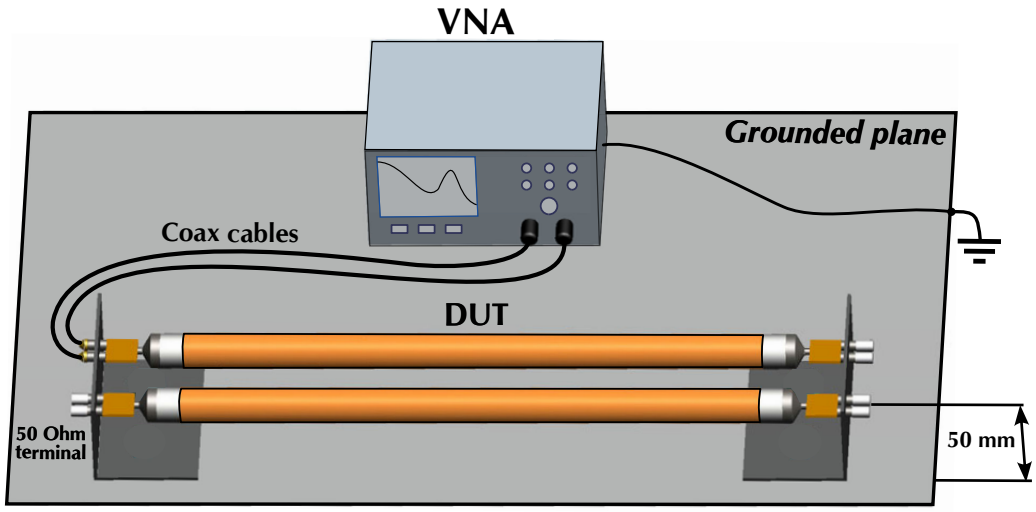


Figure 5. Measurement setup for the characterization of shielded cables of an EV.

In contrast to [41], each cable bundle is modeled and characterized as a single unit using a vector network analyzer (VNA) in the test frequency range of 150 kHz to 108 MHz. Postprocessing of the characterization results is performed afterward in the ADS software environment. The OC and SC tests' CM and DM impedances are depicted in Figure 6 for both the DC link wire harness (highlighted blue) and the load wire harness (highlighted red). These CM and DM impedances are much higher for the load's wire harness due to its physical length, which induces greater parasitic effects. The CM OC impedance curves of the DC link cables shown in Figure 6a exhibit an equivalent stray capacitance of 171 pF between the pair of cables to the shield in the low-frequency range (below 10 MHz), which yields an equivalent parasitic capacitance of 85.5 pF for a single cable to the shield.

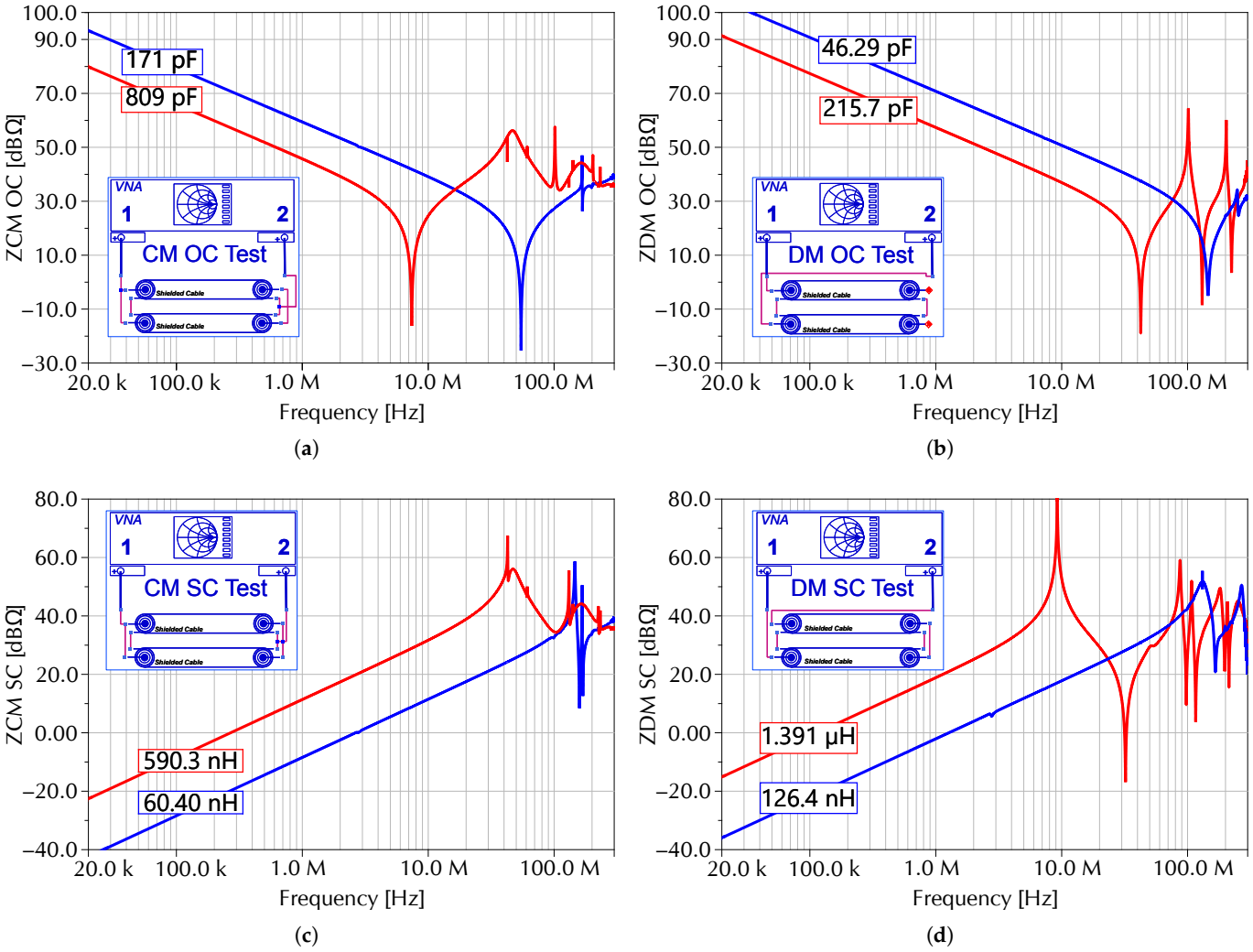


Figure 6. Impedance simulation results of the modeled DC link and load wiring harnesses. (**a**) CM OC impedances. (**b**) DM OC impedances. (**c**) CM SC impedances. (**d**) DM SC impedances.

The DM OC impedance curves displayed in Figure 6b demonstrate an equivalent stray capacitance of 46.29 pF in the low frequency range between the harness wires, which is equivalent to the series connection of two 85.5 pF capacitors. The same analysis applies to the load wire harness. The value of the latter's series parasitic inductance is halved when crossed by CM signals, as can be seen by comparing the impedance results of the DM SC test in Figure 6d to those of the CM SC test in Figure 6c. This inductance is higher by an order of magnitude compared to that of the DC link harness (more than ten times in the DM SC test).

A final evaluation is carried out to assess the overall worst-case capacitive coupling of the cable bundles to the ground. The power harnesses are characterized separately in open-circuit mode, with their shields grounded and the VNA connected each time to one terminal. The resulting impedances, along with their total distributed stray capacitances, are depicted in Figure 7. The DC link cables exhibit the same capacitive impedance because they are identical and at the same height above the plane ground. This also applies to the load cables. In comparison to the DC link cables, the load cables exhibit a higher capacitive coupling to ground (405.1 pF per cable) with markedly pronounced self-resonances due to their lengthy structure.

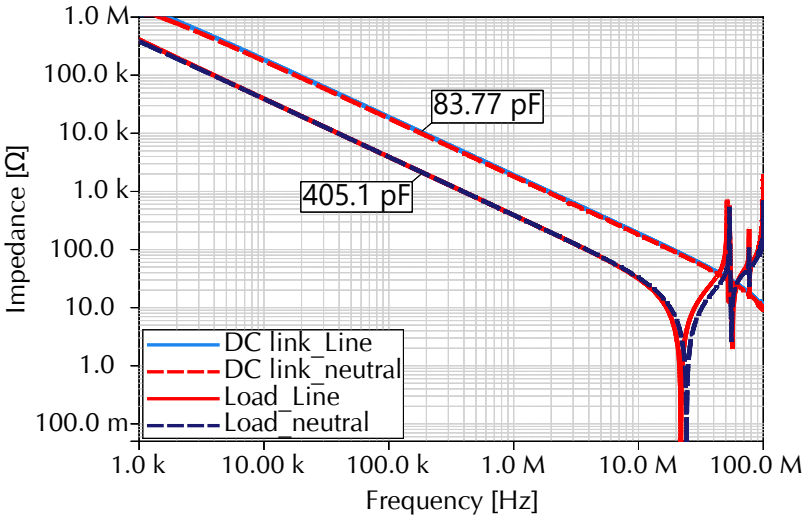


Figure 7. Input and output power harnesses coupling to the ground.

These results showcase the contribution of the wire harnesses to the parasitic paths of the noise signals and provide insight into their impact on the system impedance and induced EMI levels.

2.3. Modeling of the PSFB DC-DC Converter

The PSFB power converter is designed and modeled to step down an input DC voltage of 400 V delivered by the HV battery of an EV into an output voltage of 48 V DC with high isolation and efficiency above 95% under full load conditions. The characteristics of the designed converter are listed in Table 1.

Table 1. Specifications of the designed PSFB DC-DC power converter.

DC link input voltage (Vin)	400 V
Max Output Voltage (Vout)	48 V
Max Output Power @ Full Load	1 kW
Max DC Output current @ Full load	≈20.83 A
Switching frequency (f_{sw})	100 kHz
Control Technique	Peak Current Mode Control

A full electromagnetic (EM) model of the PSFB converter is designed and implemented based on the specifications laid out in Table 1 to study its power-conversion performance and EMI signature. Figure 8 shows the circuit diagram of the actual designed power converter. The majority of discrete power components are provided by their respective manufacturers and vendors, when available, and implemented in simulations, either as high-fidelity Simulation Program with Integrated Circuit Emphasis (SPICE) models for active components or as measured Touchstone files for passive components. All critical components were modeled with their parasitic behavior (ESR, ESL, saturation, stray capacitance, etc.), not as ideal L/C.

The converter PCB module was primarily designed in ADS software as an initial step to be then later exported into CST Studio Suite to be characterized within the CISPR 25 virtual test setup for conducted EMI as shown in Figure 2, following the same broadband modeling and simulation strategy for conducted emissions reported in [28]. A first draft of the PCB layout was initially designed on a four-layer board, including the power nets

and the integrated circuit (IC) stage with its feeding network. To ensure a high degree of freedom, the PCB track patterns were smoothed and rounded, as seen in Figure 9.

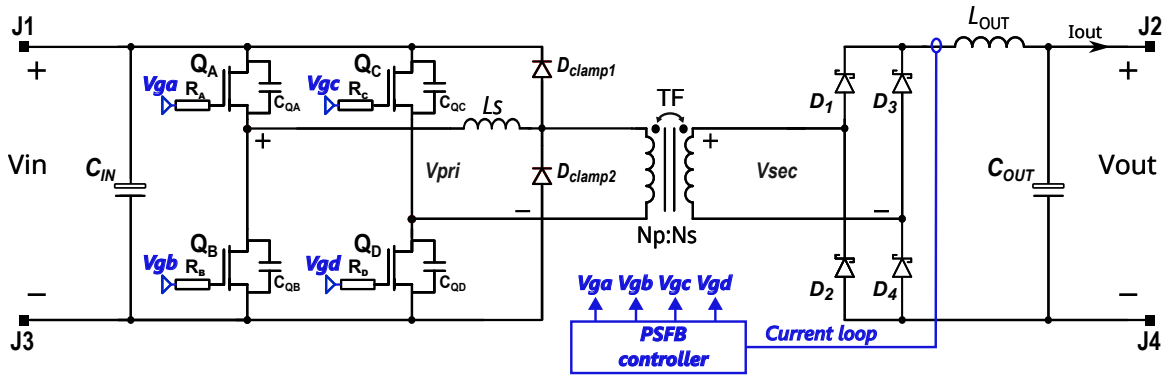


Figure 8. Schematic of the designed PSFB converter with a primary clamp.

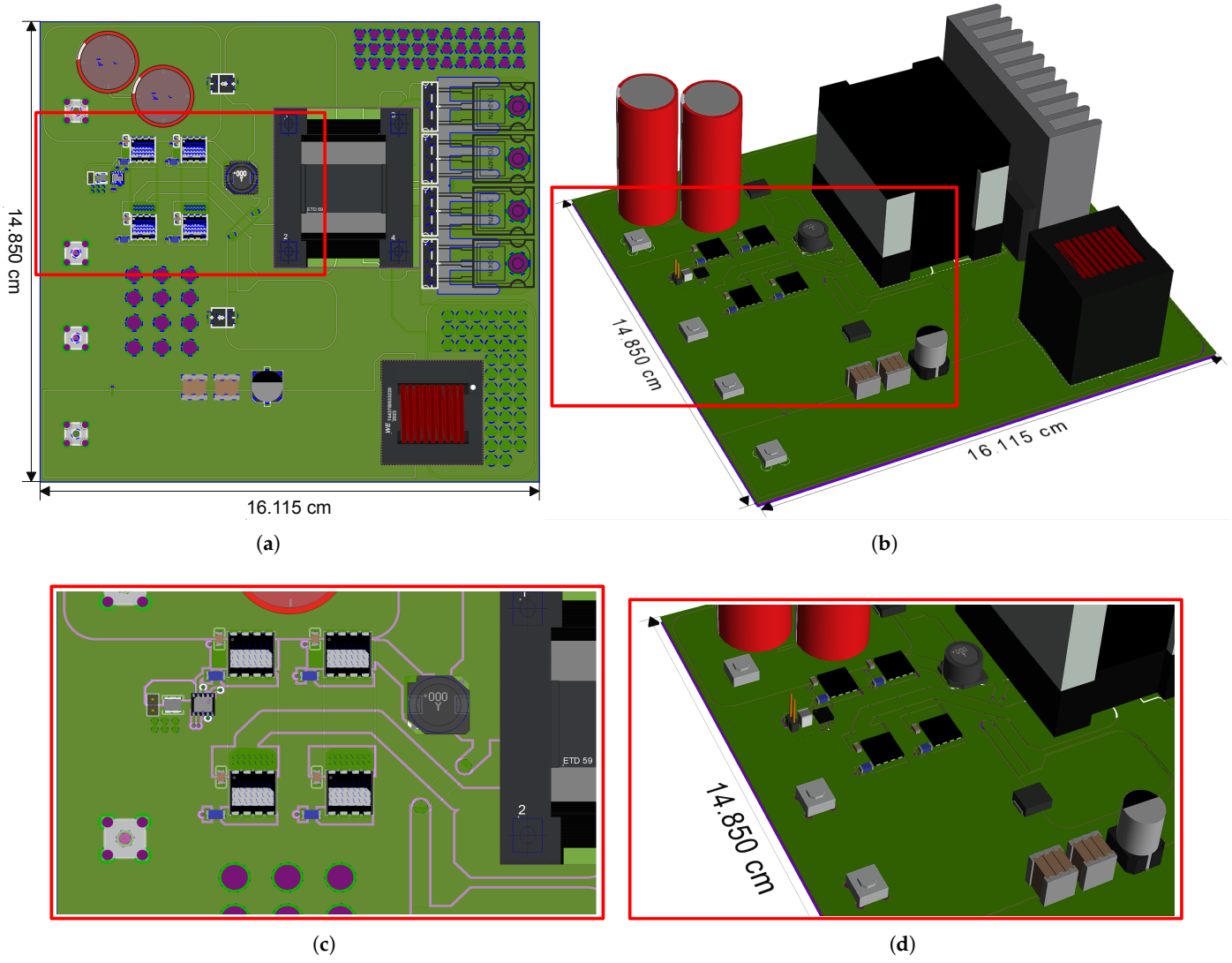


Figure 9. PSFB converter initial PCB board prototype. (**a**) Top view. (**b**) 3D view. (**c**) Top 2D zoom at the power FETs and IC stage (upper packages denuded). (**d**) 3D zoom at the power FETs and IC stage.

Nonetheless, when exporting a complex multilayer structure to CST, lumped ports cannot be reliably assigned to internal nodes in the presence of inner power or ground

planes. After numerous design iterations, the control stage portion was excluded from the 3D EM model and, instead, set as an external circuit command block in ADS.

This was done to avoid simulation errors and to ensure a correct interface between the EM-extracted S-parameter model and the external IC controller stage. Consequently, the PCB layout was redesigned as a two-layer board, as shown in Figure 10. This simplified board retained the same dimensions, layout, routing, number of components, and their disposition, but utilized simplified tracks with polygon and square shapes to alleviate the meshing process of the power module, reducing computational effort and memory consumption. The power module's PCB was modeled on a two-layer board with a copper thickness of 5.8 mil and a 28 mil thick FR4 substrate.

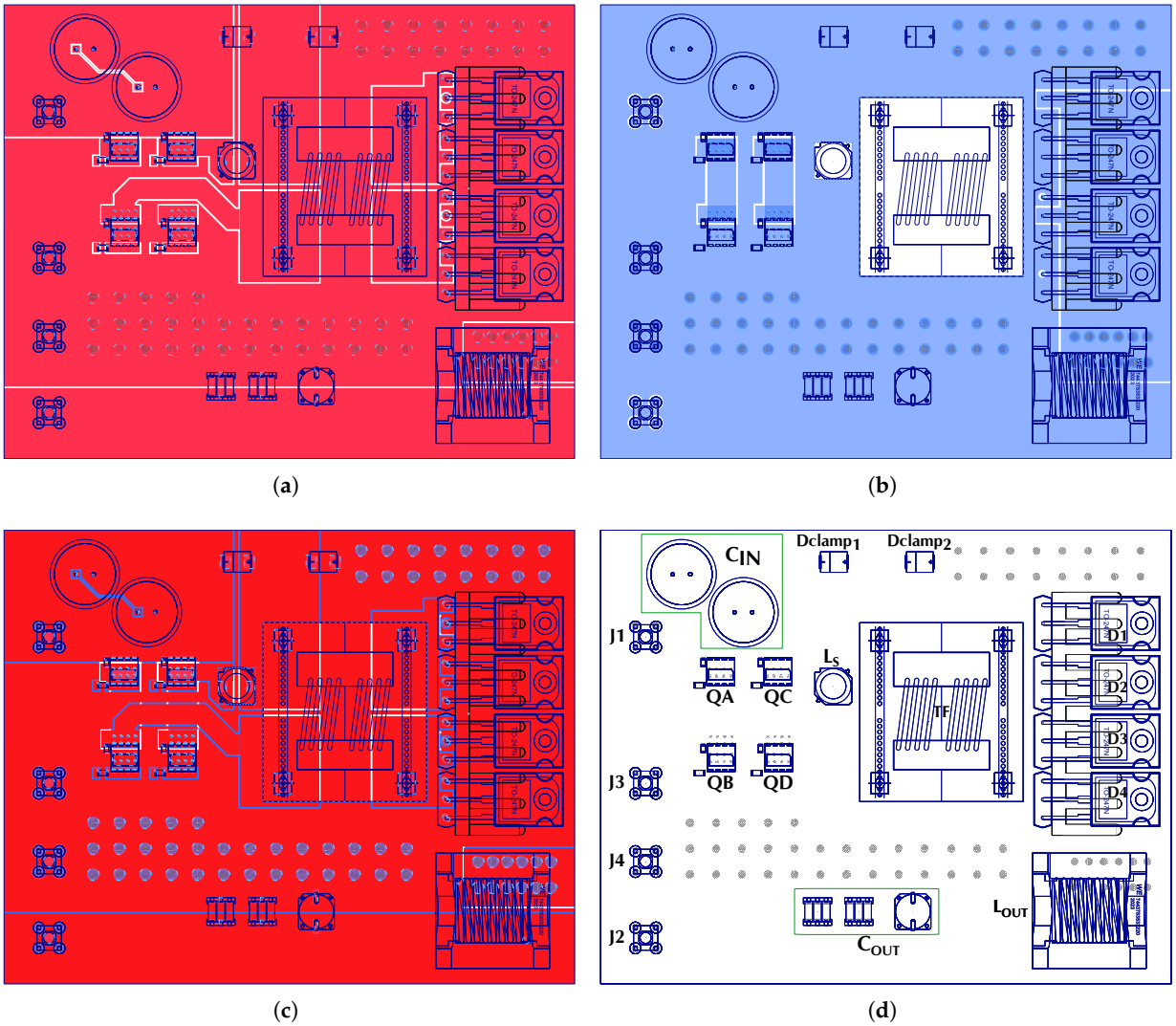


Figure 10. PCB board layout of the PSFB power converter. (**a**) Top layer. (**b**) Bottom layer. (**c**) Top and bottom layers. (**d**) Outlines and labels of the main components.

This simplification removes internal planes and allows clean port definition on top and bottom layers, reducing the port count from 87 to 77 due to the removal of the IC control stage, while preserving the dominant parasitic effects of the power stage. To quantify the impact of this modification, the S-parameters of the four-layer and two-layer PCB board models were compared over a broadband range covering the frequency band of interest. Instead of comparing all ports randomly and discriminately, the main power nets that carry the critical switching currents were selected, as highlighted in Figure 11.

These include the input power rail via its reflection coefficient S_{11} (Figure 11a), the output power rail via transmission coefficient S_{29} (Figure 11b), and the nets connecting the leading and lagging legs to the power transformer via transmission coefficients S_{34} and S_{56}, as shown in Figure 11c and Figure 11d, respectively. The characterization results depicted in Figure 12 show very good agreement between the four-layer and two-layer models.

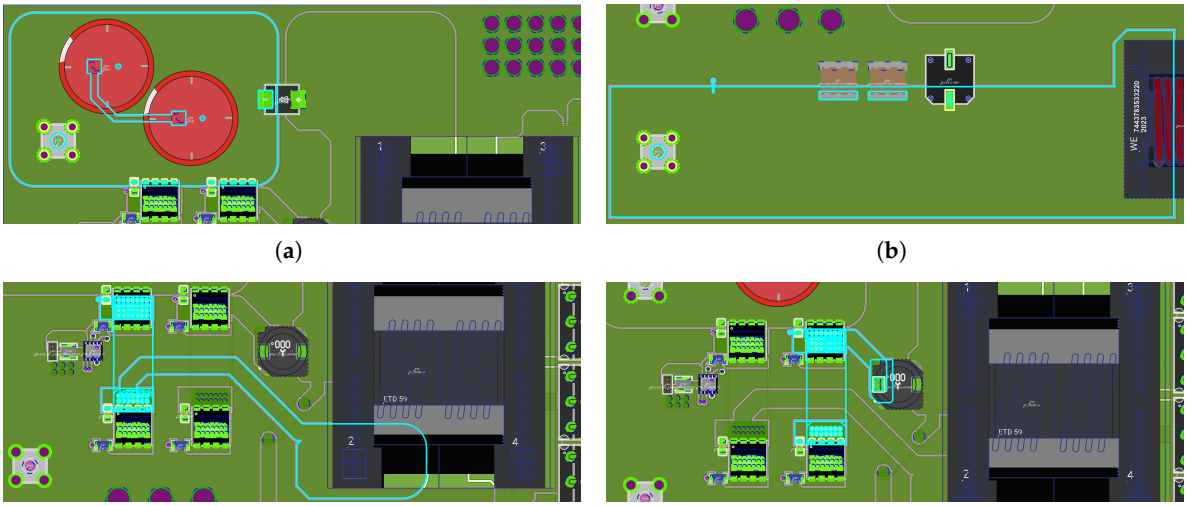


Figure 11. Characterized power nets in the original four-layer PCB and the simplified two-layer geometry. (**a**) Input power rail net. (**b**) Output power rail net. (**c**) Leading leg to transformer connection net. (**d**) Lagging leg to transformer connection net.

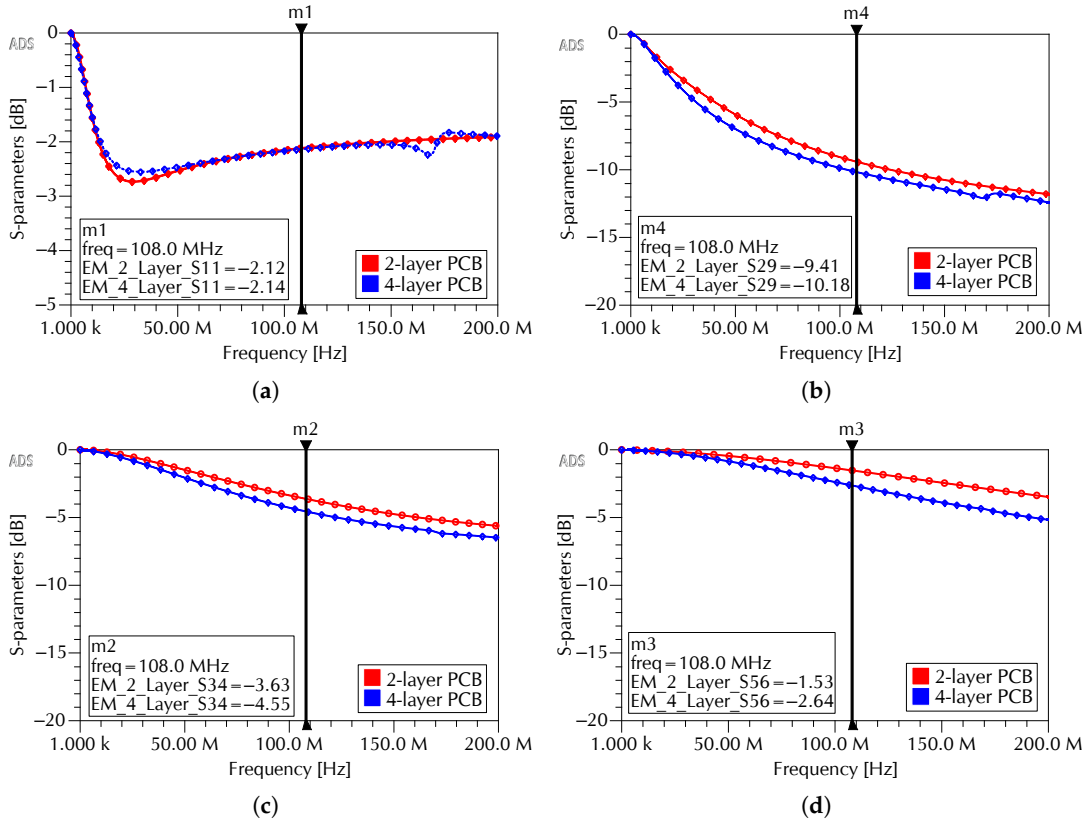


Figure 12. S-parameters comparison between the four-layer and two-layer PCB models for the selected power nets. (**a**) Input power rail (S_{11}). (**b**) Output power rail (S_{29}). (**c**) Leading leg to transformer (S_{34}). (**d**) Lagging leg to transformer (S_{56}).

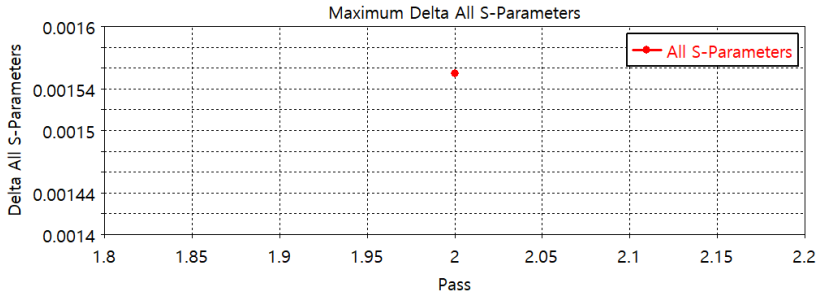
As shown in Figure 12, the differences observed at 108 MHz are: 0.02 dB for S_{11}, 0.77 dB for S_{29}, 0.92 dB for S_{34}, and 1.11 dB for S_{56}. All deviations are below 1.2 dB, and most are well under 1 dB. This demonstrates that the main electromagnetic effects, including current return paths, parasitic couplings, characteristic impedances, and high-frequency signatures, are faithfully preserved in the two-layer model. Thus, the two-layer simplified geometry does not compromise the essence of the electromagnetic behavior and, therefore, the accuracy of the conducted EMI predictions. Furthermore, such simplifications enabled the smallest possible time steps ($T_{\text{step_max}} < 1$ ns) to achieve very dense transient EM simulations with high precision, allowing for the capture of all fast transient EMI phenomena of the power-conversion system with full resolution in time and frequency, in conjunction with the fastest possible rate of reproducibility.

A cleanly designed PCB layout with minimal stray elements and parasitic coupling effects is crucial for achieving an optimized performance power converter with a low EMI signature and favorable thermal profile. Therefore, a set of basic techniques for EMI reduction was adopted within the designed power module. To begin with, the routing of the PCB was made with wide tracks to reduce their resistive and inductive elements, which in turn reduces voltage spikes, copper losses, and enhances efficiency. At the same time, the PCB was designed with a large copper pour ground plane connected to the top layer by an array of stitching vias to decrease the adverse capacitive coupling effect of wide tracks. To further diminish this effect, copper keepouts were established at the bottom layer within the copper pour underneath the shunt inductor L_s and the power transformer to reduce the parasitic capacitances between their top layer terminals and the ground net. This overwhelming ground net allows for a short connection between the clamping diodes and the hot point on the primary side of the transformer. The leading leg (QA, QD) and lagging leg (QB, QC) were disposed close to each other to minimize the length of the switching loop, with their GaN power FETs connected from the top to the bottom layer using via arrays. Finally, the diodes on the bridge rectifier were connected next to each other for a compact and adequate connection of their base plate (case) to the heat sink mounted directly on the top-ground net. This overwhelming ground net allows for a short connection between the clamping diodes and the hot point on the primary side of the transformer.

The PCB board was exported into the CST Studio environment for evaluation within the CISPR 25 virtual test setup for conducted EMI, following the same broadband modeling and simulation strategy for conducted emissions reported in [28]. In this setup, the wiring harnesses are included to fully characterize the behavior of the investigated PSFB converter. The 3D model of the PCB board imported in ODB++ file format is characterized in CST Studio both without and with the inclusion of the input and output power harnesses. After the elements in the structure were redefined with their respective materials, discrete ports were assigned, and the problem boundaries were defined.

Full 3D numerical simulations were then conducted in the frequency domain with a tetrahedral mesh using the built-in Finite Element Method (FEM) solver in CST Studio. For this type of electromagnetic problem, a proper frequency range must be selected. Therefore, given that the EMC test analysis covers the range of 150 kHz to 108 MHz, an interpolating sweep from DC to 600 MHz was defined for analysis, providing sufficient margin with respect to the test range, while the solution frequency for which the mesh is calculated (solution frequency) was set to 1 GHz. The 3D simulation uses a direct equation system solver with second-order tetrahedral elements. To ensure deep numerical precision before exporting the multi-port Touchstone model, the linear solver accuracy threshold was tightened from the default 10^{-3} to 10^{-6}, and the low-frequency stabilization feature was enabled to manage the wide bandwidth.

The relative residual norm of the algebraic solver was monitored across the frequency sweep and successfully reached the target threshold, guaranteeing a mathematically stable solution. Spatial discretization independence was verified using CST's automated adaptive mesh refinement loop. The broadband convergence criterion was set to a maximum scattering matrix variation threshold of $\Delta S = 0.04$ (4%) between successive mesh passes. As shown in the convergence metrics (Figure 13a), the adaptive meshing process converged, with the maximum S-parameter deviation dropping well below the 0.04 target threshold by the final pass. Additionally, the broadband interpolation error estimate remained minimal (Figure 13b). This confirms that the mesh density is sufficient to accurately capture the electromagnetic behavior of the test setup and that further mesh refinement does not alter the outcome. The resulting multi-port S-parameter model of the 3D simulation was generated in a Touchstone (.SnP) file format with 77 lumped ports that enable the interface connection between the output 3D FEM model and the SPICE simulation platform, in this case, the PathWave ADS environment.



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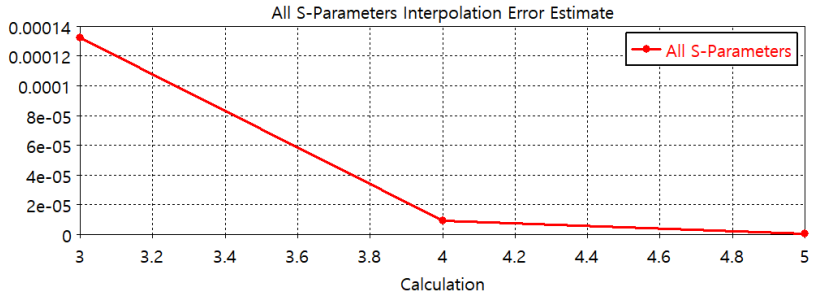
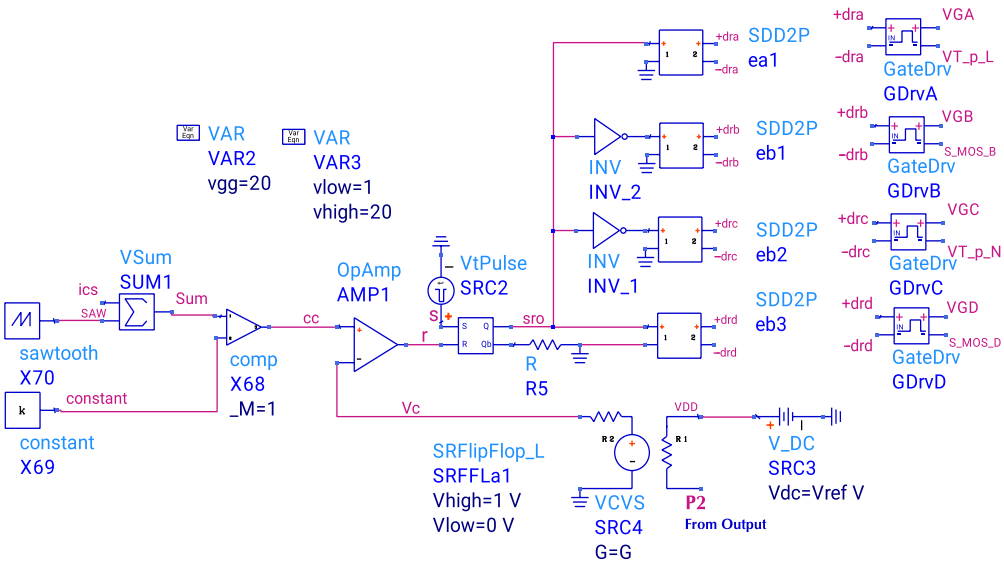


(**b**)

Figure 13. Convergence and interpolation error of the 3D EM model. (**a**) Maximum Delta of all S-parameters as a function of the adaptive mesh pass. (**b**) All S-parameters interpolation error estimate across the frequency sweep.

The multi-port model is intended to represent with high accuracy the electromagnetic behavior of the test setup, including the PSFB converter's PCB board and power cables, through the defined ports within the specified frequency range. After this S-parameter model was validated, it was exported to the ADS software environment, where each active and passive component (including the GaN FETs, clamping diodes, transformer, and output rectifier) is connected to its respective port, along with the HV battery, HV LISN circuit blocks, and the static load emulator according to the CISPR 25 conducted emission test configuration.

For example, Figure 14 shows the IC controller built in ADS. Figure 14a presents the complete controller schematic, while Figure 14b zooms in on the connections to the GaN FET pins. The controller is not included in the CST 3D EM model; it is linked in ADS to the ports of the power module. The co-simulation blocks are utilized to perform transient simulations, and EMI characterization of the DC powertrain is shown in Figure 15.



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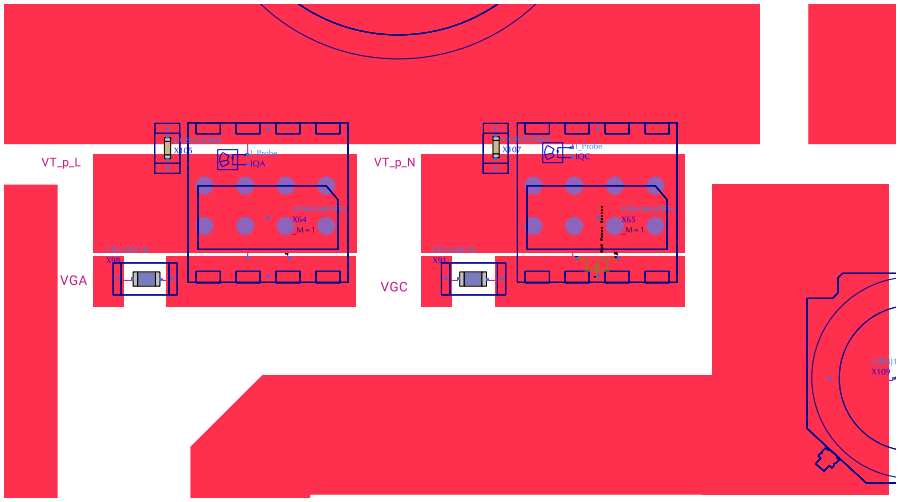


(**b**)

Figure 14. (**a**) IC Controller schematic in ADS. (**b**) Zomm at the connection of the IC stage to the GaN FETs pins.

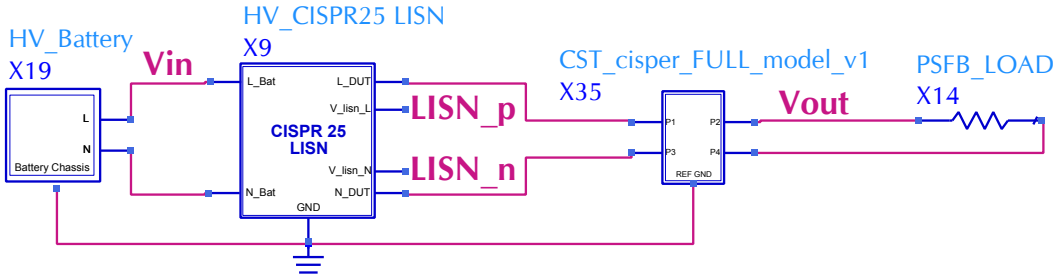


Figure 15. Top-level co-simulation schematic of the DC powertrain within CISPR 25 test setup.

This co-simulation setup enables time-domain transient analysis over several switching cycles to capture both steady-state behavior and switching-induced transients. The voltage and current waveforms at the LISN measurement ports are subsequently processed via Fast Fourier Transform (FFT) to quantify the conducted EMI spectra through direct comparison with CISPR 25's Class 2 limits.

3. Power-Conversion Performance and Conducted EMI Analysis

The results summary and analysis of the PSFB power converter performances before and after its inclusion in the DC powertrain (with the LISN connected in all cases and the clamping diodes either activated or deactivated) are discussed below.

3.1. Noise Source Impedance Analysis

To evaluate the noise source impedance characteristics of the PSFB converter and the harness's contribution to the dominant peaks in the induced EMI levels. The CM and DM impedances of the PSFB converter are extracted, both before and after the inclusion of the power harnesses. This analysis follows the modeling methodology described in [42], which is projected onto the PSFB topology based on the modeling work developed in [43]. The DM noise impedance is extracted between the input and output terminals of the converter board, and then between the input and output terminals of its power harnesses, without including the ground. The CM noise impedance is extracted between the converter input terminals and the ground reference plane. After adding the power harnesses, it is evaluated between the harness input and output terminals and the ground reference plane. These extractions were performed directly from the full co-simulation model of the CISPR 25 setup. Figure 16 shows the equivalent high-frequency model of the PSFB converter, while the corresponding stray parameter values extracted from the designed PSFB EM model and its power components are listed in Table 2. Figure 17 shows the equivalent differential-mode and common-mode noise source models of the PSFB converter in standalone mode, together with their respective impedances.

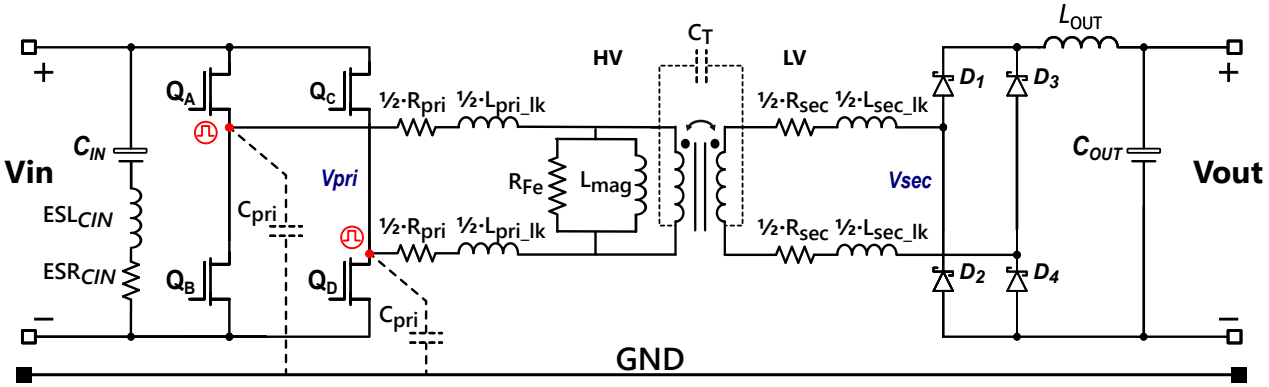


Figure 16. Equivalent noise model of a PSFB converter as introduced in [42].

Table 2. Parameter values of the equivalent model of the PSFB.

Parameter	Values
R_{pri}	29.23 mΩ
L_{pri_lk}	12.21 µH
R_{sec}	1.44 mΩ
L_{sec_lk}	0.179 µH
C_{pri}	252.8 pF
C_T	60.42 pF
C_{IN}	2 × 560 µF
$ESL_{C_{IN}}$	2 × 9.81 nH
$ESR_{C_{IN}}$	2 × 63 mΩ

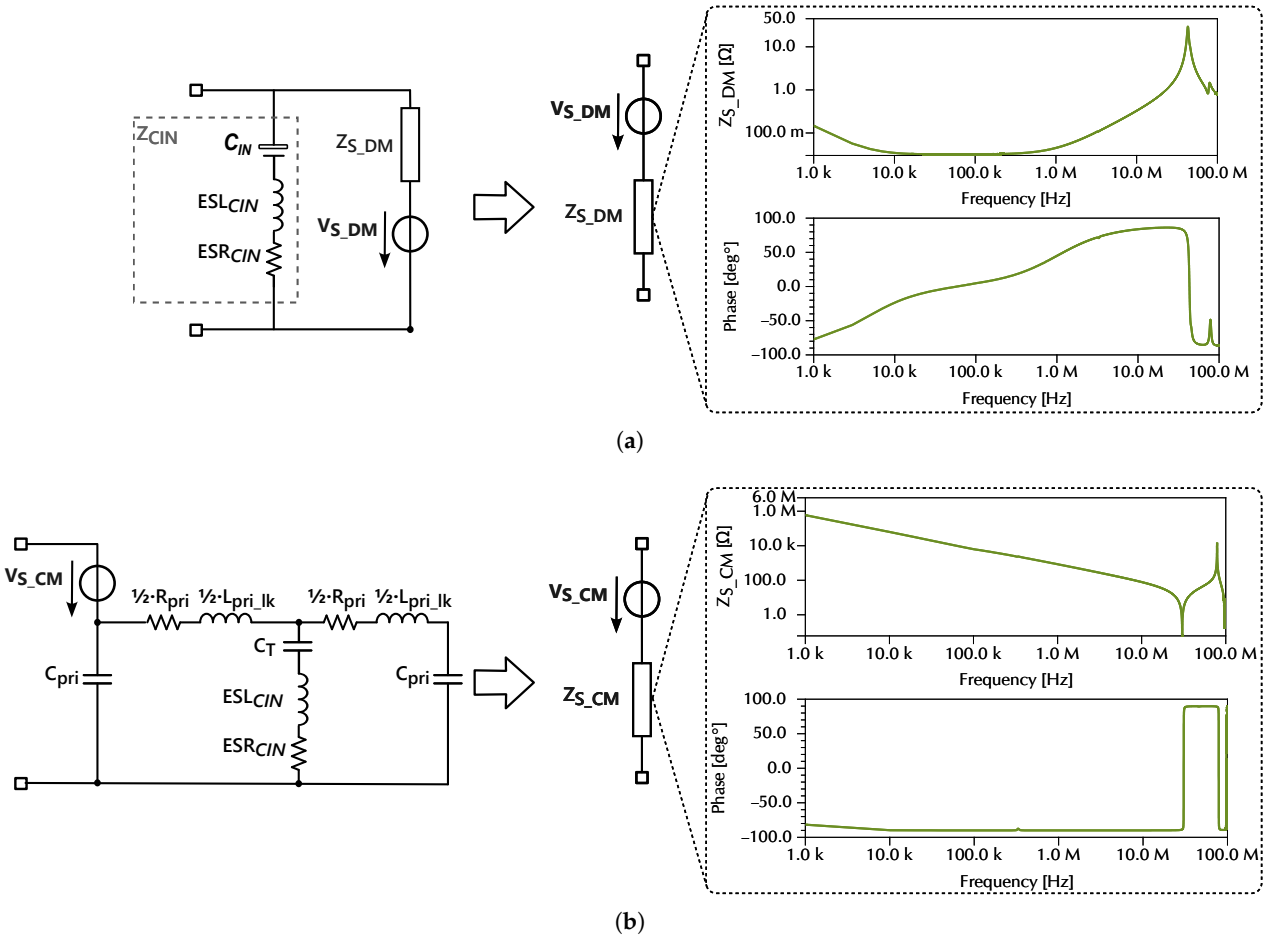


Figure 17. PSFB converter noise source impedances. (**a**) DM impedance. (**b**) CM impedance.

When analyzing the PSFB converter alone, the DM noise source impedance Z_{S_DM} is primarily determined by the DC-link capacitor as shown in Figure 17a. Thus, Z_{S_DM} is modeled in parallel with the DC-link capacitor impedance $Z_{C_{IN}}$ using Thévenin's theorem. Over the frequency range of interest, the impedance of the DC-link capacitor is very low; therefore, the contribution of the converter's internal DM impedance is neglected. Consequently, Z_{S_DM} is effectively defined by the DC-link capacitor together with its parasitic elements (ESR and ESL).

The CM noise, generated by high-frequency pulsations of the power devices (GaN FETs) at the primary-side switching nodes, flows to ground through the parasitic capacitances (C_{pri}) and through the transformer's inter-winding capacitance (C_T). The CM noise source impedance Z_{S_CM} is therefore derived from the equivalent converter model (Figure 16) by reducing the circuit to the equivalent shown in Figure 17b, assuming that a conducting diode is always present on the PSFB secondary side. The CM impedance Z_{S_CM} shown in Figure 17b can then be calculated using the parameter values listed in Table 2.

The DM and CM noise source impedances of the PSFB converter alone, and then within the DC powertrain (including power harnesses, HV battery, test setup, etc.), are depicted in Figure 18. The DM impedance is dominated by the DC-link capacitor (C_{IN}) impedance at low frequencies (below 1 MHz). However, beyond 19 kHz, the PSFB converter exhibits an increase in DM impedance due to the stray inductive effect of the cables.

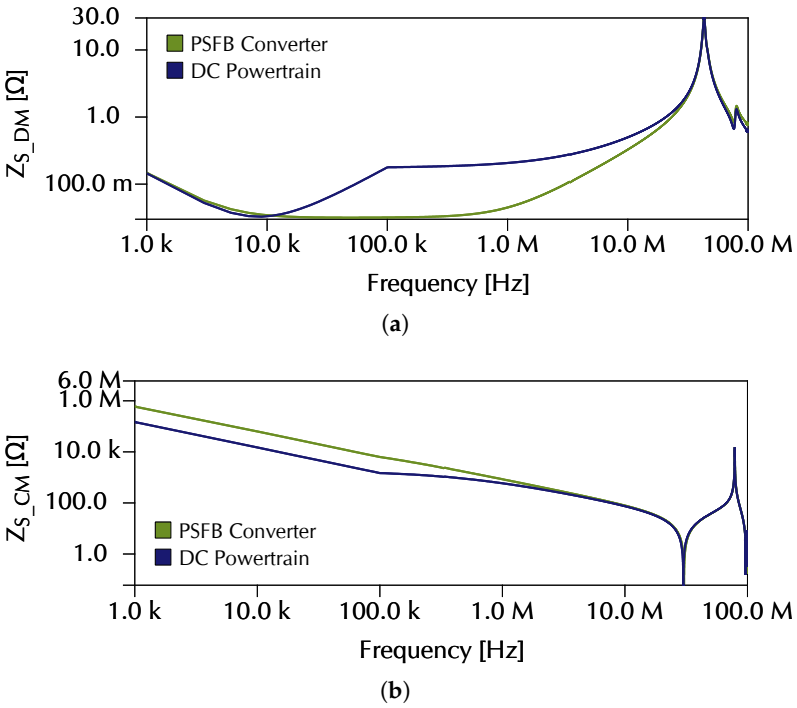


Figure 18. PSFB converter noise source impedances before and after inclusion of power harnesses. (**a**) DM impedance. (**b**) CM impedance.

The CM noise impedance, on the other hand, drops to a lower level between 1 kHz and 1 MHz after the addition of the power harnesses, which accentuates the parasitic coupling to ground and raises the CM noise levels.

3.2. Effect of Harnesses and Clamping Diodes on Power-Conversion Efficiency and Noise Levels

The switching waveforms of the designed PSFB power module operating at full load, directly connected without the inclusion of the HV battery and power harnesses, are presented in Figure 19. The converter achieves an efficiency of 97.26% under full load conditions. In this case, the clamping diodes D_{CLAMP1} and D_{CLAMP2} are deactivated (off-state). The last two cycles of the output voltage and current show clean waveforms with an output power slightly below the nominal values due to the power losses introduced by the PCB board and its discrete power components. In terms of noise ripple, the converter yields a peak-to-peak voltage ripple of 403 mV_{PP} and a 175 mA_{PP} ripple current.

Figure 20 presents the switching waveforms of the designed PSFB power module after the inclusion of the HV battery and wiring power harnesses, which refers to the full DC powertrain setup. The efficiency of the converter drops to 96.62% after its inclusion in the test setup, and the ripple of the voltage and current output waveforms is accentuated by 77 mV_{PP} and 34 mA_{PP}, respectively, knowing that D_{CLAMP1} and D_{CLAMP2} are also deactivated in this case.

The power cables generate EMI noise, and their resistance causes substantial voltage drops at high current loads, especially in the absence of a form of closed-loop control, which affects the output voltage and overall efficiency of the converter. However, for the application at hand, this effect is limited as the PSFB converter's closed-loop control circuit actively adjusts the duty cycle by effectively widening the on-time of the switching devices to compensate for the voltage drop occasioned by the inclusion of the power harnesses. This active adjustment is seen in the transformer secondary voltage V_{sec} depicted in Figure 21a.

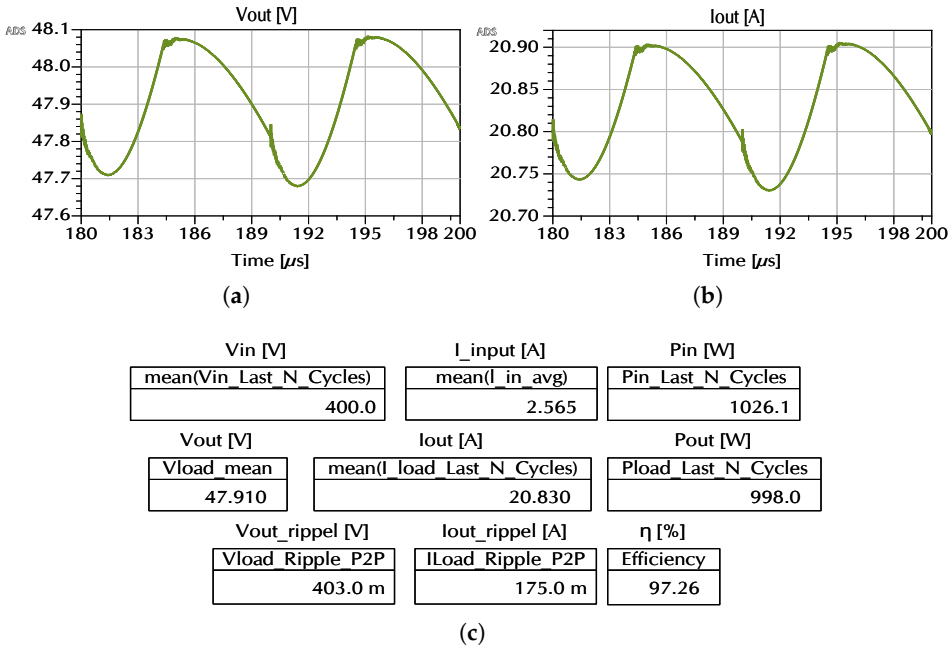


Figure 19. Overall performance of the PSFB converter with clamping diodes deactivated. (**a**) Output voltage. (**b**) Output current. (**c**) Rectangular plots at the last two switching cycles.

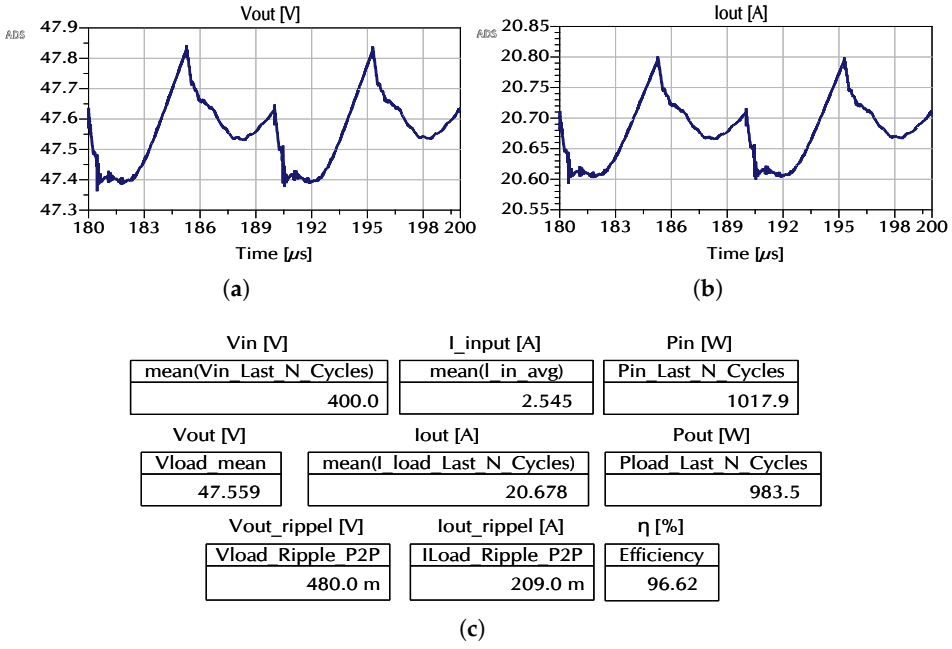
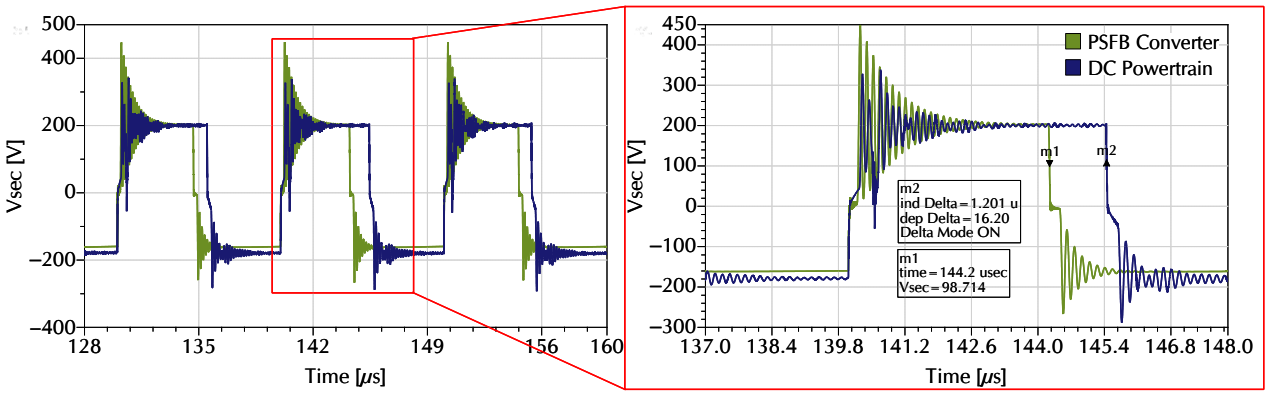
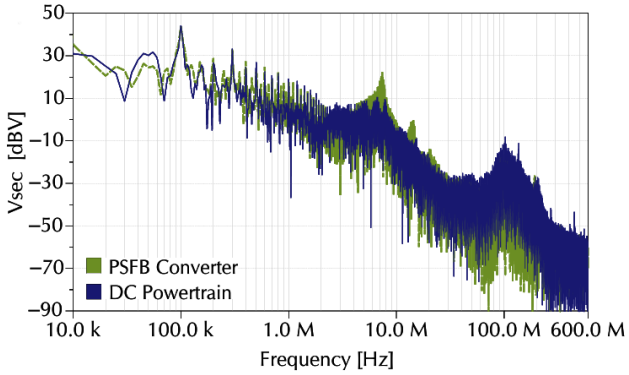


Figure 20. Overall performance of the DC powertrain with clamping diodes deactivated. (**a**) Output voltage. (**b**) Output current. (**c**) Rectangular plots at the last two switching cycles.

The FFT spectra of this secondary voltage before and after the inclusion of the PSFB converter within the DC powertrain have similar spectral profiles that showcase two noise peaks at nearly 7 MHz and 100 MHz, which are related to their transient turn-on and turn-off noise oscillations. The addition of the power harnesses, which exhibit an additional resistance, introduces a damping effect on the noise oscillations of V_{sec}, which is reflected in the magnitude of its related mid-frequency spectral noise peaks. The conducted EMI spectra of the PSFB converter before and after its inclusion within the DC powertrain are shown in Figure 22. Their trend correlates with the noise source impedances in Figure 18.

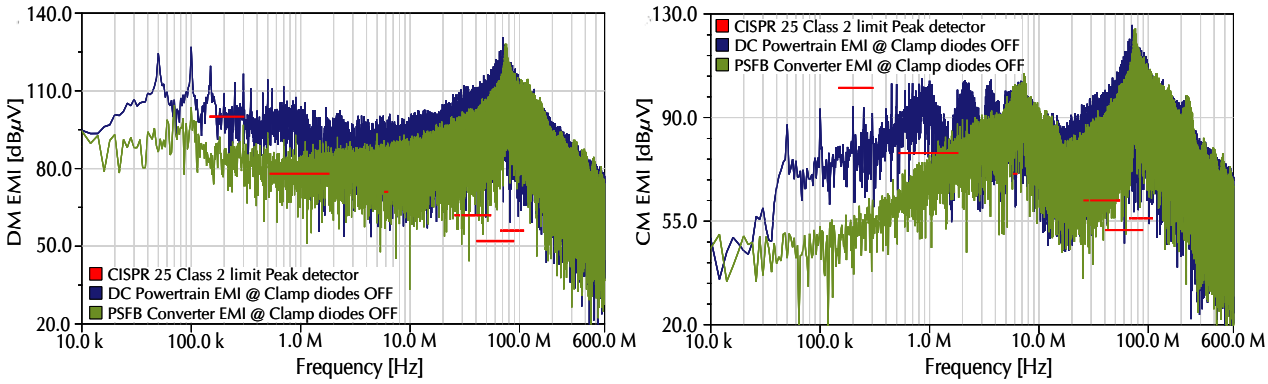


(**a**)



(**b**)

Figure 21. V_{sec} of the PSFB converter alone and within the DC powertrain with D_{CLAMP1} and D_{CLAMP2} off. (**a**) Transient waveform. (**b**) Spectral content.



(**a**) (**b**)

Figure 22. EMI noise of the PSFB converter alone and within the DC powertrain. (**a**) DM noise. (**b**) CM noise.

The CM and DM noise levels of the PSFB converter in standalone mode and within the DC powertrain both exceed the Class 2 limit, causing the PSFB converter to fail to meet the CISPR 25 standard. The effect of the wiring harnesses on the levels of induced EMI is noticeable, as the CM and DM noise levels of the DC powertrain increase considerably in the frequency range below 100 MHz. For instance, a difference of 38.15 dBμV in magnitude is estimated for the DM noise at 50 kHz, which is apparently due to the distributed inductance and resistance of the cables.

As for the CM noise, the difference observed is higher at low frequencies (e.g., 45.22 dBμV at 50 kHz), which is attributed to the low impedance path introduced

by the inclusion of the wiring harnesses through stray capacitances, which heightens the amount of capacitive CM noise currents along the cables toward the reference ground. Figure 23 shows the transformer secondary voltage waveforms evaluated within the DC powertrain before and after the inclusion of clamping diodes D_{CLAMP1} and D_{CLAMP2}. Figure 24 shows the conducted CM and DM noise spectra before and after their inclusion.

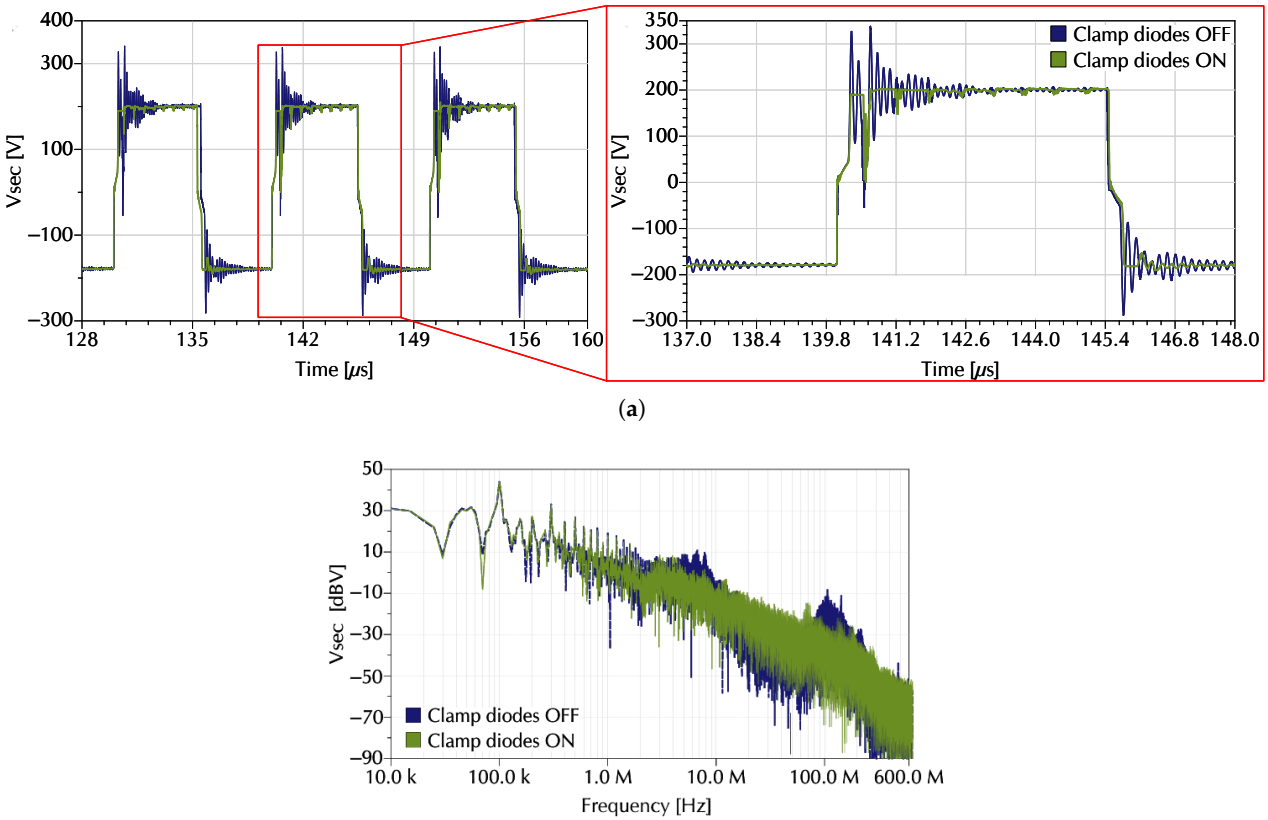


Figure 23. V_{sec} of the DC Powertrainwith D_{CLAMP1} and D_{CLAMP2} in off-state and on-state. (**a**) Transient waveform. (**b**) Spectral.

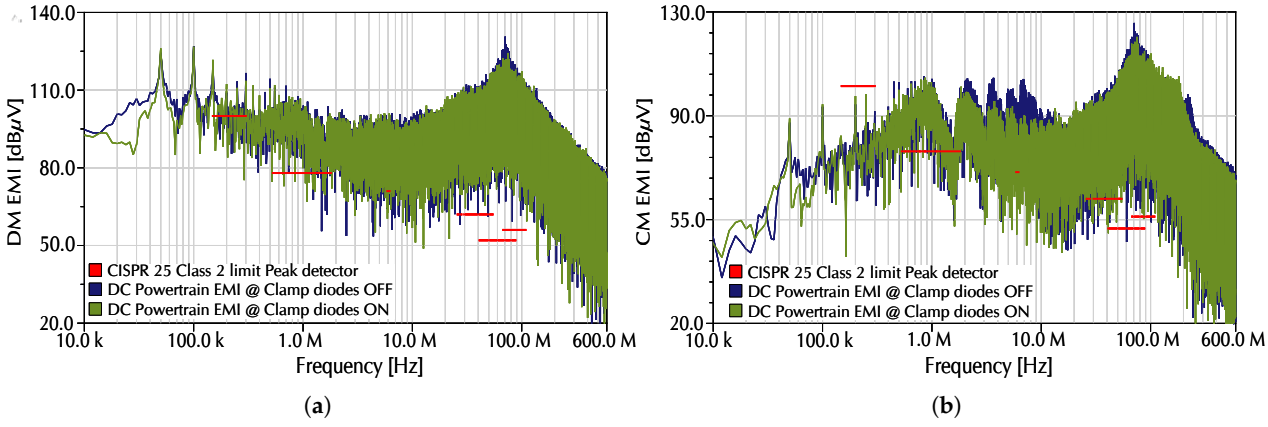


Figure 24. DC Powertrain EMI spectra with D_{CLAMP1} and D_{CLAMP2} in off-state and on-state. (**a**) DM noise. (**b**) CM noise.

The following quantitative correlations can be established with the parasitic values listed in Table 2. The DM impedance (Figure 17a) exhibits three distinct regions: capacitive below 10 kHz (C_{IN_total} = 1120 µF, i.e., 2 × C_{IN}), a resistive plateau between 10 kHz and 1 MHz corresponding to the equivalent parallel resistance ESR_{total} = 31.5 mΩ, and induc-

tive above 1 MHz corresponding to the equivalent parallel inductance $ESL_{\text{total}} = 4.9$ nH. The highest DM emission peak at 75.21 MHz (Figure 24a, EMI with clamping diodes off) is caused by a resonance between the transformer inter-winding capacitance $C_T = 60.42$ pF and the residual DM loop inductance $L_{\text{loop_DM}} \approx 74.2$ nH, which includes the contribution of the power harnesses. This peak lies in the inductive region above 1 MHz, where ESL_{total} and the harness inductance dominate the DM impedance.

The CM impedance (Figure 17b) is purely capacitive below 10 MHz, dominated by $C_{\text{CM_eq}} = C_{\text{pri}} + C_T = 313.22$ pF. A sharp series resonance dip occurs near 30.33 MHz, where the phase crosses 0°, corresponding to the cancellation between $L_{\text{pri_lk}}$ and the equivalent series capacitance of the layout. The PSFB exhibits a first CM emission peak observed at 7 MHz (Figure 22b, green spectrum). This peak is caused by the resonance between $L_{\text{pri_lk}}$ and the transformer inter-winding capacitance $C_T = 60.42$ pF, which gives a theoretical resonant frequency of approximately $1/(2\pi\sqrt{12.21\mu \cdot 60.42p}) \approx 5.9$ MHz, in good agreement with the peak observed near 7 MHz (slightly shifted by layout parasitics). The highest CM emission peak at 75.21 MHz lies in the inductive zone following the 30.33 MHz resonance dip and is attributed to a parasitic resonance between $C_{\text{CM_eq}}$ and the residual high-frequency loop inductance of the PCB and harnesses ($L_{\text{loop_CM}} \approx 14.3$ nH).

Going from the off-state to the on-state of D_{CLAMP1} and D_{CLAMP2} in Figure 23a, the overshoots and undershoots are greatly reduced by 136.1 V and 24.61 V, respectively. As for their spectra (Figure 23b), the two noise peaks observed near 7 MHz and 100 MHz in the off-state of D_{CLAMP1} and D_{CLAMP2} are remarkably damped when these latter are turned on (e.g., 12.35 dBV reduction at 6.7 MHz, and 19.44 dBV at 102.4 MHz). The utilization of a diode clamp at the primary stage of the PSFB converter (see Figure 8) enables the recycling of energy within the discrete commutating inductor L_s, thus maintaining it on the primary side and ensuring that the parasitic capacitances of the output rectifiers resonate with only the primary leakage inductance, which is already substantial for the designed transformer ($L_{\text{pri_lk}} = 12.21$ µH), thereby reducing the output rectifier voltage stress considerably.

Although the conducted CM and DM noise contribution of the full DC powertrain shown in Figure 24 remains high in terms of induced EMI levels after activating the clamping diodes, the effect of these latter is noticeable as it introduces some amount of damping on the CM and DM spectra. For instance, the DM noise spectrum exhibits a reduction of 3.6 dBµV at 500 kHz, and 12.69 dBµV is estimated at the main noise peak, which occurs at around 70.45 MHz. As for the CM noise spectrum, the damping is more pronounced, especially in the mid-frequency range from 2 MHz to 13.20 MHz, where a maximum decrease of 20.91 dBµV is reached at 3.658 MHz. At the high-frequency range, a 3.69 dBµV reduction is noted at 70.45 MHz. The summary of the main performances of the designed converter, evaluated under full-load conditions, along with its compliance status with the CISPR 25 standard, is presented in Table 3.

Table 3. PSFB converter performance and EMI under full load (clamp diodes on-state).

Configuration	Efficiency [%]	CM Noise	DM Noise
PSFB converter alone	97.26	Exceeds CISPR 25 Class 2	Exceeds CISPR 25 Class 2
Full DC powertrain	97.03	Exceeds CISPR 25 Class 2	Exceeds CISPR 25 Class 2

The PSFB converter achieves better efficiency and power density in standalone mode, but this is degraded within the full DC powertrain. In terms of EMC compliance, however, the PSFB converter fails to meet the CISPR 25 Class 2 limit in all cases. This noise quantification therefore provides a robust evaluation of the conducted EMI levels of the

power system and establishes a clear baseline and a correct starting point for implementing a well-dimensioned noise mitigation strategy, such as a dedicated EMI filter.

4. Conclusions

This paper establishes a comprehensive broadband simulation-based EMC modeling and EMI assessment methodology for a 1 kW GaN-based phase-shift full-bridge converter in an EV DC powertrain. By combining full-wave electromagnetic and circuit-level simulations, the proposed approach accurately captures parasitic effects from PCB layout, power harnesses, and discrete components, enabling reliable system-level EMI prediction.

The virtual prototype was assessed within a CISPR 25-compliant setup over the 150 kHz–108 MHz range. Simulation results showed that the converter achieves high efficiency above 97% under full load conditions (97.26% standalone, 97.03% integrated). However, in the absence of proper input filtering, even with the integral clamping diodes activated, both common-mode and differential-mode conducted emissions exceed CISPR 25 Class 2 limits across the entire spectrum. Power harnesses were found to significantly increase EMI levels at low frequencies due to distributed inductance and stray capacitance.

The undamped conducted EMI levels presented in this study (with clamping diodes ON) serve as a baseline reference for future input EMI filter design. This work demonstrates the value of virtual prototyping for simulation-based EMI prediction, enabling designers to identify EMC compliance issues before physical prototyping and to size proper, dedicated filtering stages. Future work will also explore active common mode EMI cancellation techniques, such as impedance balancing and transformer parasitic capacitance compensation, to further improve the EMC performance of the GaN-based PSFB converter.

A full CISPR 25 compliance study through PCB or component optimization is left for future work. Furthermore, a comparative study of the EMI performance of different isolated topologies (LLC, DAB, etc.) and of Si versus GaN devices would be a valuable extension of this work and is planned for the future.

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Abbreviations

The following abbreviations are used in this manuscript:

ADS	Advanced Design System
CM	Common-mode
CISPR	Comité International Spécial des Perturbations Radioélectriques
DC	Direct current
DM	Differential-mode
EM	Electromagnetic
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference

EV	Electric vehicle
FEM	Finite element method
FFT	Fast Fourier transform
GaN	Gallium nitride
HV	High voltage
LISN	Line impedance stabilization network
LV	Low voltage
PCB	Printed circuit board
PSFB	Phase-shift full-bridge
SPICE	Simulation Program with Integrated Circuit Emphasis

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